

# SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCAS283E – JANUARY 1993 – REVISED MARCH 1997

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Packages, and DIPs (J)

## description

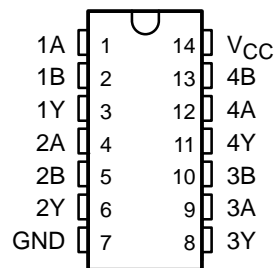
These quadruple 2-input positive-AND gates are designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The 'LVC08A perform the Boolean function  $Y = A \cdot B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

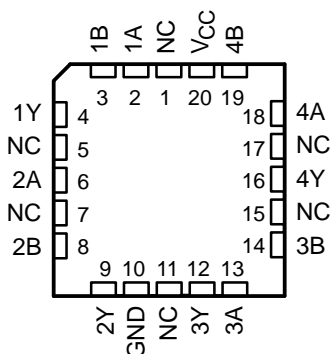
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-/5-V system environment.

The SN54LVC08A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVC08A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LVC08A ... J OR W PACKAGE  
SN74LVC08A ... D, DB, OR PW PACKAGE  
(TOP VIEW)



SN54LVC08A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L



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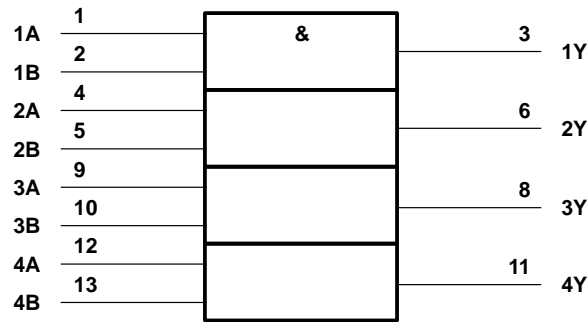
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QUADRUPLE 2-INPUT POSITIVE-AND GATES

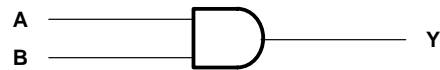
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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## recommended operating conditions (see Note 4)

			SN54LVC08A		SN74LVC08A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	2	3.6	V
		Data retention only	1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		0.8	V
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		–12		–12	mA
		V <sub>CC</sub> = 3 V		–24		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		12		12	mA
		V <sub>CC</sub> = 3 V		24		24	
Δt/Δv	Input transition rise or fall rate		0	8	0	8	ns/V
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC08A			SN74LVC08A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	2.7 V to 3.6 V	V <sub>CC</sub> –0.2			V <sub>CC</sub> –0.2			V
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I <sub>OH</sub> = –24 mA	3 V	2.2			2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V	0.2			0.2			V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±5			±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	10			10			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			5			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC08A				SN74LVC08A				UNIT
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	1	4.1	4.8		1	4.1	4.8		ns
t <sub>sk(o)</sub> <sup>‡</sup> *			1				1				ns

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

‡ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



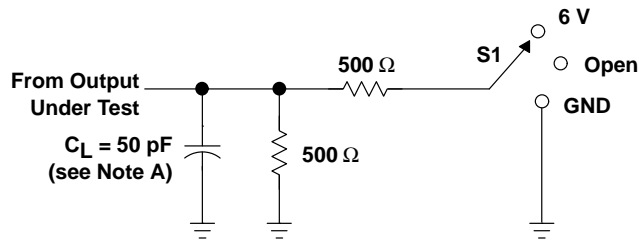
SN54LVC08A, SN74LVC08A  
QUADRUPLE 2-INPUT POSITIVE-AND GATES

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operating characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

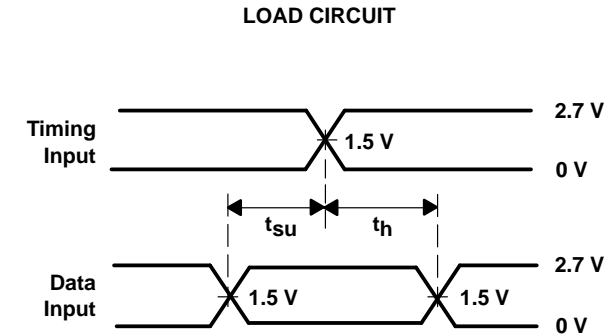
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per gate	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	10	pF

PARAMETER MEASUREMENT INFORMATION

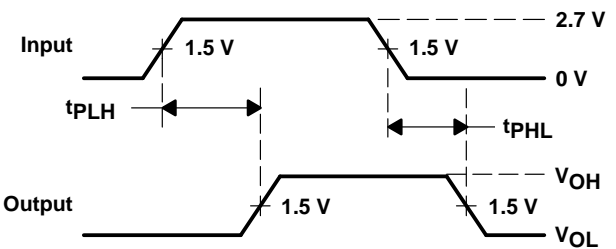


LOAD CIRCUIT

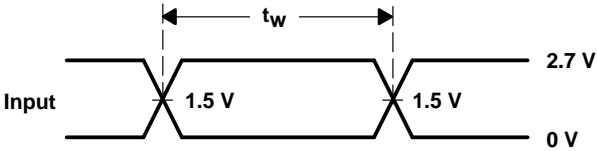
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



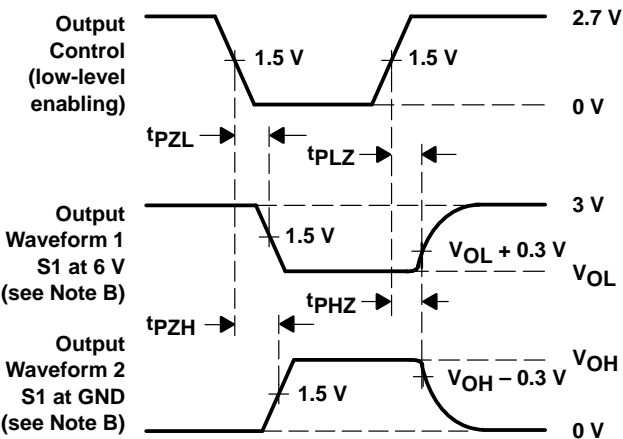
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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