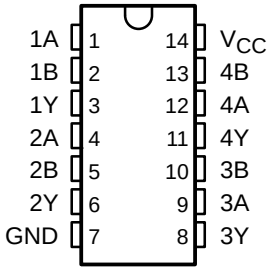
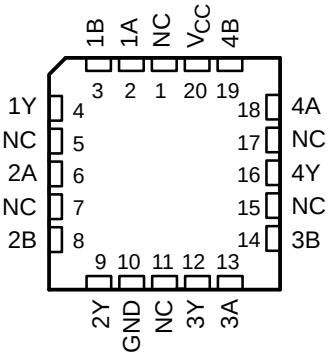
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Packages, and DIPs (J)**

SN54LVC00A . . . J OR W PACKAGE
SN74LVC00A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC00A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple 2-input positive-NAND gates are designed for 2.7-V to 3.6-V V_{CC} operation. The 'LVC00A perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

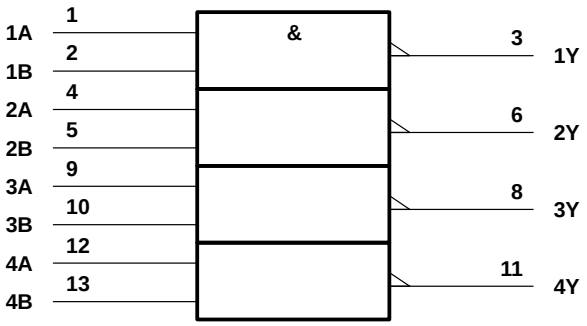
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC00A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVC00A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

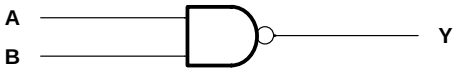
INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
PW package . . . . . 170°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

			SN54LVC00A		SN74LVC00A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	2	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12		–12	mA
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12		12	mA
		V_{CC} = 3 V		24		24	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC00A			SN74LVC00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	I_{OH} = –100 μA	2.7 V to 3.6 V	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I_{OH} = –24 mA	3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 μA	2.7 V to 3.6 V			0.2			0.2	V
	I_{OL} = 12 mA	2.7 V			0.4			0.4	
	I_{OL} = 24 mA	3 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			10			10	μA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		5			5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

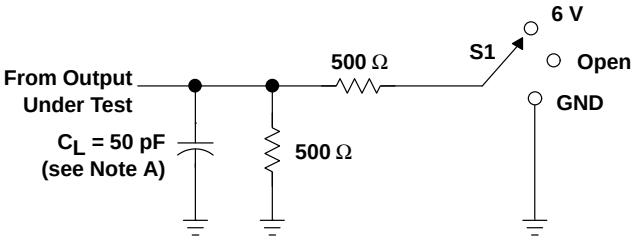
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC00A				SN74LVC00A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	1	4.3		5.1	1	4.3		5.1	ns
$t_{sk(o)}$‡*				1				1			ns

* On products compliant to MIL-PRF-38535, this parameter does not apply.
‡ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

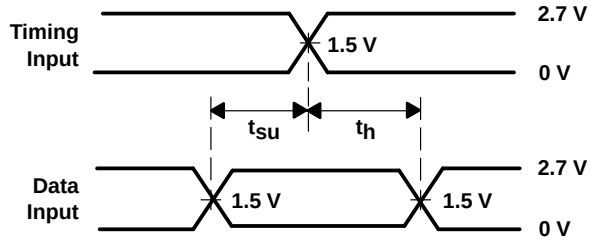
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 10 MHz	9.5	pF

PARAMETER MEASUREMENT INFORMATION

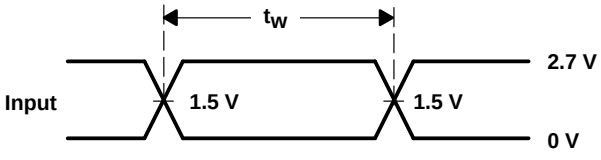


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

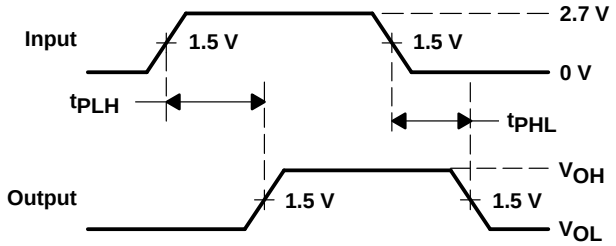
LOAD CIRCUIT



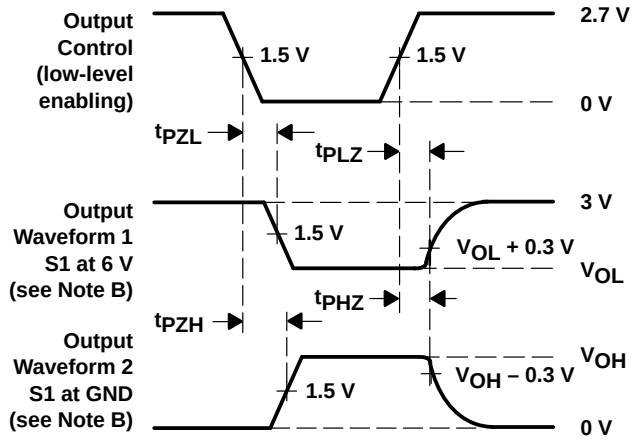
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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