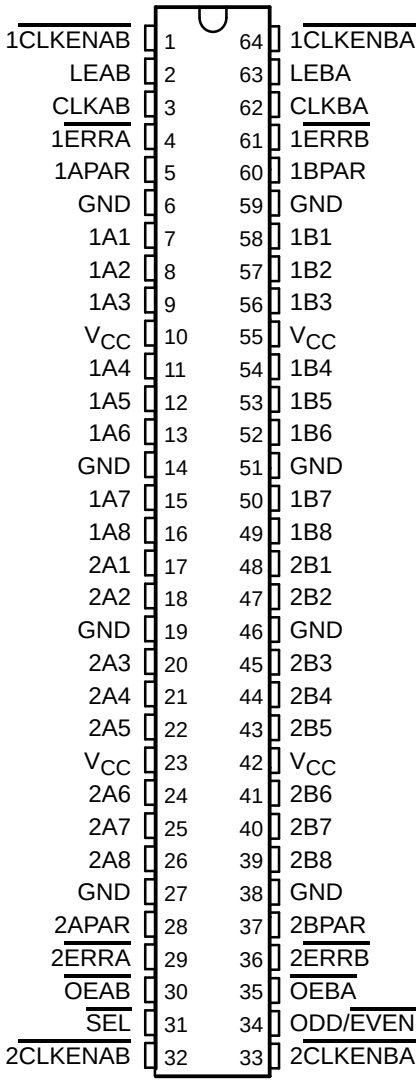
- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Simultaneously Generates and Checks Parity**
- **Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 500 mA**
- **Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

## description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 2.7-V to 3.6-V $V_{CC}$ operation.

The ′ALVC16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The ′ALVC16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/$\overline{\text{EVEN}}$) inputs and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

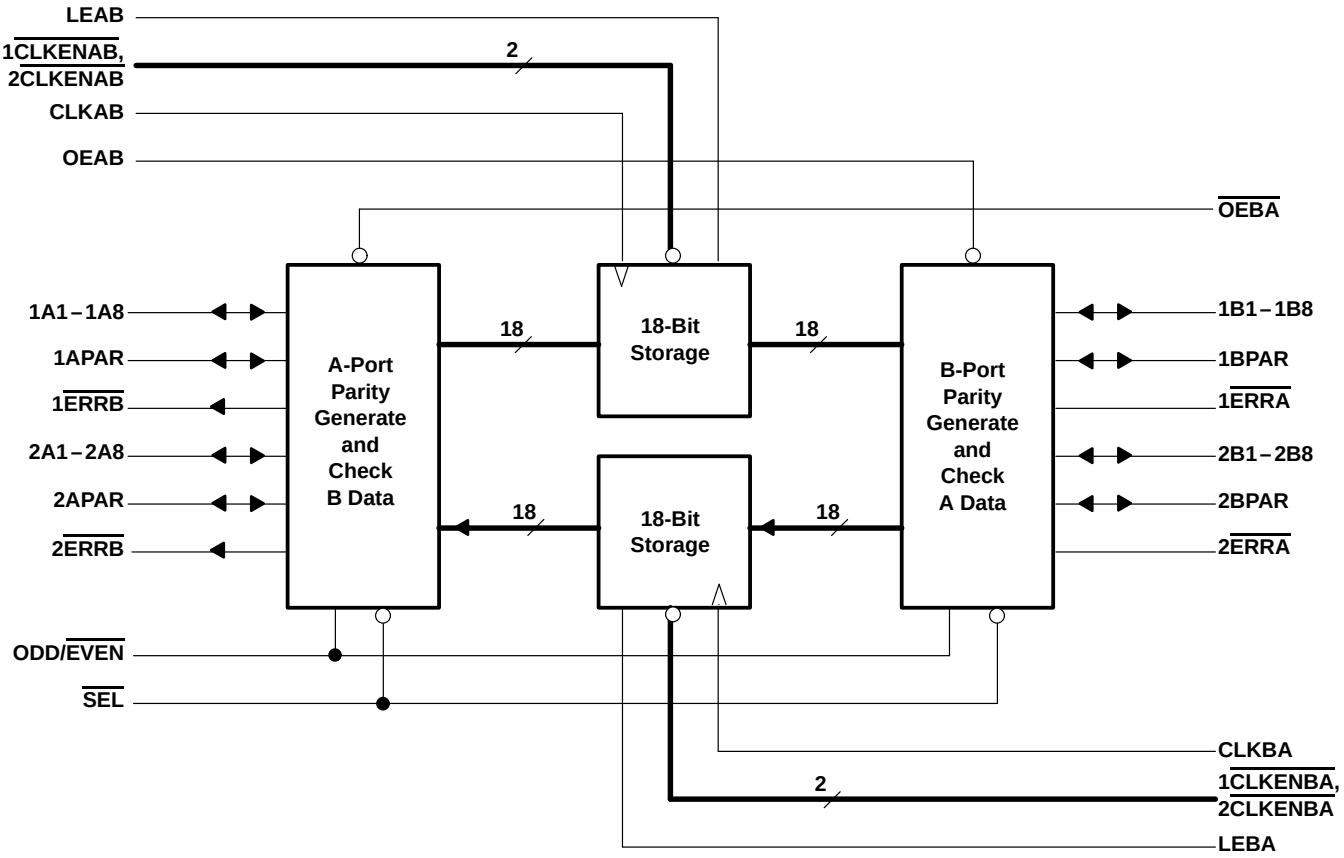
The SN74ALVC16901 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16901 is characterized for operation from –40°C to 85°C.

Widebus+, EPIC, and UBT are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

## block diagram




**FUNCTION TABLE†**

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{\text{CLKENAB}}$ | $\overline{\text{OEAB}}$ | LEAB | CLKAB | A | B |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | $B_0$‡ |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | $B_0$‡ |
| L | L | L | H | X | $B_0$§ |

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

**PARITY-ENABLE FUNCTION TABLE**

| INPUTS | | | OPERATION OR FUNCTION | |
|---|---|---|---|---|
| $\overline{SEL}$ | $\overline{OEBA}$ | $\overline{OEAB}$ | | |
| L | H | L | Parity is checked on port A and is generated on port B | |
| L | L | H | Parity is checked on port B and is generated on port A | |
| L | H | H | Parity is checked on port B and port A | |
| L | L | L | Parity is generated on port A and B if device is in FF mode | |
| H | L | L | Parity functions are disabled, device acts as a standard 18-bit registered transceiver | $Q_A$ data to B, $Q_B$ data to A |
| H | L | H | | $Q_B$ data to A |
| H | H | L | | $Q_A$ data to B |
| H | H | H | | Isolation |

**PARITY FUNCTION TABLE**

| INPUTS | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{SEL}$ | $\overline{OEBA}$ | OEAB | ODD/$\overline{EVEN}$ | Σ OF INPUTS A1 – A8 = H | Σ OF INPUTS B1 – B8 = H | APAR | BPAR | APAR | $\overline{ERRA}$ | BPAR | $\overline{ERRB}$ |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | H | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | L | N/A | N/A | L | H | Z |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | L | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | H | N/A | N/A | H | H | Z |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | L | L | Z | N/A | H |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | L | H | Z | N/A | L |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | H | L | Z | N/A | L |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | H | H | Z | N/A | H |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | L | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | L | N/A | N/A | H | L | Z |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | H | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | H | N/A | N/A | L | L | Z |
| L | L | H | H | N/A | 0, 2, 4, 6, 8 | N/A | L | H | Z | N/A | L |
| L | L | H | H | N/A | 1, 3, 5, 7 | N/A | L | L | Z | N/A | H |
| L | L | H | H | N/A | 0, 2, 4, 6, 8 | N/A | H | H | Z | N/A | H |
| L | L | H | H | N/A | 1, 3, 5, 7 | N/A | H | L | Z | N/A | L |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | H | Z | H |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | L | Z | L |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | L | Z | L |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | H | Z | H |
| L | H | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | L | Z | L |
| L | H | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | H | Z | H |
| L | H | H | H | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | H | Z | H |
| L | H | H | H | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | L | Z | L |
| L | L | L | L | N/A | N/A | N/A | N/A | PE† | Z | PE† | Z |
| L | L | L | H | N/A | N/A | N/A | N/A | PO‡ | Z | PO‡ | Z |

† Parity output is set to the level so that the specific bus side is set to even parity.
‡ Parity output is set to the level so that the specific bus side is set to odd parity.

PRODUCT PREVIEW

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (I/O ports) (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND pins . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

### recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7 V | | –12 | mA |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7 V | | 12 | mA |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $I_I$ = –18 mA | | 2.7 V | | | –1.2 | V |
| $V_{OH}$ | | $I_{OH}$ = –100 μA | | MIN to MAX | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | |
| | | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | MIN to MAX | | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | Control pins | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | Data I/Os | $V_I$ = 0.8 V | | 3 V | 75 | | | μA |
| | | $V_I$ = 2 V | | | –75 | | | |
| $I_{OZ}$‡ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | $V_{CC}$ = 3 V to 3.6 V, Other inputs at $V_{CC}$ or GND | One input at $V_{CC}$ – 0.6 V, | | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | | | pF |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

PRODUCT PREVIEW

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.