- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V_{CC}	7	50	V_{CC}
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
2$\overline{OE}$	28	29	2LE

PRODUCT PREVIEW

description

This 20-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVC16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable (1$\overline{OE}$ or 2$\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16841 is characterized for operation from −40°C to 85°C.
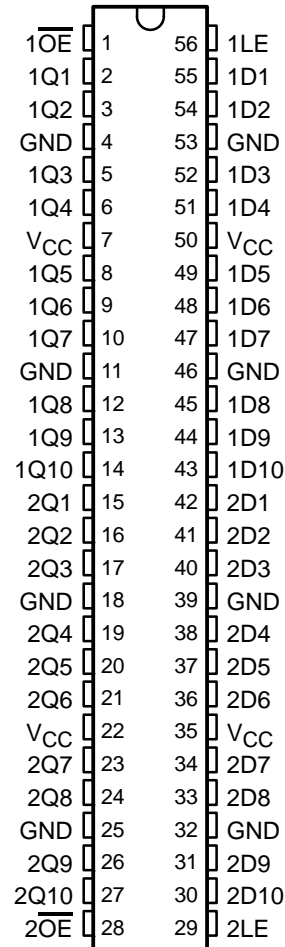
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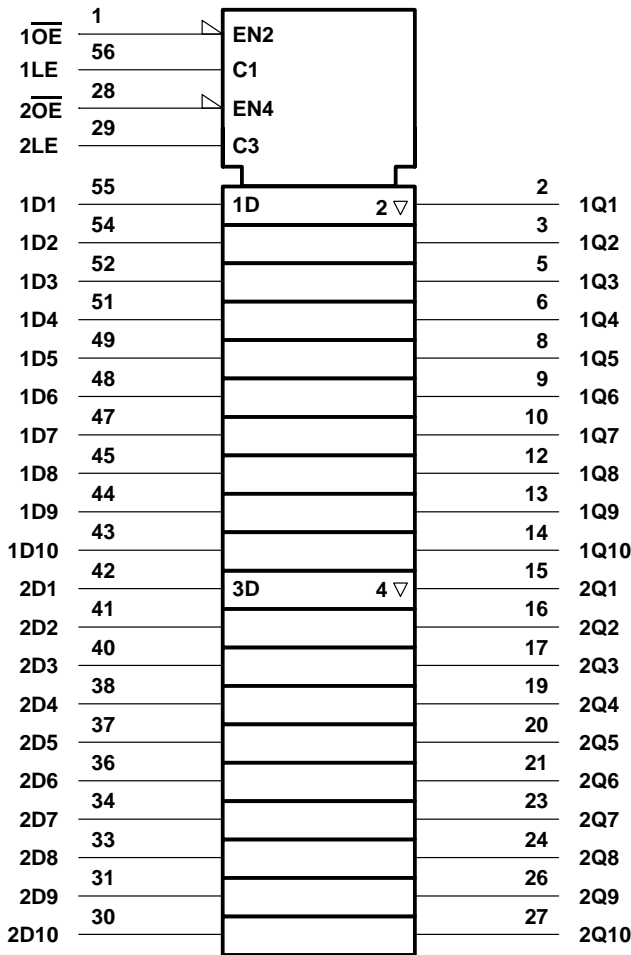
TEXAS INSTRUMENTS

SN74ALVC16841
20-BIT BUS-INTERFACE D-TYPE LATCH
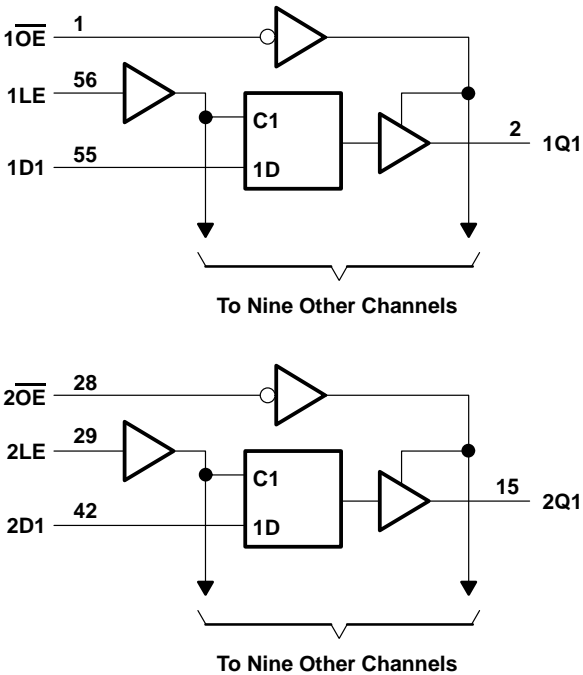## WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol[†]

Pin	Label		Label	Pin
1	1$\overline{OE}$ → EN2			
56	1LE — C1			
28	2$\overline{OE}$ → EN4			
29	2LE — C3			
55	1D1 — 1D	2 ▽	1Q1	2
54	1D2		1Q2	3
52	1D3		1Q3	5
51	1D4		1Q4	6
49	1D5		1Q5	8
48	1D6		1Q6	9
47	1D7		1Q7	10
45	1D8		1Q8	12
44	1D9		1Q9	13
43	1D10		1Q10	14
42	2D1 — 3D	4 ▽	2Q1	15
41	2D2		2Q2	16
40	2D3		2Q3	17
38	2D4		2Q4	19
37	2D5		2Q5	20
36	2D6		2Q6	21
34	2D7		2Q7	23
33	2D8		2Q8	24
31	2D9		2Q9	26
30	2D10		2Q10	27

logic diagram (positive logic)

To Nine Other Channels

To Nine Other Channels

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS
INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 4.6 V

Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) .... −50 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA

Continuous current through V_{CC} or GND .... ±100 mA

Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package .... 1 W
DL package .... 1.4 W

Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu A$		MIN to MAX	$V_{CC}-0.2$	V
	$I_{OH} = -12\ mA$		2.7 V	2.2	
			3 V	2.4	
	$I_{OH} = -24\ mA$		3 V	2	
V_{OL}	$I_{OL} = 100\ \mu A$		MIN to MAX	0.2	V
	$I_{OL} = 12\ mA$		2.7 V	0.4	
	$I_{OL} = 24\ mA$		3 V	0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V	±5	μA
$I_{I(hold)}$	$V_I = 0.8\ V$		3 V	75	μA
	$V_I = 2\ V$			−75	
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V	±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V	40	μA
$\triangle I_{CC}$	$V_{CC} = 3\ V$ to 3.6 V, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\ V$,		750	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

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