

# SN74ALVC16825

## 18-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCAS271 – OCTOBER 1993 – REVISED MARCH 1994

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50  $\Omega$  or Greater
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

The SN74ALVC16825 is an 18-bit buffer and line driver designed for 2.7-V to 3.6-V  $V_{CC}$  operation. It will improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

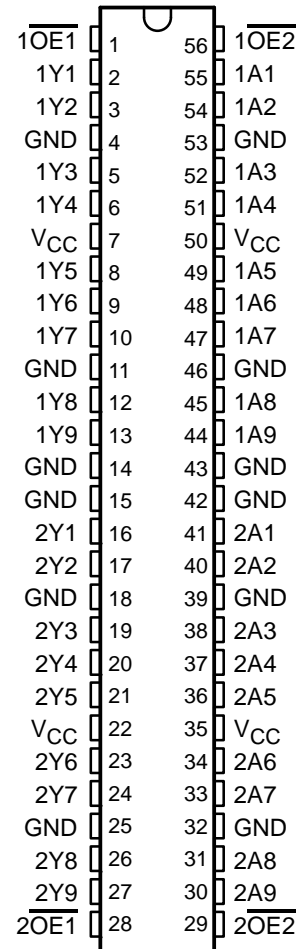
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all nine affected outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16825 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16825 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### DGG OR DL PACKAGE (TOP VIEW)



FUNCTION TABLE  
(each 9-bit section)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

PRODUCT PREVIEW

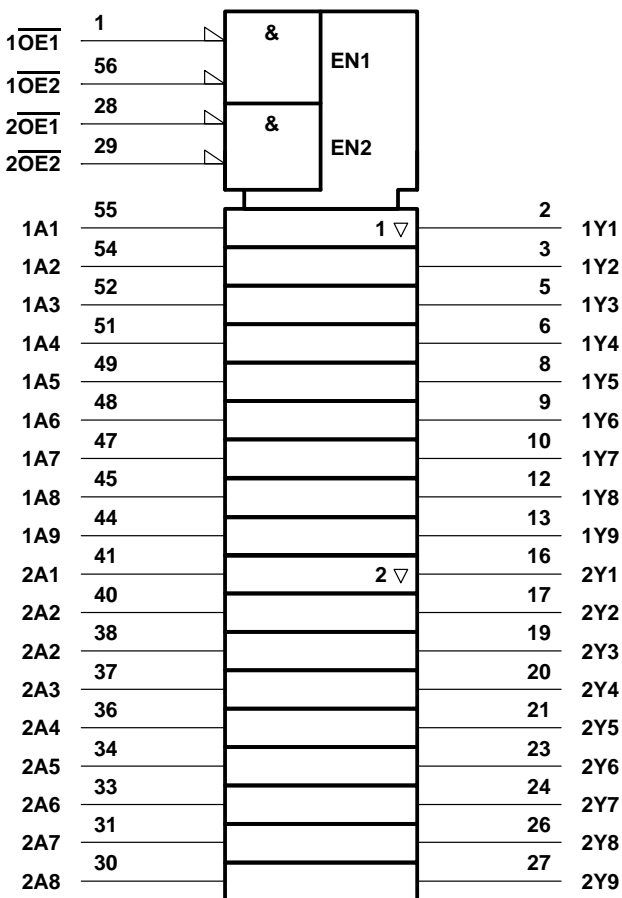
# SN74ALVC16825

## 18-BIT BUFFER/DRIVER

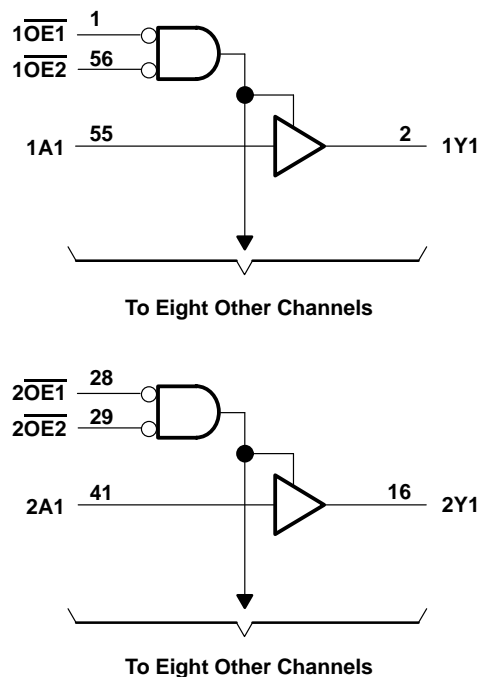
### WITH 3-STATE OUTPUTS

SCAS271 – OCTOBER 1993 – REVISED MARCH 1994

#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 4.6 V
Input voltage range, $V_I$ (I/O ports) (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 4.6 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

**SN74ALVC16825**  
**18-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS271 – OCTOBER 1993 – REVISED MARCH 1994

**recommended operating conditions**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V}$		-12	mA
		$V_{CC} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V}$		12	mA
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	5	ns/V
$T_A$	Operating free-air temperature		-40	85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	MIN	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	MIN to MAX	V <sub>CC</sub> − 0.2		V
		I <sub>OH</sub> = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I <sub>OH</sub> = −24 mA	3 V	2		
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	MIN to MAX	0.2		V
		I <sub>OL</sub> = 12 mA	2.7 V	0.4		
		I <sub>OL</sub> = 24 mA	3 V	0.55		
I <sub>I</sub>	Control pins	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5		μA
I <sub>I</sub> (hold)	Data pins	V <sub>I</sub> = 0.8 V	3 V	75		μA
		V <sub>I</sub> = 2 V		−75		
I <sub>OZ</sub> <sup>‡</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10		μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40		μA
ΔI <sub>CC</sub>		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		750		μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

**PRODUCT PREVIEW**



## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.