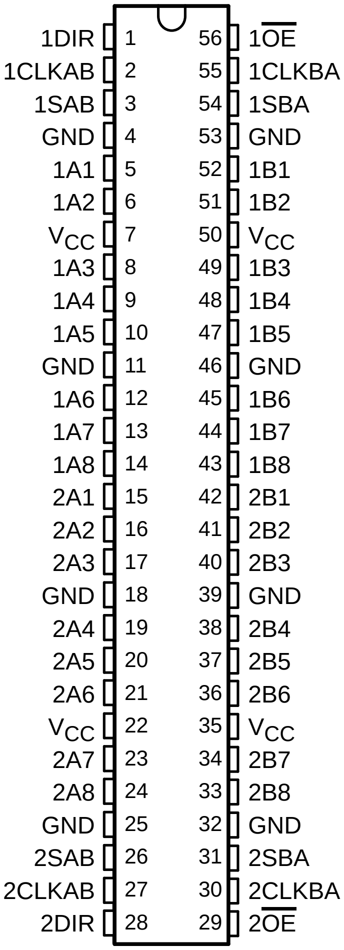
SN74ALVC16646
16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS265 – JANUARY 1993 – REVISED MARCH 1994

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



1DIR	1	56	1$\overline{OE}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	2$\overline{OE}$

description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74ALVC16646 is available in TI’s shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16646 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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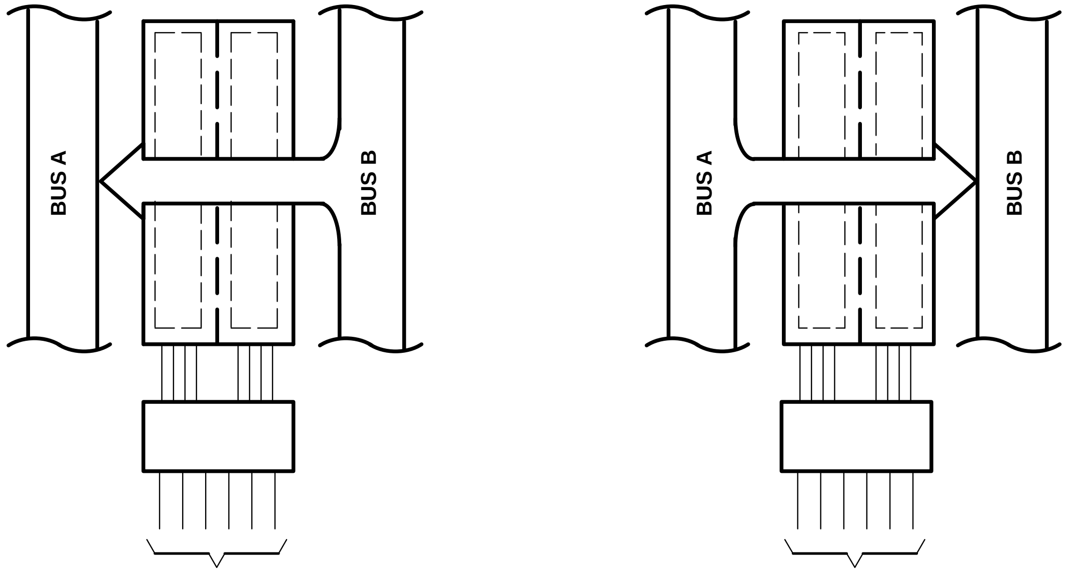
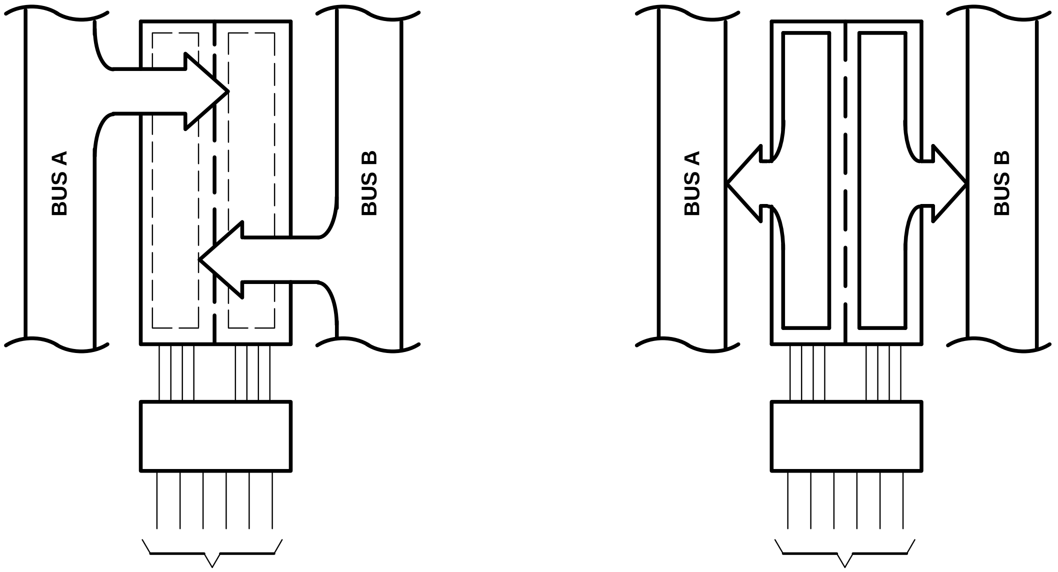


$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A

$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

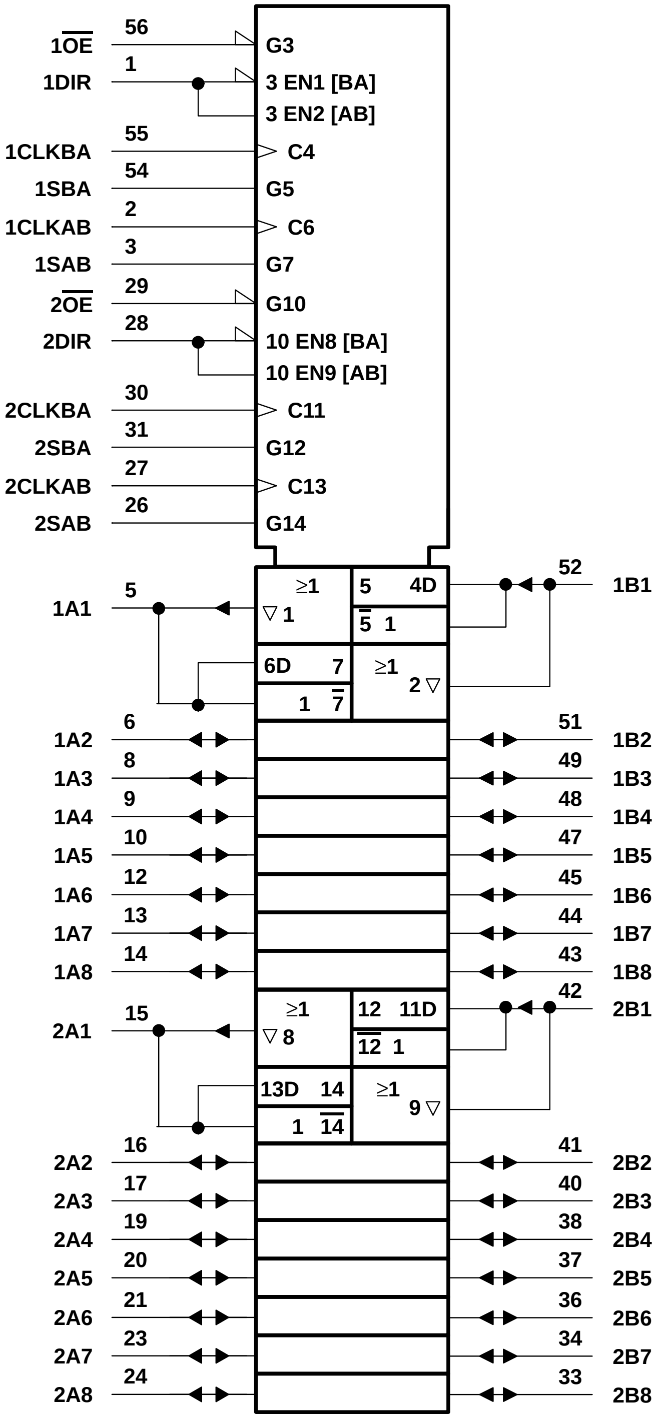
STORAGE FROM
A, B, OR A AND B

$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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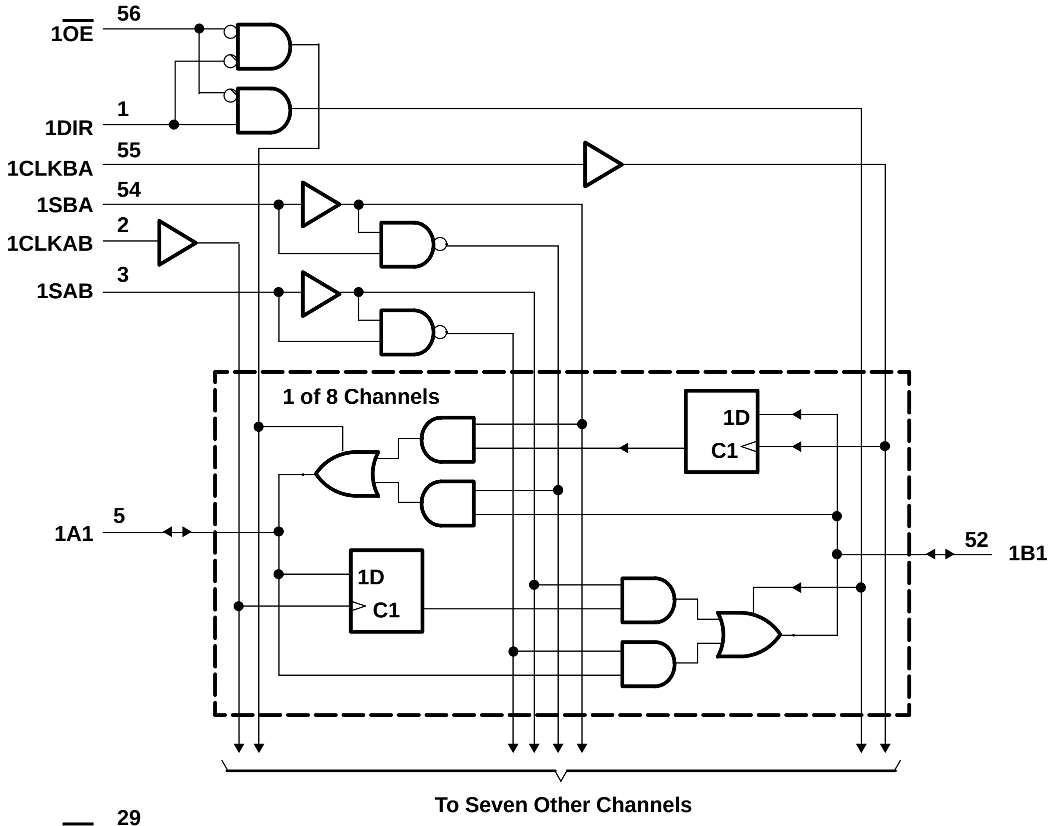
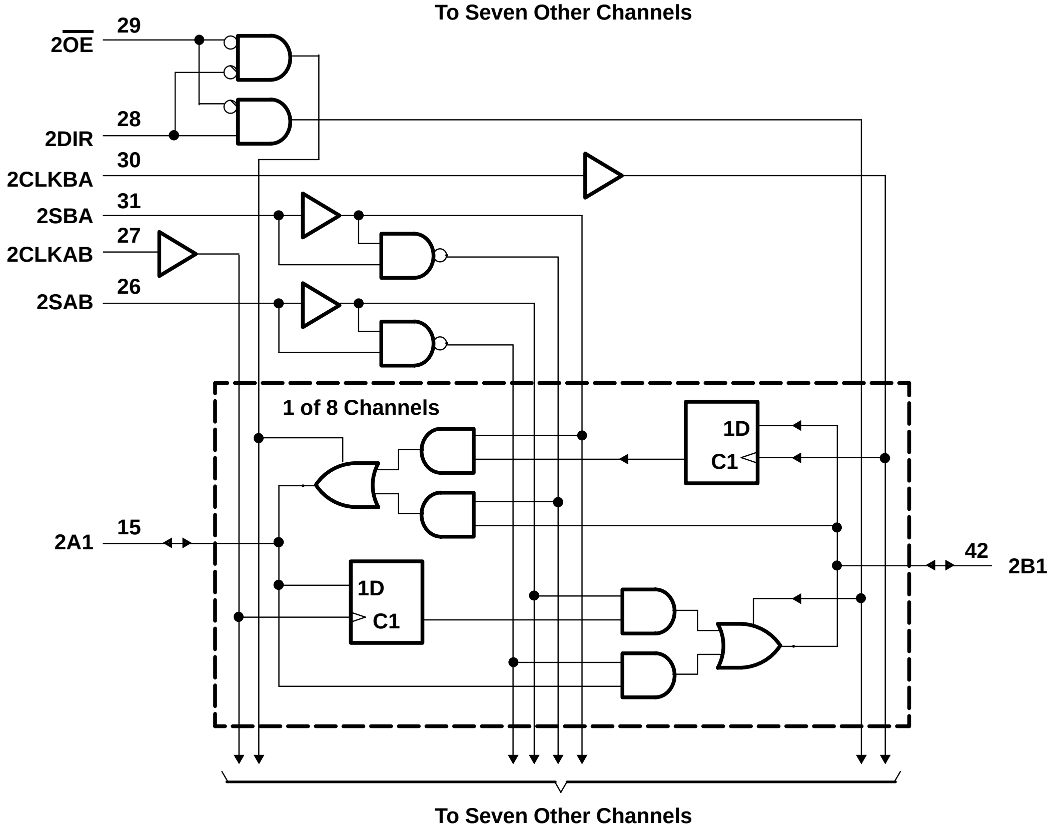
logic diagram (positive logic)





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FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified[†]	Store A, B unspecified[†]
X	X	X	↑	X	X	Unspecified[†]	Input	Store B, A unspecified[†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}		–0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1)		–0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2)		–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)		–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V_{CC} or GND		±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3):	DGG package	1 W
	DL package	1.4 W
Storage temperature range		–65°C to 150°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		V_I = V_{CC} or GND	3.6 V		±5	µA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		µA
		V_I = 2 V		–75		
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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