- **Members of the Texas Instruments**
  Widebus ™ **Family**

- **Provides Extra Data Width Necessary for**
  Wider Address/Data Paths or Buses With
  Parity

- **Flow-Through Architecture Optimizes**
  PCB Layout

- **Distributed V$_{CC}$ and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- *EPIC* ™ **(Enhanced-Performance Implanted**
  CMOS) 1-μm Process

- **500-mA Typical Latch-Up Immunity**
  at 125°C

- **Package Options Include Plastic 300-mil**
  Shrink Small-Outline (DL) Package Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Package Using 25-mil Center-to-Center Pin
  Spacings

54AC16823 . . . WD PACKAGE
74AC16823 . . . DL PACKAGE
(TOP VIEW)

1CLR	1	56	1CLK
1OE	2	55	1CLKEN
1Q1	3	54	1D1
GND	4	53	GND
1Q2	5	52	1D2
1Q3	6	51	1D3
V$_{CC}$	7	50	V$_{CC}$
1Q4	8	49	1D4
1Q5	9	48	1D5
1Q6	10	47	1D6
GND	11	46	GND
1Q7	12	45	1D7
1Q8	13	44	1D8
1Q9	14	43	1D9
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V$_{CC}$	22	35	V$_{CC}$
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2OE	27	30	2CLKEN
2CLR	28	29	2CLK
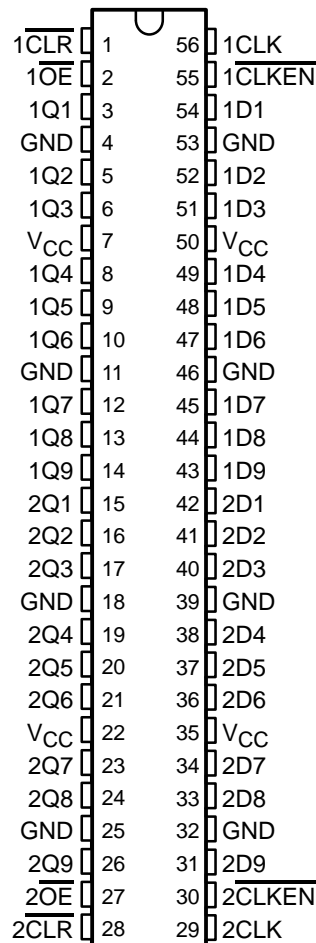
description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

The 'AC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

The output enable (OE) input can be used to place the outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16823 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16823 is characterized for operation from –40°C to 85°C.

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FUNCTION TABLE
(each 9-bit stage)

INPUTS					OUTPUT
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†

Pin	Label				Pin	Label
2	1$\overline{\text{OE}}$ → EN1					
1	1$\overline{\text{CLR}}$ → R2					
55	→ G3					
56	1CLK → 3C4					
27	2$\overline{\text{OE}}$ → EN5					
28	2$\overline{\text{CLR}}$ → R6					
30	→ G7					
29	2CLK → 7C8					

In	Pin	Block	Pin	Out
1D1	54	4D 1, 2 ▽	3	1Q1
1D2	52		5	1Q2
1D3	51		6	1Q3
1D4	49		8	1Q4
1D5	48		9	1Q5
1D6	47		10	1Q6
1D7	45		12	1Q7
1D8	44		13	1Q8
1D9	43		14	1Q9
2D1	42	8D 5, 6 ▽	15	2Q1
2D2	41		16	2Q2
2D3	40		17	2Q3
2D4	38		19	2Q4
2D5	37		20	2Q5
2D6	36		21	2Q6
2D7	34		23	2Q7
2D8	33		24	2Q8
2D9	31		25	2Q9
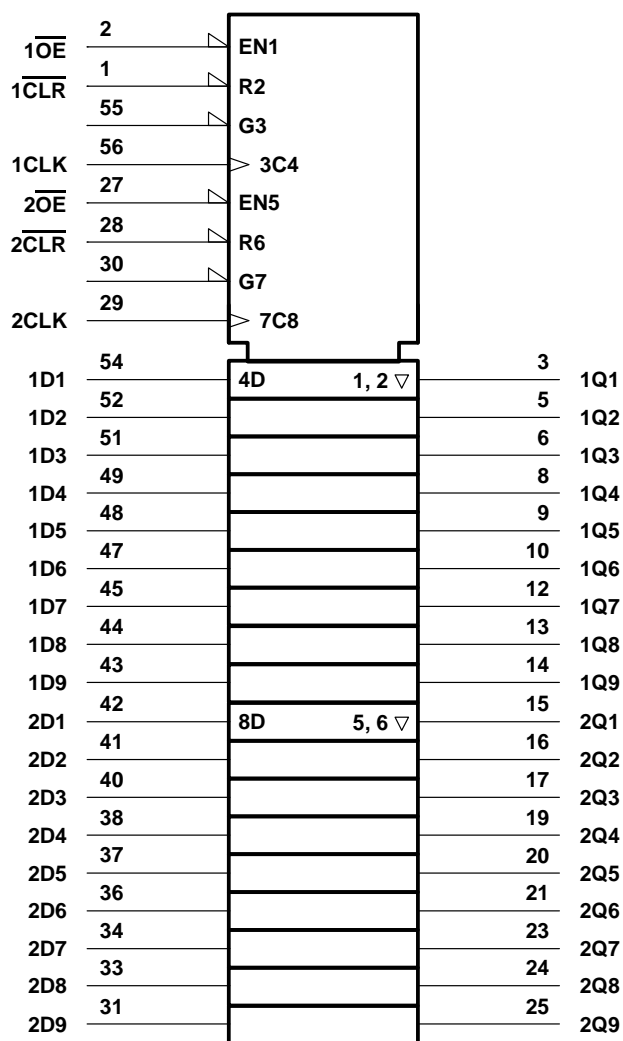
logic diagram (positive logic)

1$\overline{\text{OE}}$ 2
1$\overline{\text{CLR}}$ 1
1$\overline{\text{CLKEN}}$ 55
1CLK 56
1D1 54

R
CE
C1
1D

3 1Q1

One of Nine Channels

To Eight Other Channels

2$\overline{\text{OE}}$ 27
2$\overline{\text{CLR}}$ 28
2$\overline{\text{CLKEN}}$ 30
2CLK 29
2D1 42

R
CE
C1
1D

15 2Q1

One of Nine Channels

To Eight Other Channels
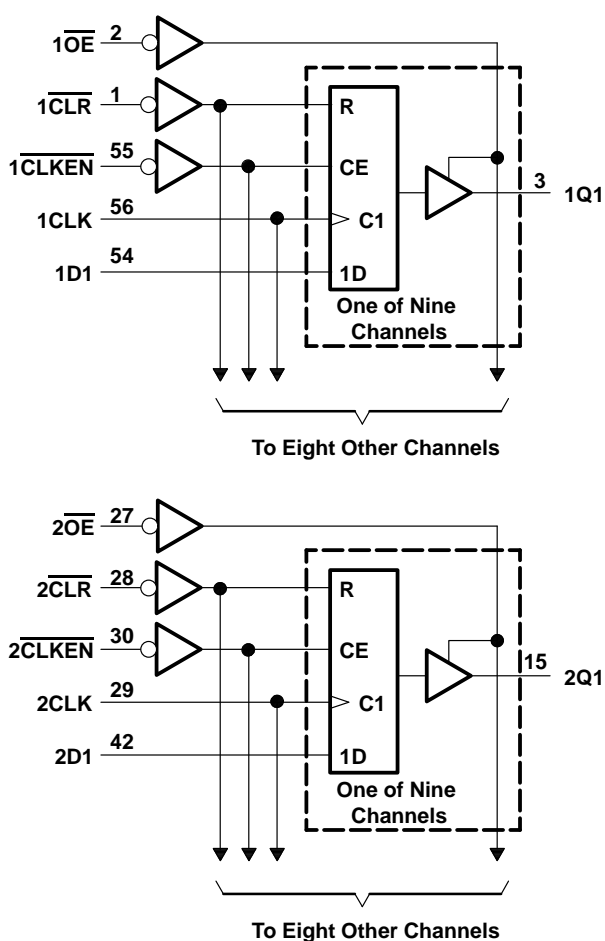
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air)(see Note 2): DL package .... 1.4 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2.   The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54AC16823			74AC16823			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3:   Unused inputs must be held high or low to prevent them from floating.

TEXAS INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	TA = 25°C			54AC16823		74AC16823		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
	$I_{OH} = -4\ mA$		3 V	2.58			2.48		2.48		
	$I_{OL} = -24\ mA$		4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75\ mA^†$		5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50\ \mu A$		3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12\ mA$		3 V			0.36		0.44		0.44	
	$I_{OL} = 24\ mA$		4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75\ mA^†$		5.5 V				1.65		1.65		
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1		μA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V		±0.5		±5		±5		μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V		8		80		80		μA
C_i	$V_I = V_{CC}$ or GND		5 V		3						pF
C_o	$V_O = V_{CC}$ or GND		5 V		11						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			TA = 25°C		54AC16823		74AC16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	60	0	60	0	60	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	8.4		8.4		8.4		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	0.5		0.5		0.5		ns
		Data	7.2		7.2		7.2		
		$\overline{CLKEN}$ low	5.8		5.8		5.8		
t_h	Hold time after CLK↑	Data	0		0		0		ns
		$\overline{CLKEN}$ high or low	1		1		1		

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timing requirements over recommended operating free-air temperature range,
V_{CC} **= 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)**

			T_A = 25°C		54AC16823		74AC16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	115	0	115	0	115	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	4.4		4.4		4.4		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	0.6		0.6		0.6		ns
		Data	5		5		5		
		$\overline{CLKEN}$ low	4.2		4.2		4.2		
t_h	Hold time after CLK↑	Data	1.3		1.3		1.3		ns
		$\overline{CLKEN}$ high or low	1.4		1.4		1.4		

switching characteristics over recommended operating free-air temperature range,
V_{CC} **= 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16823		74AC16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			60			60		60		MHz
t_{PLH}	CLK	Q	3.9	13.8	16.8	3.9	18.8	3.9	18.8	ns
t_{PHL}			4.7	14.5	17.3	4.7	18.9	4.7	18.9	
t_{PHL}	$\overline{CLR}$	Q	4	12.4	14.9	4	16.2	4	16.2	ns
t_{PZH}	$\overline{OE}$	Q	3	11.1	14	3	15.4	3	15.4	ns
t_{PZL}			4.3	15	18.7	4.3	20.8	4.3	20.8	
t_{PHZ}	$\overline{OE}$	Q	4.5	8.5	10.4	4.5	11.2	4.5	11.2	ns
t_{PLZ}			3.9	7.7	9.3	3.9	10.3	3.9	10.3	

switching characteristics over recommended operating free-air temperature range,
V_{CC} **= 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16823		74AC16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			115			115		115		MHz
t_{PLH}	CLK	Q	3.1	7.8	10.6	3.1	12	3.1	12	ns
t_{PHL}			3.9	8.6	11.4	3.9	12.7	3.9	12.7	
t_{PHL}	$\overline{CLR}$	Q	3.2	7.4	9.9	3.2	11	3.2	11	ns
t_{PZH}	$\overline{OE}$	Q	2.2	6.1	8.6	2.2	9.7	2.2	9.7	ns
t_{PZL}			3	7.4	10.6	3	11.8	3	11.8	
t_{PHZ}	$\overline{OE}$	Q	4.2	6.8	8.7	4.2	9.3	4.2	9.3	ns
t_{PLZ}			3.7	6.2	7.8	3.7	8.6	3.7	8.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	36	pF
	Outputs disabled		18	

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
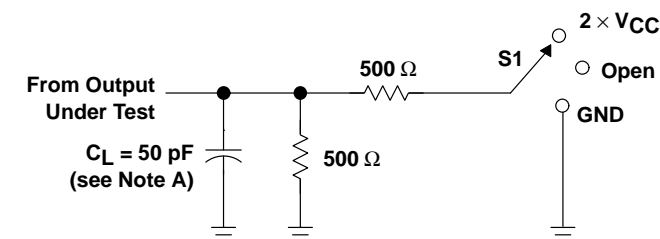
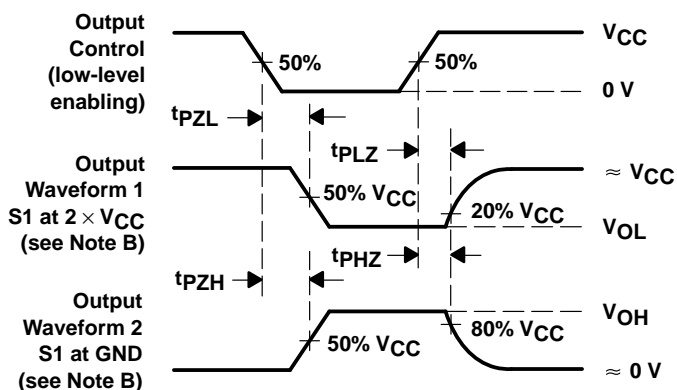| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
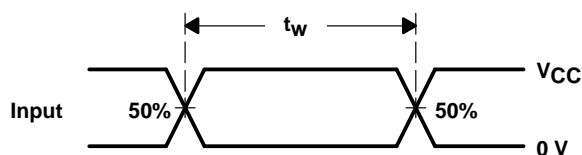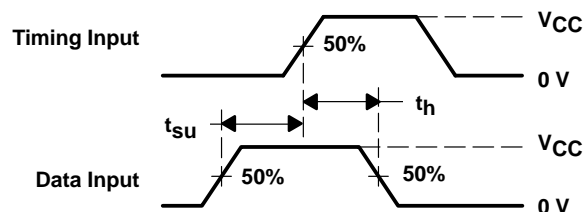
VOLTAGE WAVEFORMS
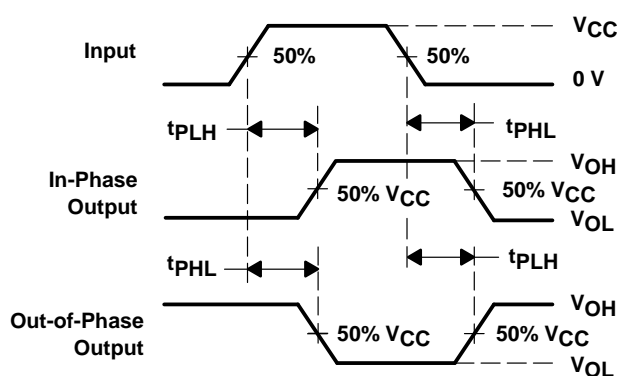
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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