- Members of the Texas Instruments
  Widebus™ Family

- 3-State Outputs Drive Bus Lines Directly

- Flow-Through Architecture Optimizes
  PCB Layout

- Distributed V_{CC} and GND Pin
  Configurations Minimize High-Speed
  Switching Noise

- *EPIC*™ (Enhanced-Performance Implanted
  CMOS) 1-μm Process

- 500-mA Typical Latch-Up Immunity at
  125°C

- Package Options Include Plastic 300-mil
  Shrink Small-Outline (DL) Packages Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Packages Using 25-mil Center-to-Center
  Pin Spacings

54AC16620 . . . WD PACKAGE
74AC16620 . . . DL PACKAGE
(TOP VIEW)

1OEAB	1	48	1$\overline{\text{OEBA}}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2OEAB	24	25	2$\overline{\text{OEBA}}$

description

The 'AC16620 are inverting 16-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.
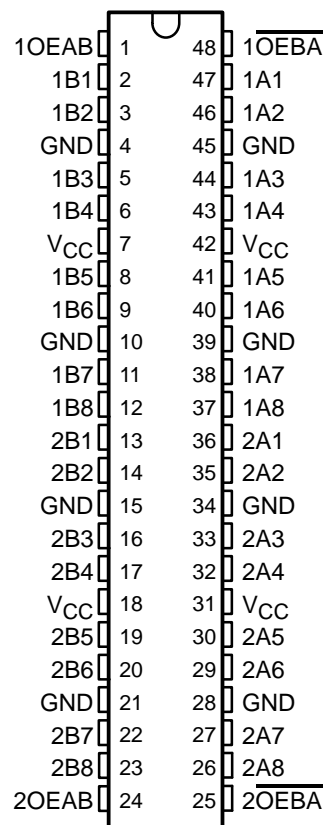
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the complementary output-enable (OEAB or $\overline{\text{OEBA}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the transceiver the capability to store data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74AC16620 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16620 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16620 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	$\overline{\text{B}}$ data to A bus
L	H	$\overline{\text{B}}$ data to A bus, $\overline{\text{A}}$ data to B bus
H	L	Isolation
H	H	$\overline{\text{A}}$ data to B bus

logic symbol[†]
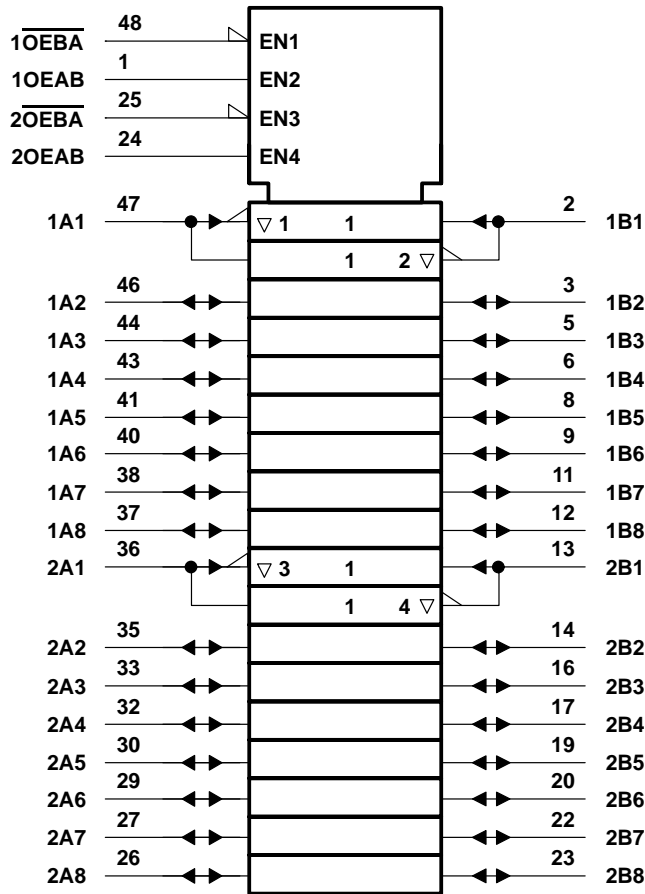
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
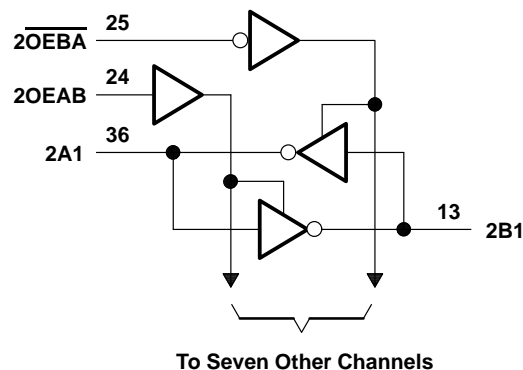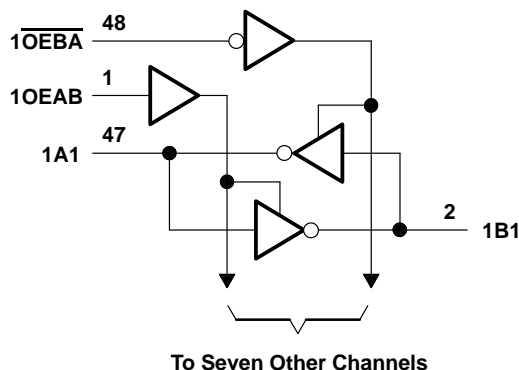
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.2 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 2)

			54AC16620			74AC16620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4			–4	mA
		V_{CC} = 4.5 V			–24			–24	
		V_{CC} = 5.5 V			–24			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16620		74AC16620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80		80	µA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

TEXAS
INSTRUMENTS

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16620		74AC16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.7	6.1	8.7	2.7	9.7	2.7	9.7	ns
t_{PHL}			3.9	7.9	10.6	3.9	11.7	3.9	11.7	
t_{PZH}	$\overline{OEBA}$	A	3.2	7.1	10	3.2	11.2	3.2	11.2	ns
t_{PZL}			4.5	11.1	13.5	4.5	15	4.5	15	
t_{PHZ}	$\overline{OEBA}$	A	5.3	7.4	9.5	5.3	10.2	5.3	10.2	ns
t_{PLZ}			4.6	7	9.2	4.6	9.8	4.6	9.8	
t_{PZH}	OEAB	B	3.1	6.7	9.5	3.1	10.7	3.1	10.7	ns
t_{PZL}			4.4	9.6	13	4.4	14.5	4.4	14.5	
t_{PHZ}	OEAB	B	5	7.1	9.3	5	9.8	5	9.8	ns
t_{PLZ}			4.4	6.8	8.9	4.4	9.4	4.4	9.4	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

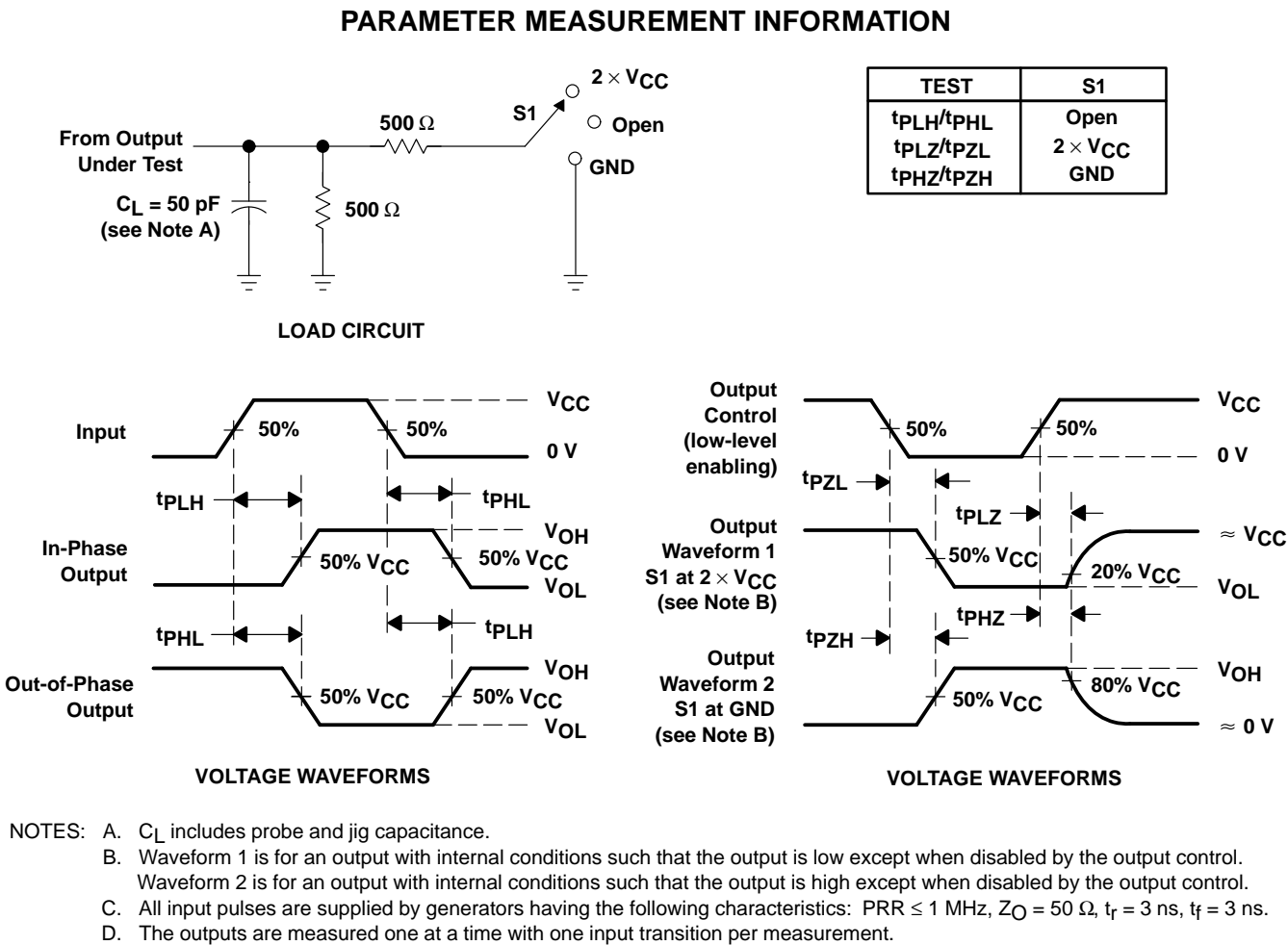| PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16620		74AC16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.1	3.9	6.1	2.1	6.8	2.1	6.8	ns
t_{PHL}			3.1	4.9	7.3	3.1	8.2	3.1	8.2	
t_{PZH}	$\overline{OEBA}$	A	2.2	4.3	6.8	2.2	7.6	2.2	7.6	ns
t_{PZL}			3.3	5.5	8.4	3.3	9.4	3.3	9.4	
t_{PHZ}	$\overline{OEBA}$	A	4.9	6.6	8.6	4.9	9.2	4.9	9.2	ns
t_{PLZ}			4.1	5.8	7.8	4.1	8.3	4.1	8.3	
t_{PZH}	OEAB	B	2.2	4.2	6.5	2.2	7.3	2.2	7.3	ns
t_{PZL}			3.4	5.4	8.1	3.4	9.1	3.4	9.1	
t_{PHZ}	OEAB	B	4.6	6.4	8.5	4.6	9	4.6	9	ns
t_{PLZ}			4.1	5.6	7.6	4.1	8	4.1	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	49	pF
	Outputs disabled		6	

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.