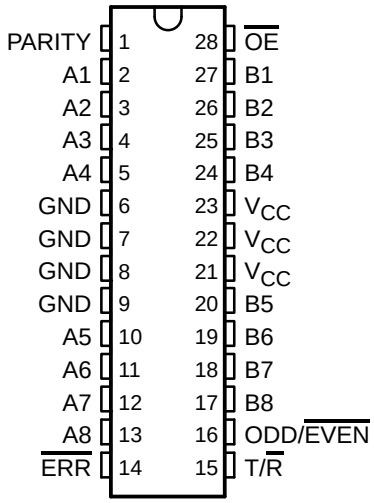
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin $V_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW PACKAGE**
**(TOP VIEW)**




## description

The 74ACT11657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker and is intended for bus-oriented applications.

The transmit/receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data flows from the A port to the B port (transmit mode); when T/$\overline{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the ODD/$\overline{EVEN}$ input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/$\overline{EVEN}$ input. For example, if ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the $\overline{ERR}$ output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/$\overline{EVEN}$ is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then $\overline{ERR}$ is low, indicating a parity error.

The 74ACT11657 is characterized for operation from –40°C to 85°C.

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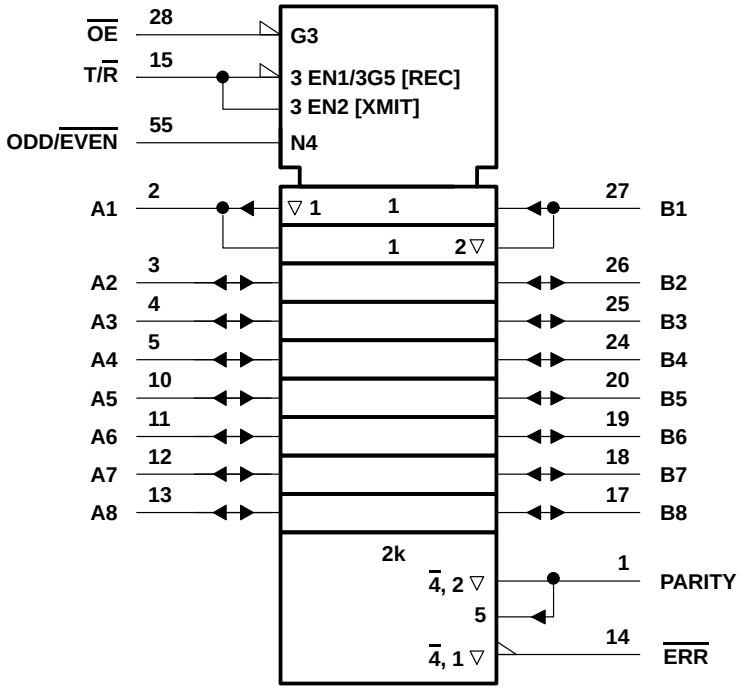
**FUNCTION TABLE**

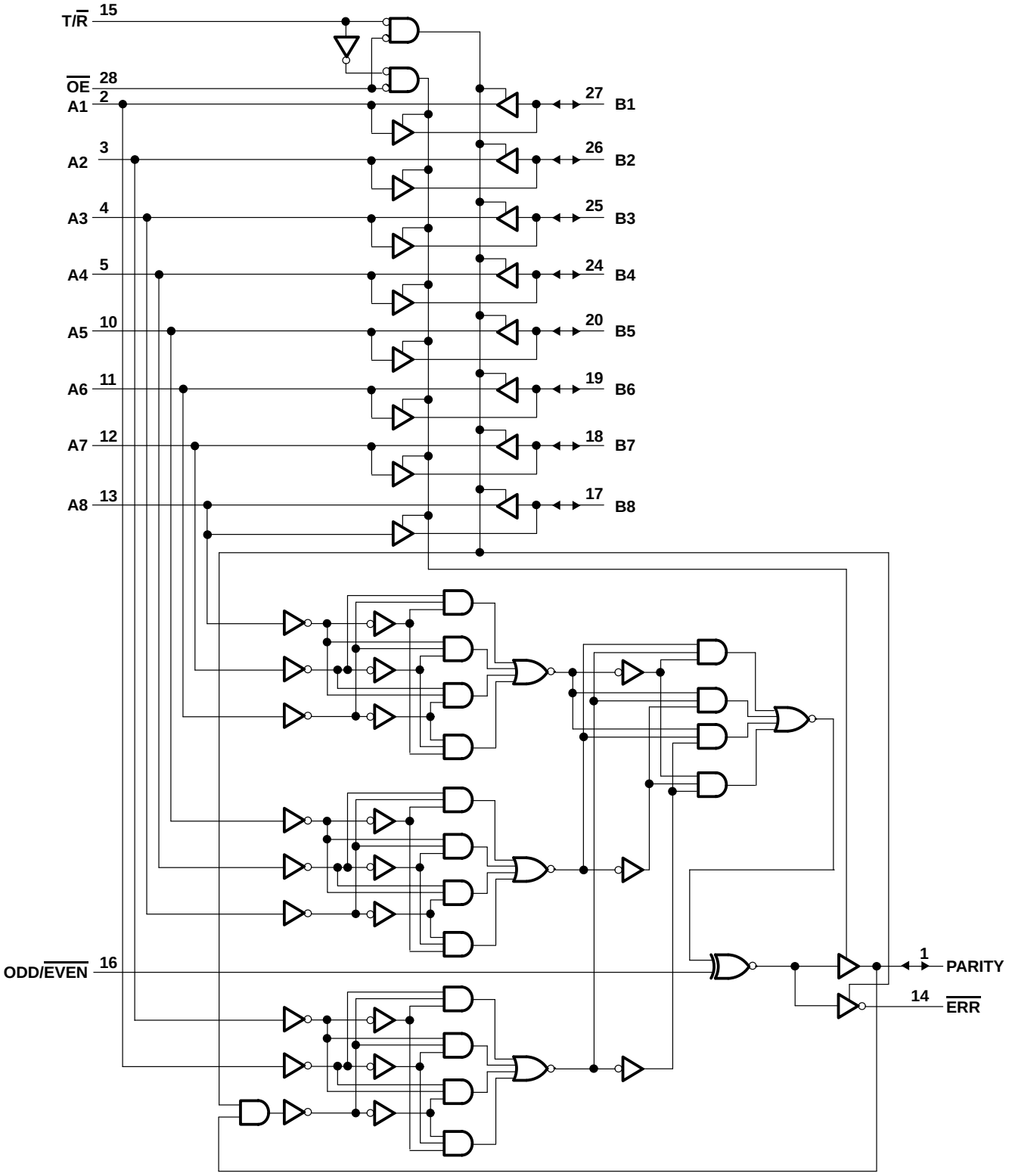
| NUMBER OF A OR B INPUTS THAT ARE HIGH | INPUTS | | | INPUT/OUTPUT PARITY | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{OE}$ | T/$\overline{R}$ | ODD/$\overline{EVEN}$ | | $\overline{ERR}$ | OUTPUT MODE |
| 0, 2, 4, 6, 8 | L | H | H | H | Z | Transmit |
| | L | H | L | L | Z | Transmit |
| | L | L | H | H | H | Receive |
| | L | L | H | L | L | Receive |
| | L | L | L | H | L | Receive |
| | L | L | L | L | H | Receive |
| 1, 3, 5, 7 | L | H | H | L | Z | Transmit |
| | L | H | L | H | Z | Transmit |
| | L | L | H | H | L | Receive |
| | L | L | H | L | H | Receive |
| | L | L | L | H | H | Receive |
| | L | L | L | L | L | Receive |
| Don't care | H | X | X | Z | Z | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±225 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = – 50 μA | 4.5 V | 4.4 | | | 4.4 | | V |
| | | | 5.5 V | 5.4 | | | 5.4 | | |
| | | $I_{OH}$ = – 24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | | 5.5 V | 4.94 | | | 4.8 | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 μA | 4.5 V | | | 0.1 | | 0.1 | V |
| | | | 5.5 V | | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.44 | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | 1.65 | |
| $I_I$ | A or B ports | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | μA |
| $I_{OZ}$‡ | Control Inputs | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 80 | μA |
| $\Delta I_{CC}$§ | | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 0.9 | | 1 | mA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | | | | pF |
| $C_o$ | PARITY/$\overline{ERR}$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 10 | | | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | 5 V | | 12 | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

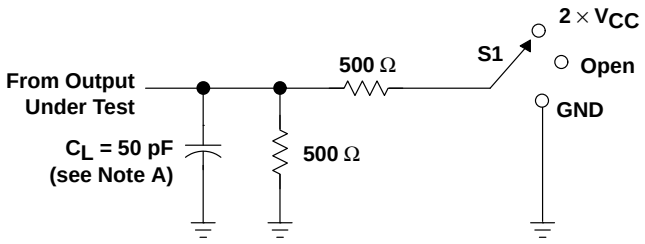
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 2.9 | 6.7 | 8.4 | 2.9 | 9.4 | ns |
| $t_{PHL}$ | | | 2.2 | 7 | 8.4 | 2.2 | 9.4 | |
| $t_{PLH}$ | A | PARITY | 3.4 | 10.4 | 12.7 | 3.4 | 14.4 | ns |
| $t_{PHL}$ | | | 3.9 | 10.9 | 13.2 | 3.9 | 15 | |
| $t_{PLH}$ | ODD/$\overline{EVEN}$ | PARITY, $\overline{ERR}$ | 2.5 | 7.9 | 9.4 | 2.5 | 10.7 | ns |
| $t_{PHL}$ | | | 3 | 8.5 | 10 | 3 | 11.3 | |
| $t_{PLH}$ | B | $\overline{ERR}$ | 4.6 | 18.1 | 20.6 | 4.6 | 23.6 | ns |
| $t_{PHL}$ | | | 4.9 | 18.5 | 21.8 | 4.9 | 24.6 | |
| $t_{PLH}$ | PARITY | $\overline{ERR}$ | 4 | 10.9 | 12.8 | 4 | 14.6 | ns |
| $t_{PHL}$ | | | 3.9 | 11 | 12.9 | 3.9 | 14.7 | |
| $t_{PZH}$ | $\overline{OE}$ | A, B, PARITY, or $\overline{ERR}$ | 2.6 | 9.1 | 10.8 | 2.6 | 12.1 | ns |
| $t_{PZL}$ | | | 3.1 | 10.6 | 12.3 | 3.1 | 13.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | A, B, PARITY, or $\overline{ERR}$ | 4.5 | 9.1 | 10.8 | 4.5 | 12.1 | ns |
| $t_{PLZ}$ | | | 4.5 | 8.7 | 10.5 | 4.5 | 11.6 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

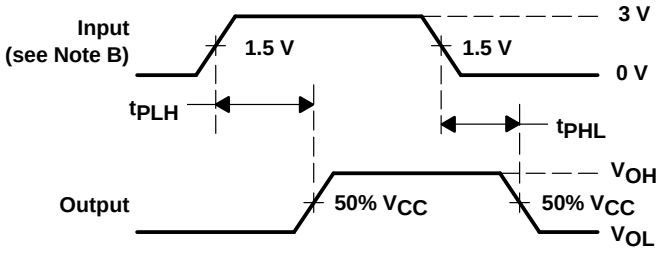
| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 50 pF, f = 1 MHz | 95 | pF |
| | | Outputs disabled | | 21 | |

## PARAMETER MEASUREMENT INFORMATION

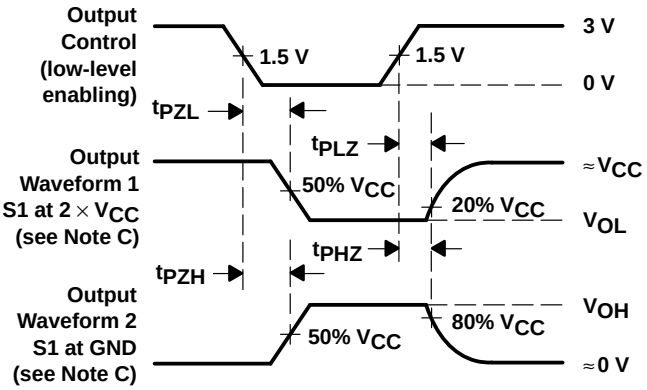



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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