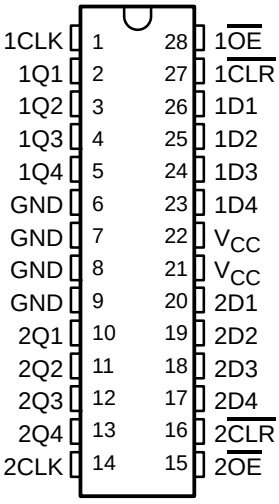
- **Inputs Are TTL-Voltage Compatible**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Asynchronous Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11874 contains dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes this device particularly suitable for implementing buffer registers, I/O ports, and working registers.

The D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 74ACT11874 has $\overline{CLR}$ inputs and noninverting outputs. Taking $\overline{CLR}$ low causes the four Q outputs to go low independently of the clock.

The 74ACT11874 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

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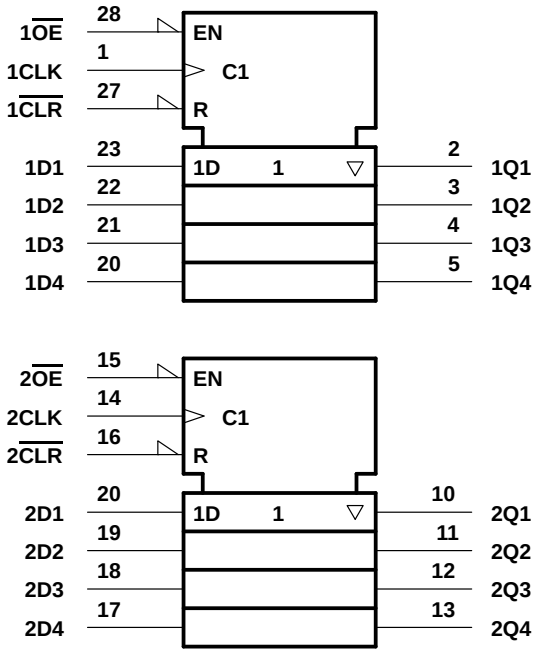
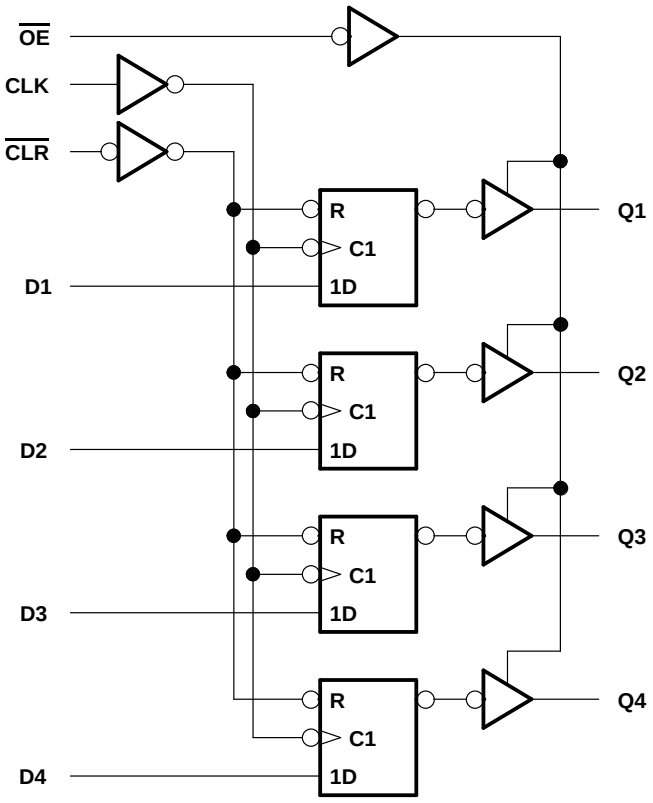
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each 4-bits) (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{clock}	Clock frequency		0		125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low		2		4		ns
		CLK high or low		2		4		
t_{su}	Setup time before CLK↑	Data		1		5		ns
		$\overline{CLR}$ low		2		2		
t_h	Hold time after CLK↑	Data		2		1		ns

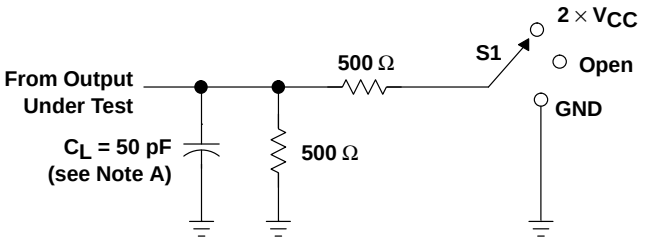
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	CLK	Any Q		7.5		3.7	9.4	ns
t_{PHL}				8.1		4.1	10.6	
t_{PHL}	$\overline{CLR}$	Any Q		8.8		3.5	11.8	ns
t_{PZH}	$\overline{OE}$	Any Q		6.4		1.6	7.4	ns
t_{PZL}				8.6		2.4	9.5	
t_{PHZ}	$\overline{OE}$	Any Q		6.9		5.4	9.4	ns
t_{PLZ}				6.8		4.9	9.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

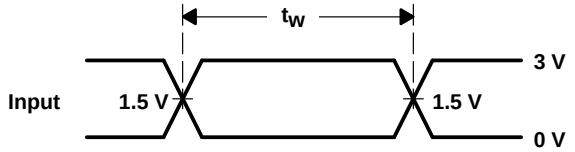
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	76	pF
		Outputs disabled		64	

PARAMETER MEASUREMENT INFORMATION

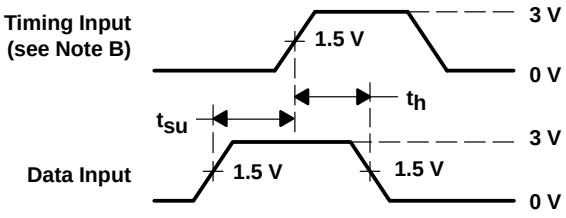


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



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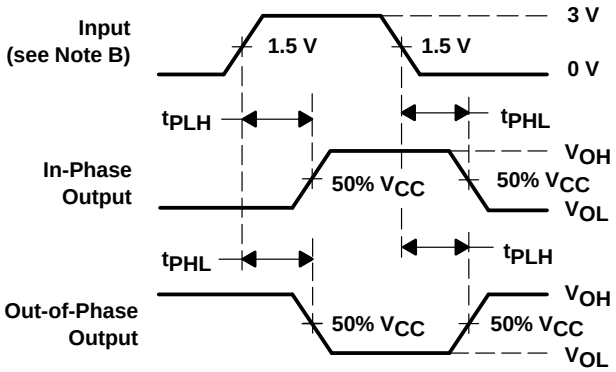
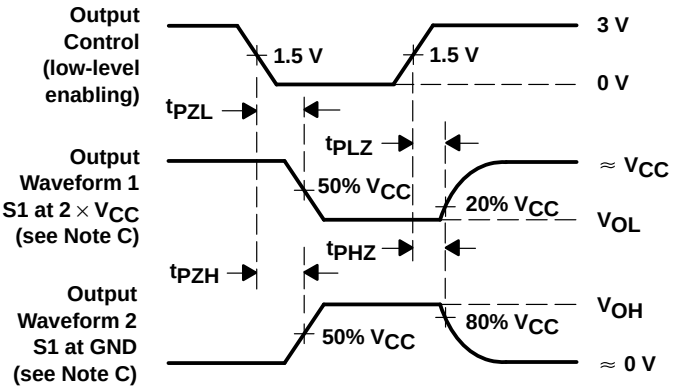


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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