- **Members of the Texas Instruments**
  ***Widebus*™ Family**

- **Inputs Are TTL-Voltage Compatible**

- **Flow-Through Architecture Optimizes**
  PCB Layout

- **Distributed V_{CC} and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- ***EPIC*™ (Enhanced-Performance Implanted**
  CMOS) 1-μm Process

- **500-mA Typical Latch-Up Immunity at**
  125°C

- **Package Options Include Plastic 300-mil**
  Shrink Small-Outline (DL) Packages Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Packages Using 25-mil Center-to-Center
  Pin Spacings

54ACT16541 . . . WD PACKAGE
74ACT16541 . . . DL PACKAGE
(TOP VIEW)

|			
$\overline{1OE1}$	1	48	$\overline{1OE2}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
$\overline{2OE1}$	24	25	$\overline{2OE2}$

description

The 'ACT16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The 74ACT16541 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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logic symbol†

	Pin		
1$\overline{\text{OE1}}$	1	&	EN1
1$\overline{\text{OE2}}$	48		
2$\overline{\text{OE1}}$	24	&	EN2
2$\overline{\text{OE2}}$	25		

Input	Pin		Pin	Output
1A1	47	1 1 ▽	2	1Y1
1A2	46		3	1Y2
1A3	44		5	1Y3
1A4	43		6	1Y4
1A5	41		8	1Y5
1A6	40		9	1Y6
1A7	38		11	1Y7
1A8	37		12	1Y8
2A1	36	1 2 ▽	13	2Y1
2A2	35		14	2Y2
2A3	33		16	2Y3
2A4	32		17	2Y4
2A5	30		19	2Y5
2A6	29		20	2Y6
2A7	27		22	2Y7
2A8	26		23	2Y8
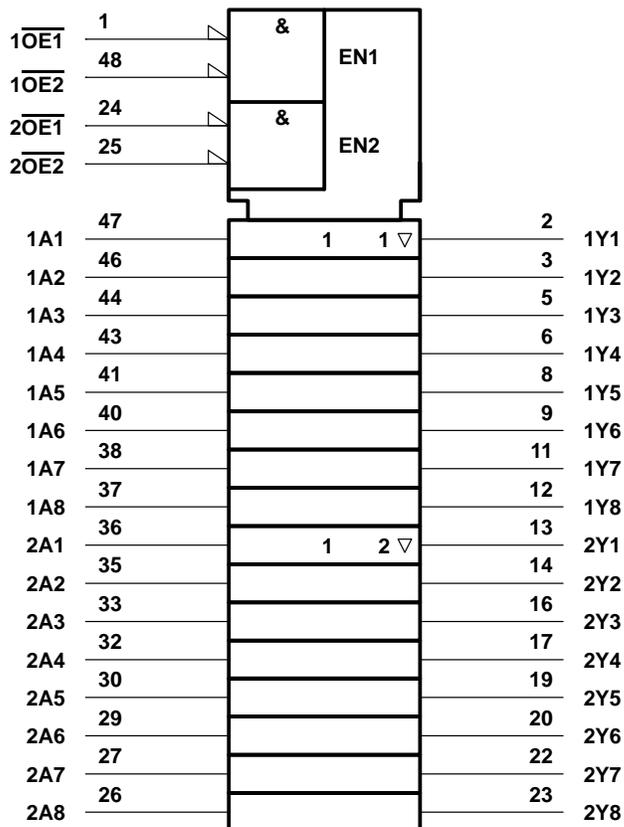
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
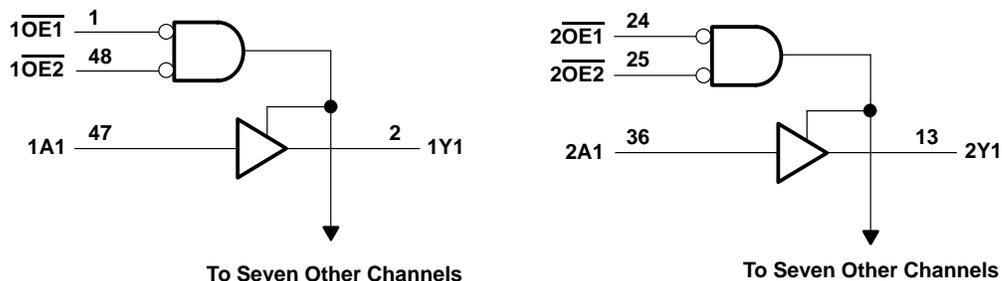
To Seven Other Channels

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . 1.2 W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
          2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16541			74ACT16541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16541		74ACT16541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ mA$	5.5 V	3.9			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75\ mA†$	5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ mA$	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75\ mA†$	5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μA
$\Delta I_{CC}‡$	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5.5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16541		74ACT16541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.1	5.9	7.9	3.1	9	3.1	9	ns
t_{PHL}			2.7	6.3	8.3	2.7	9.2	2.7	9.2	
t_{PZH}	$\overline{OE}$	Y	2.8	6.5	8.9	2.8	9.7	2.8	9.7	ns
t_{PZL}			3.5	7.5	9.9	3.5	11	3.5	11	
t_{PHZ}	$\overline{OE}$	Y	4.5	8.5	10.3	4.5	11.3	4.5	11.3	ns
t_{PLZ}			4.9	8	9.9	4.9	10.7	4.9	10.7	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver		Outputs enabled	$C_L = 50\ pF,$ $f = 1\ MHz$	40	pF
		Outputs disabled		9.5	

![Texas Instruments logo]

PARAMETER MEASUREMENT INFORMATION
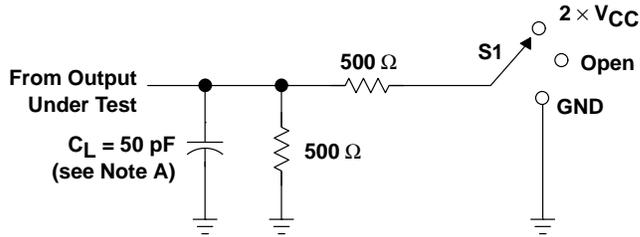
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND
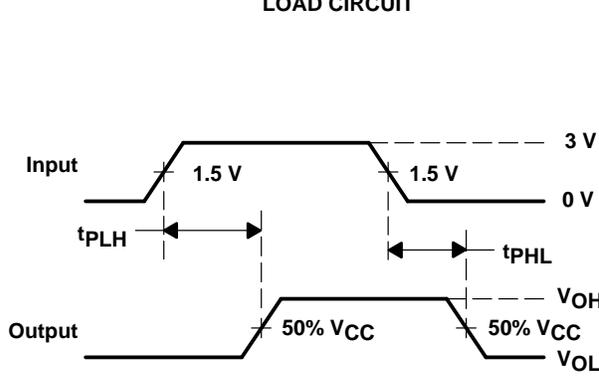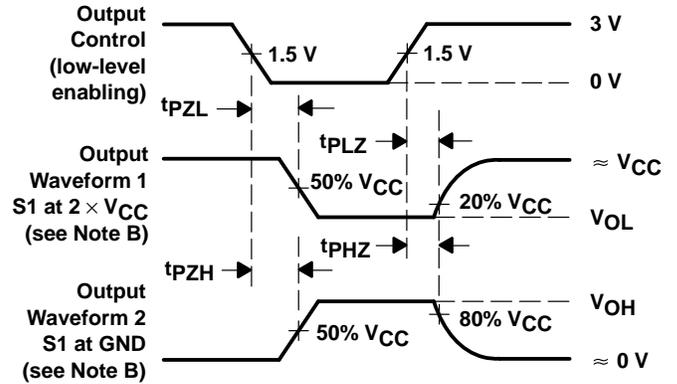
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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