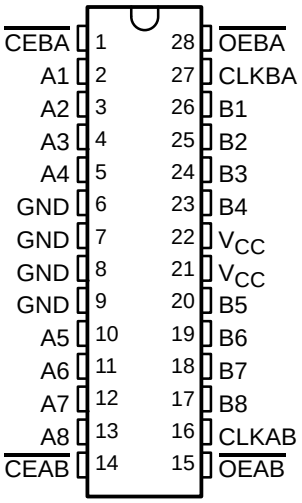
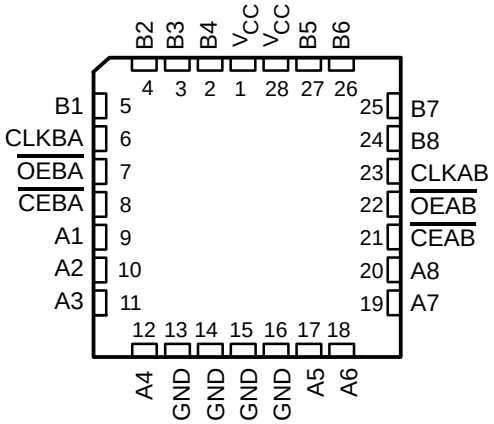
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

54ACT11470 . . . JT PACKAGE
74ACT11470 . . . DW PACKAGE
(TOP VIEW)



54AC11470 . . . FK PACKAGE
(TOP VIEW)



description

The ′ACT11470 is an 8-bit registered bus transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Separate clock (CLKAB or CLKBA) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data to B. If both $\overline{\text{CEAB}}$ and CLKAB are low, then the B port presents the level of the A port prior to the most recent low-to-high transition of CLKAB. Data flow from B to A is similar, but requires the use of $\overline{\text{CEBA}}$, CLKBA, and $\overline{\text{OEBA}}$ inputs.

To avoid false clocking of the flip-flops, $\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$ should not be switched from low to high while CLK is low.

The 54ACT11470 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11470 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CEAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{CEBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

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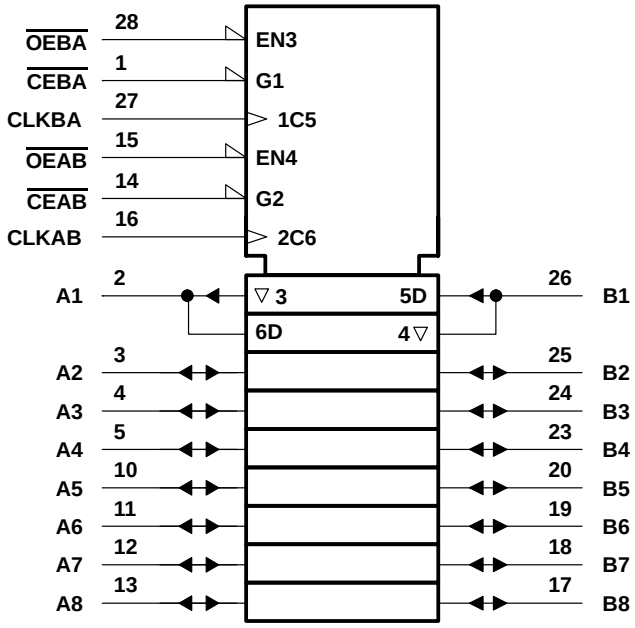
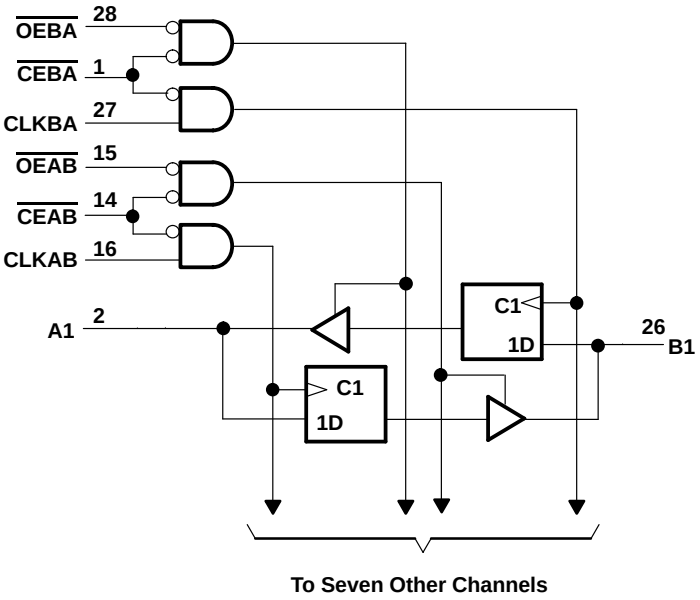
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT11470			74ACT11470			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11470		74ACT11470		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT11470		74ACT11470		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	CLK high or low	5.5		5.5		5.5		ns
t_{su}	Setup time	Data before CLK↑	2		2		2		ns
		Data before $\overline{CEAB}$↑ or $\overline{CEBA}$↑	2		2		2		
t_h	Hold time	Data after CLK↑	3		3		3		ns
		Data after $\overline{CEAB}$↑ or $\overline{CEBA}$↑	3		3		3		

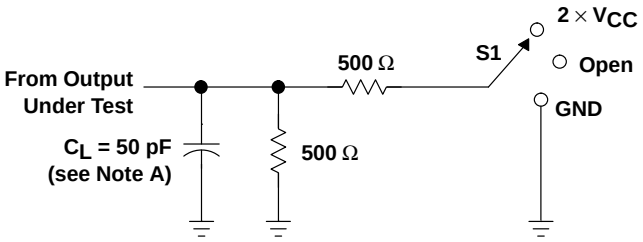
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11470		74ACT11470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	CLKAB or CLKBA	A or B	3.4	7.3	9	3.4	10.7	3.4	10.1	ns
t_{PHL}			4.2	8.3	10.2	4.2	12	4.2	11.4	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	3	7	9.5	3	11.5	3	10.5	ns
t_{PZL}			4.3	8.6	11.4	4.3	15	4.3	13.7	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	4.5	7.9	9.6	4.5	11	4.5	10.5	ns
t_{PLZ}			5.1	7.7	9.5	5.1	10.7	5.1	10.2	
t_{PZH}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	3.4	7.3	10	3.4	12	3.4	11.1	ns
t_{PZL}			4.6	9	11.9	4.6	15.5	4.6	14.2	
t_{PHZ}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	4.8	7.9	9.9	4.8	11.4	4.8	10.9	ns
t_{PLZ}			5.1	7.9	9.8	5.1	11.2	5.1	10.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

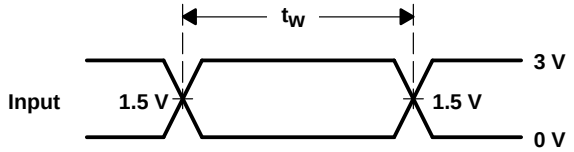
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		27	

PARAMETER MEASUREMENT INFORMATION

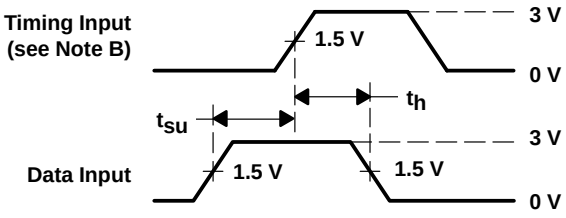


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



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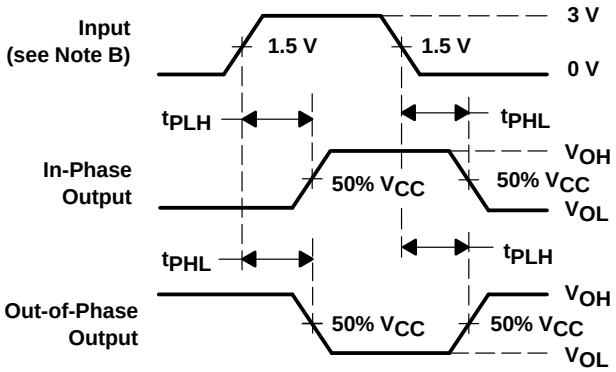
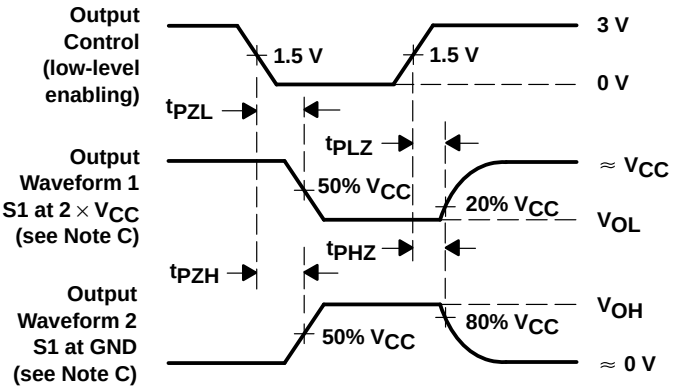


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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