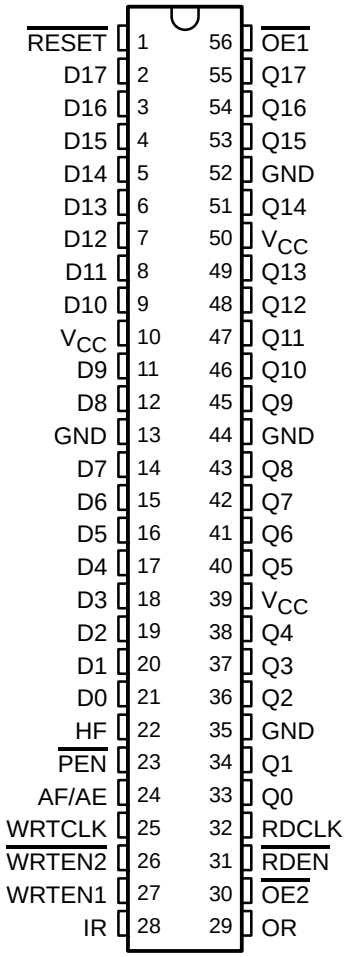
SCAS201 – MARCH 1991 – REVISED APRIL 1992

- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7803 and SN74ACT7813**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

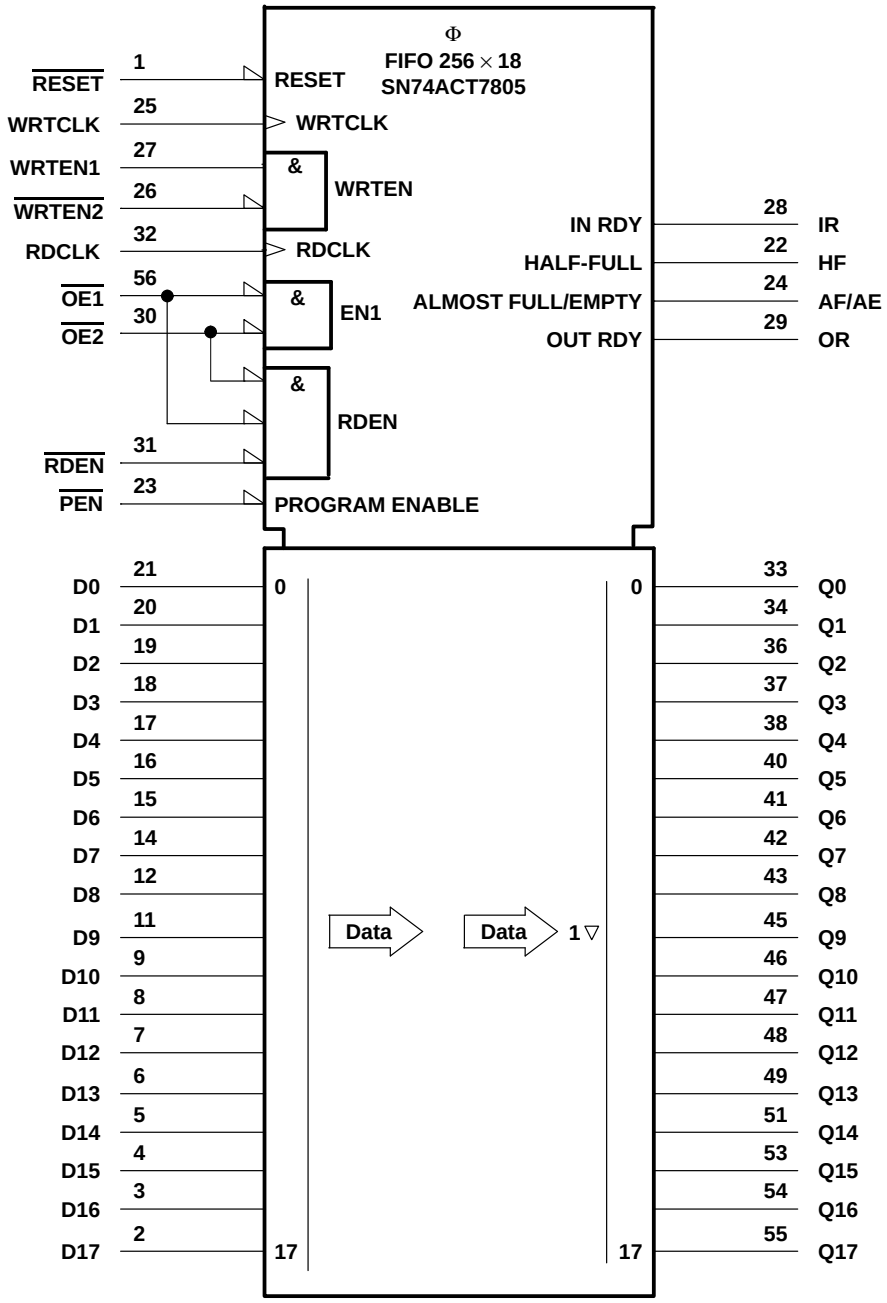
The SN74ACT7805 is a 256-word × 18-bit clocked FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented Output Edge Control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

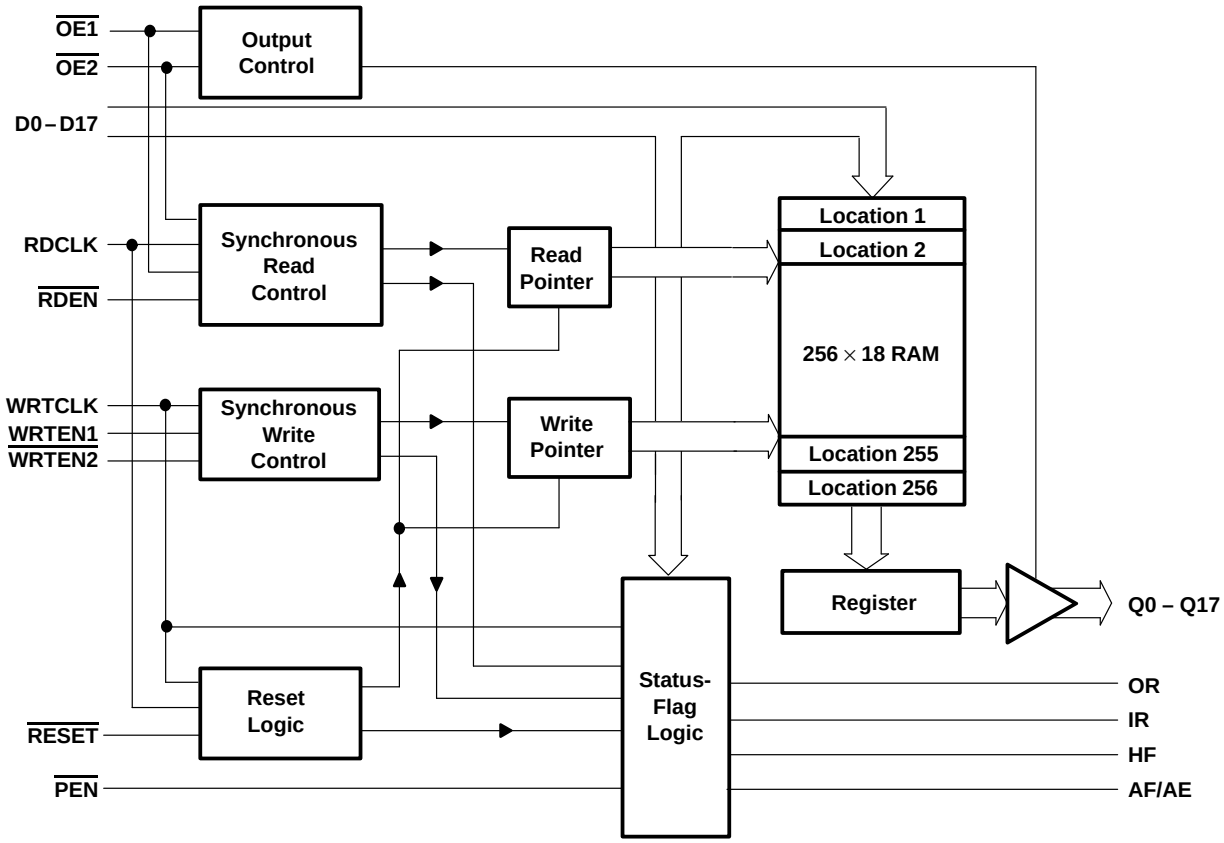
The SN74ACT7805 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{OE1}$, $\overline{OE2}$	56, 30	I	Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{PEN}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{RDEN}$	31	I	Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{RESET}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{WRTEN2}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

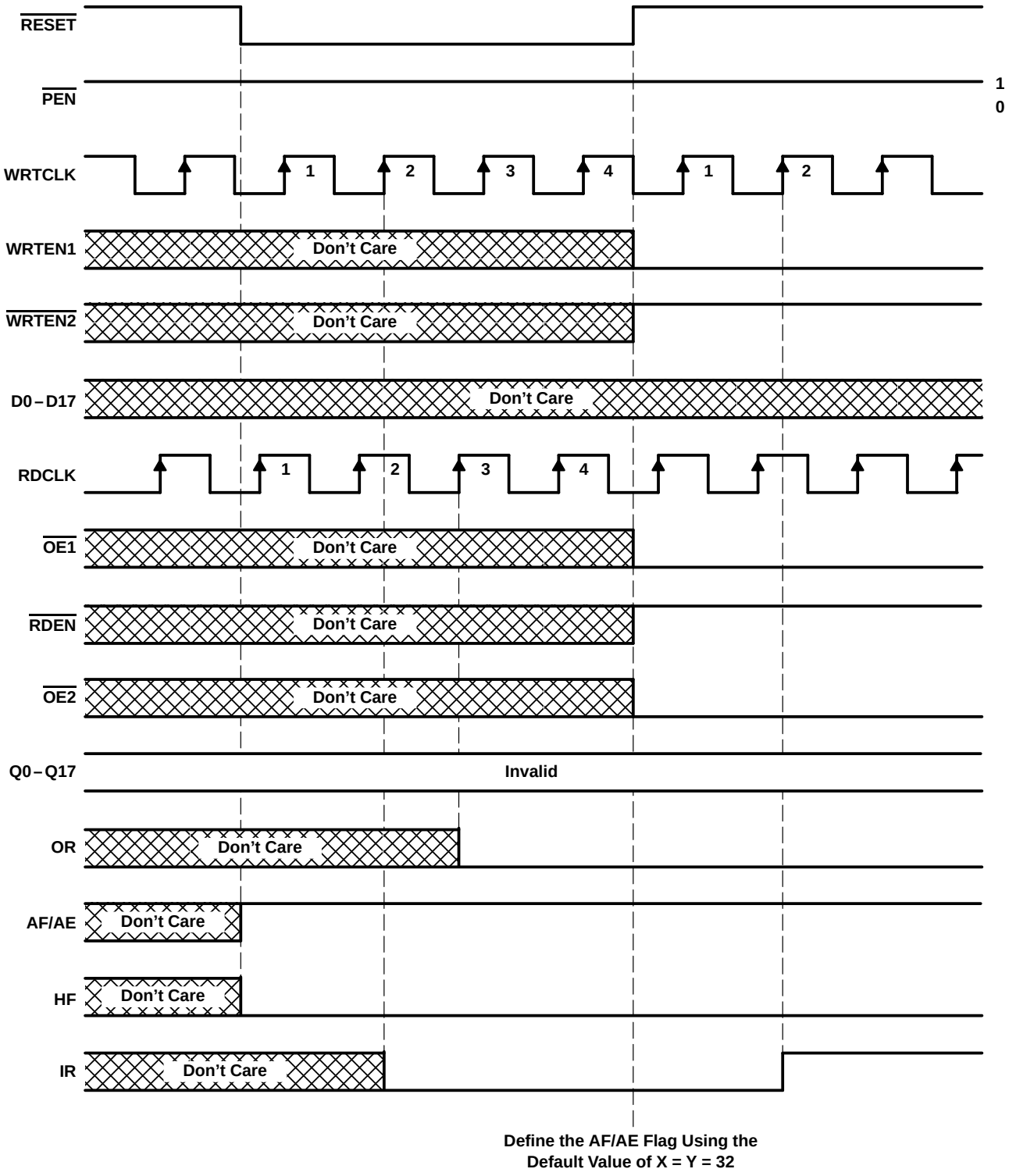


Figure 1. Reset Cycle

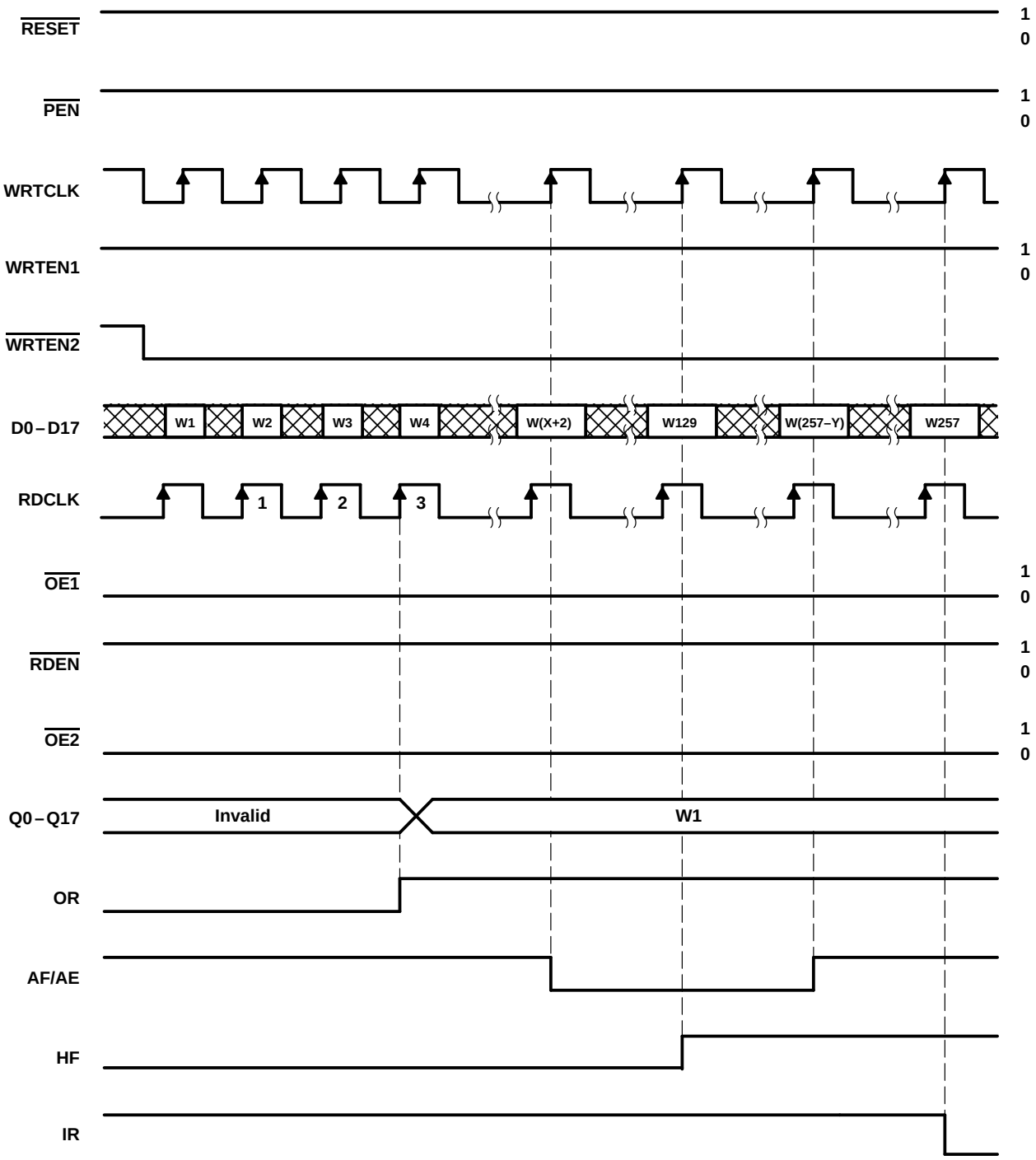


Figure 2. Write

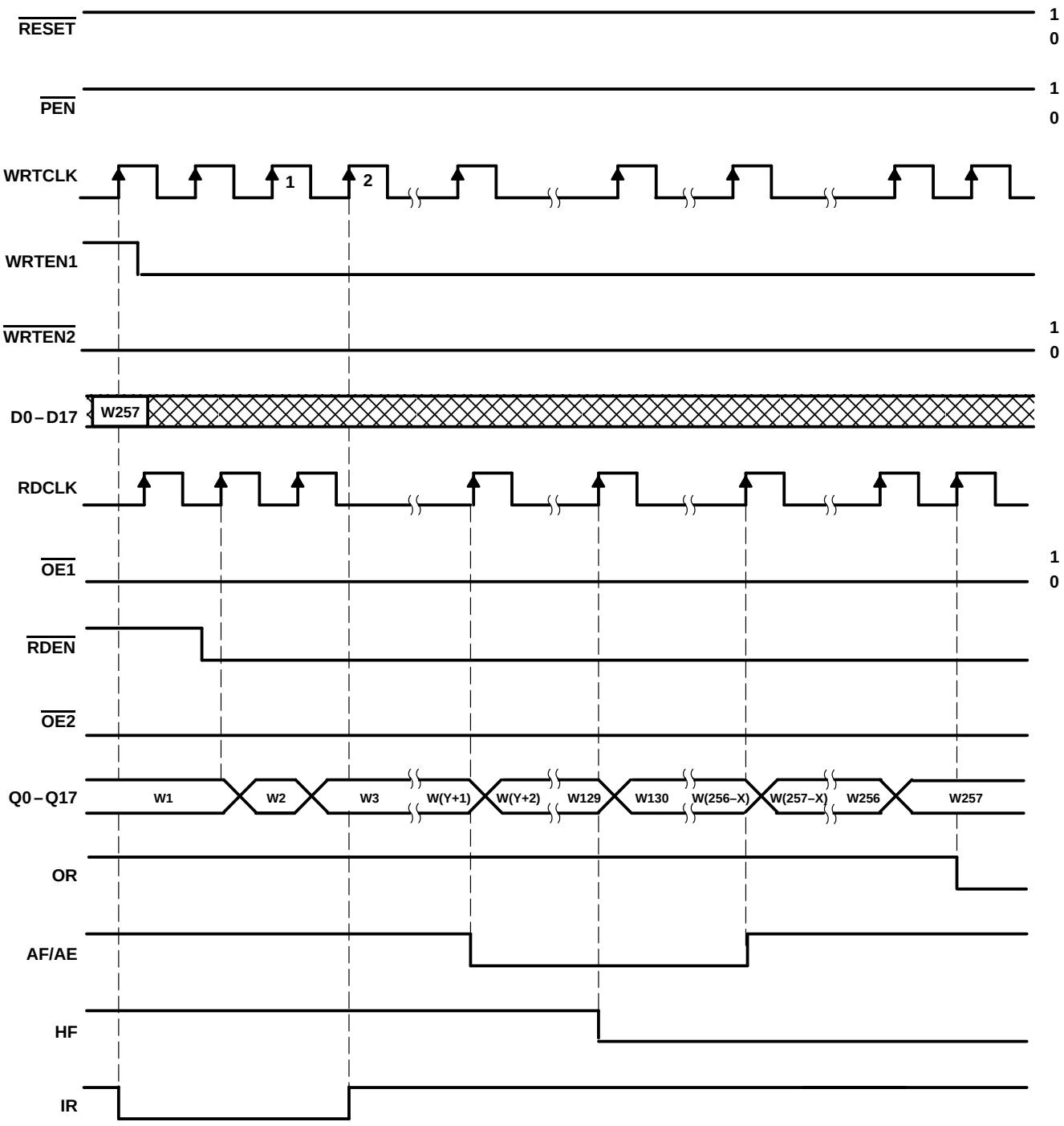


Figure 3. Read

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 32 are used. The AF/AE flag is high when the FIFO contains X or less words or (256 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D6 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 127 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 32, $\overline{PEN}$ must be held high.

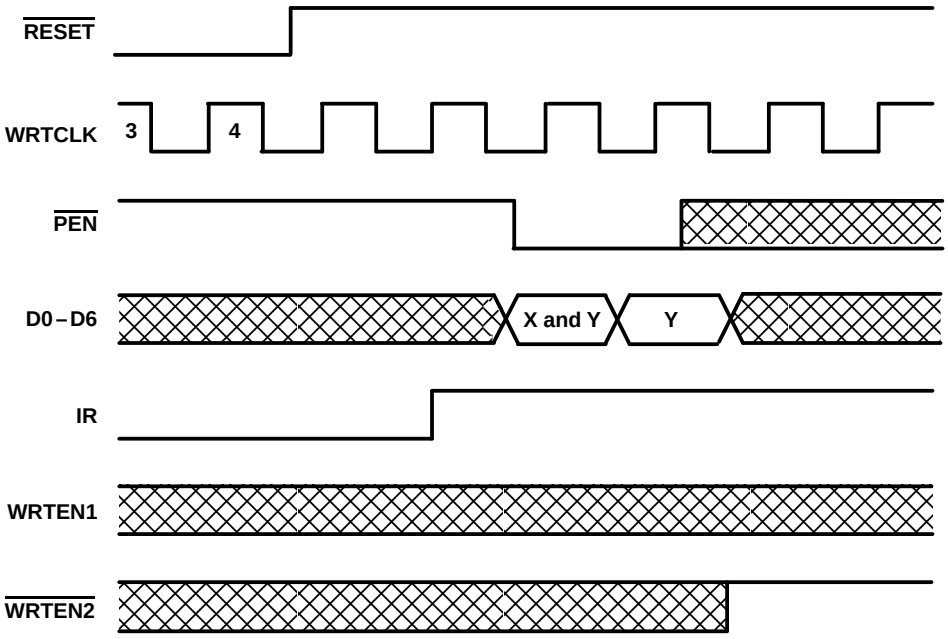


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			′ACT7805-15		′ACT7805-20		′ACT7805-25		′ACT7805-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{PEN}$ low	8		9		9		12		
t_{su}	Setup time	D0−D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑	4		5		5		5		
		$\overline{OE1}$, $\overline{OE2}$ before RDCLK↑	5		5		6		6		
		$\overline{RDEN}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		6		6		
		$\overline{PEN}$ before WRTCLK↑	5		6		6		6		
		Define AF/AE: $\overline{PEN}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0−D17) after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑	0		0		0		0		
		$\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		2		
		Define AF/AE: $\overline{PEN}$ after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	′ACT7805-15			′ACT7805-20		′ACT7805-25		′ACT7805-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
	RDCLK↑		7		17	7	19	7	21	7	23	
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF,	f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

**PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE**

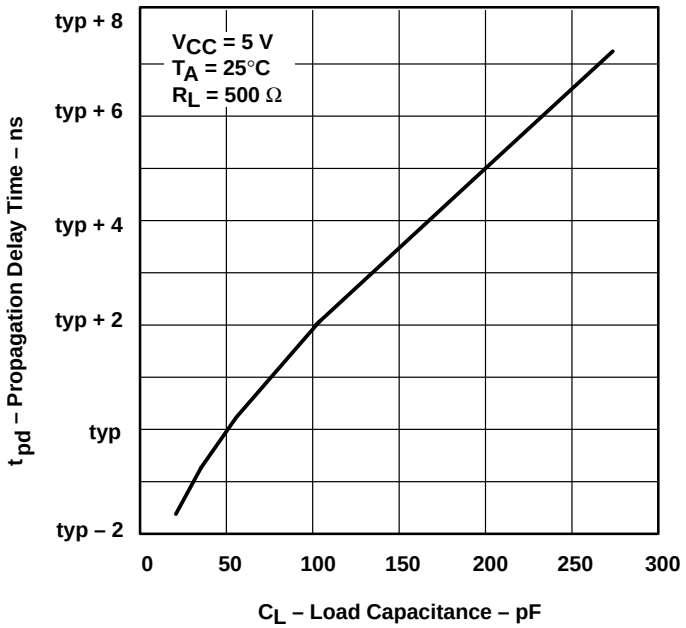


Figure 5

**SUPPLY CURRENT
vs
CLOCK FREQUENCY**

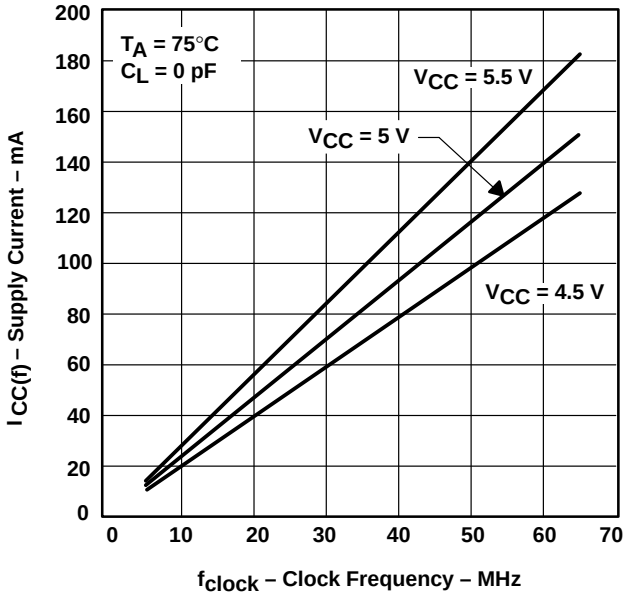


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

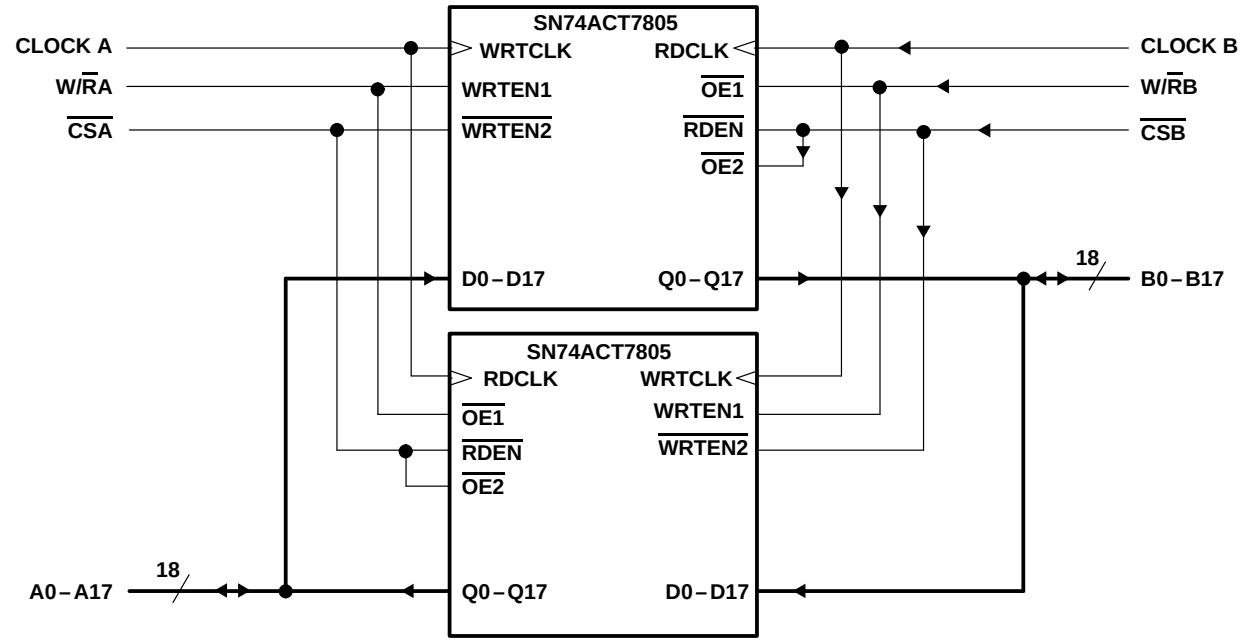


Figure 7. Bidirectional Configuration

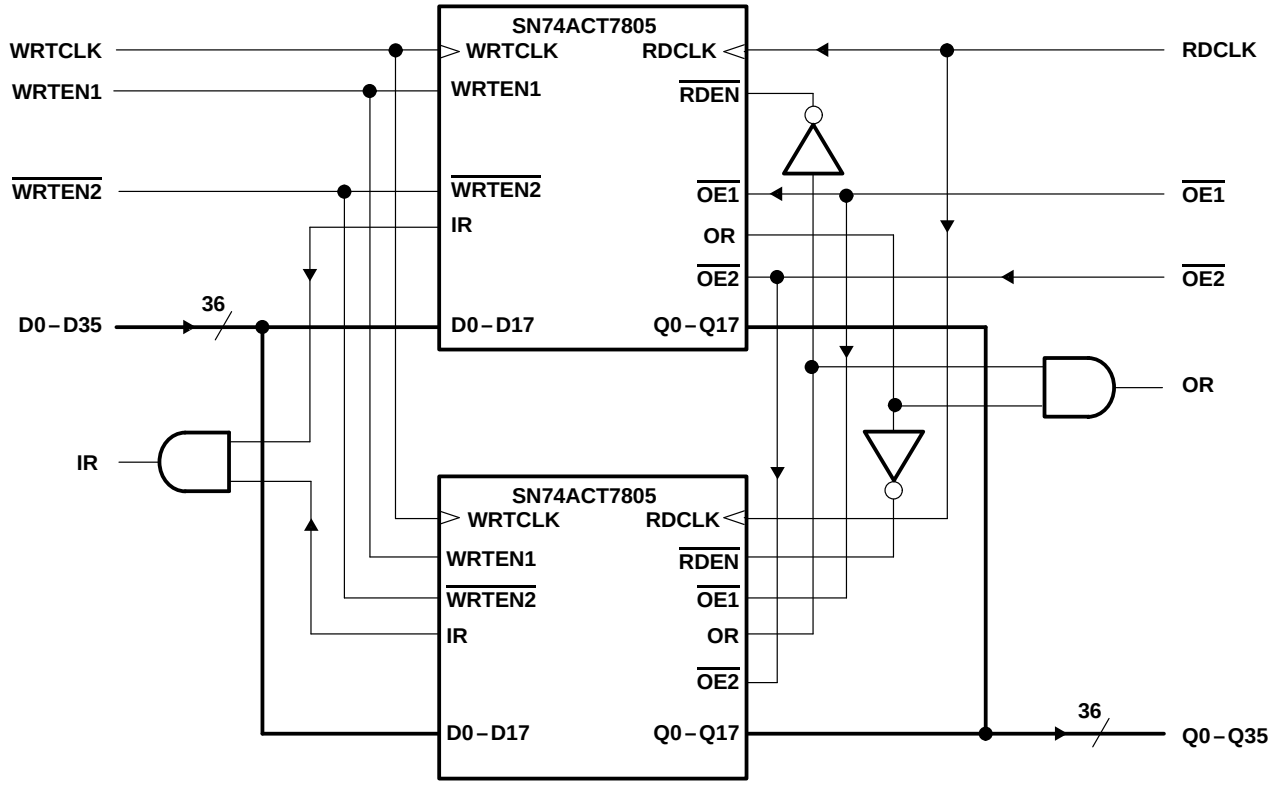


Figure 8. Word-Width Expansion: 256 × 36 Bits

PARAMETER MEASUREMENT INFORMATION

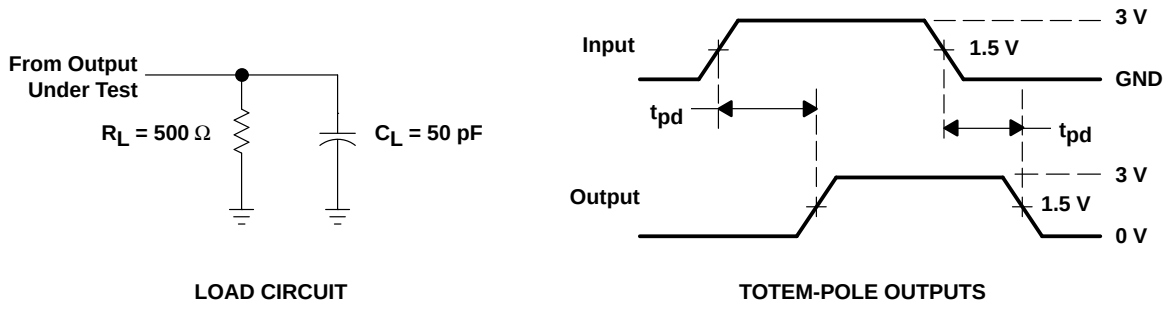
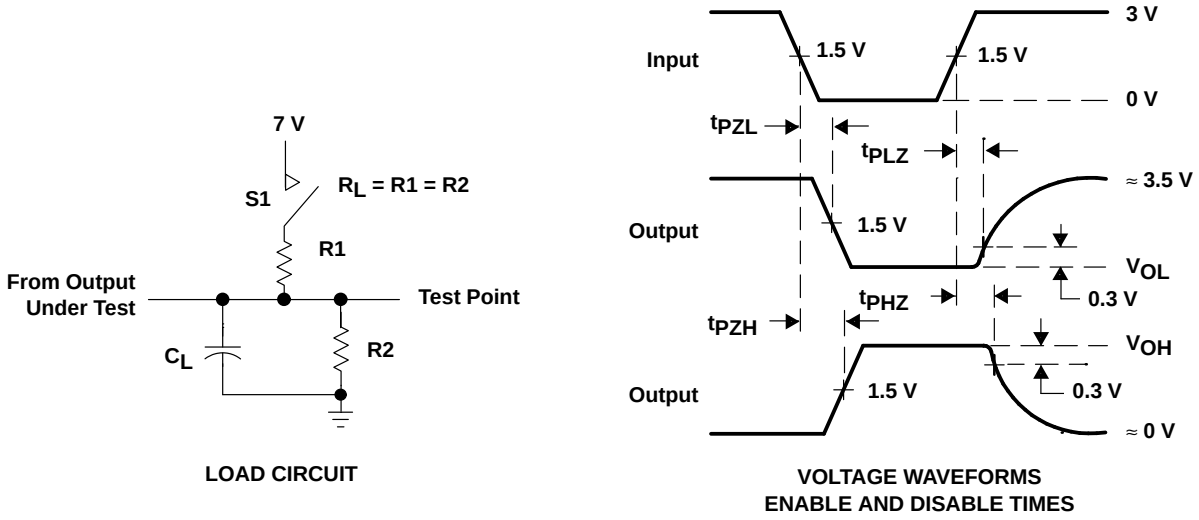


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 10. 3-State Outputs (Any Q)

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