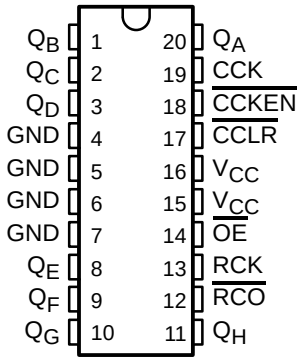
- **Inputs Are TTL-Voltage Compatible**
- **Parallel Registered Outputs**
- **Internal Counters Have Direct Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

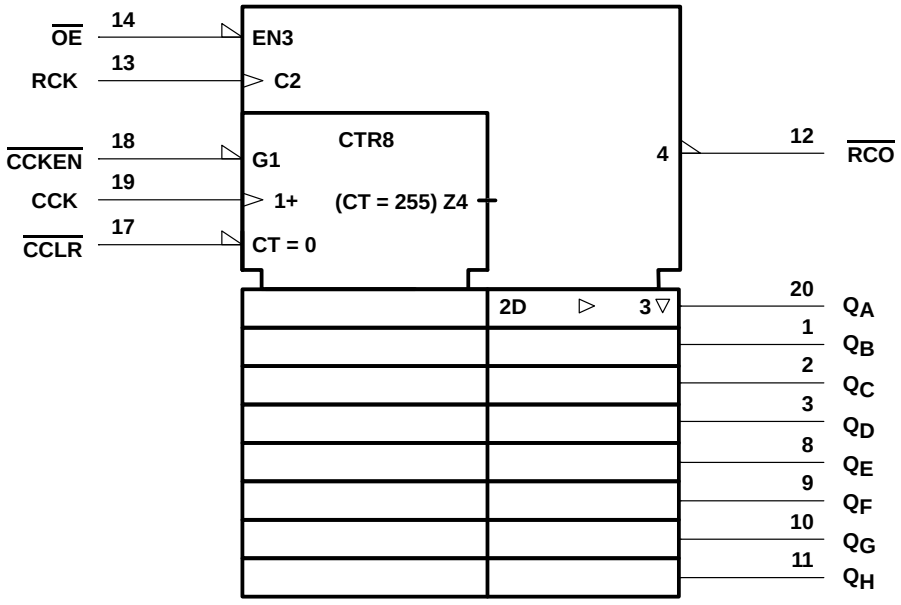
The 74ACT11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear ($\overline{CCLR}$) input and a count-enable ($\overline{CCKEN}$) input. For cascading, a ripple-carry ($\overline{RCO}$) output is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74ACT11590 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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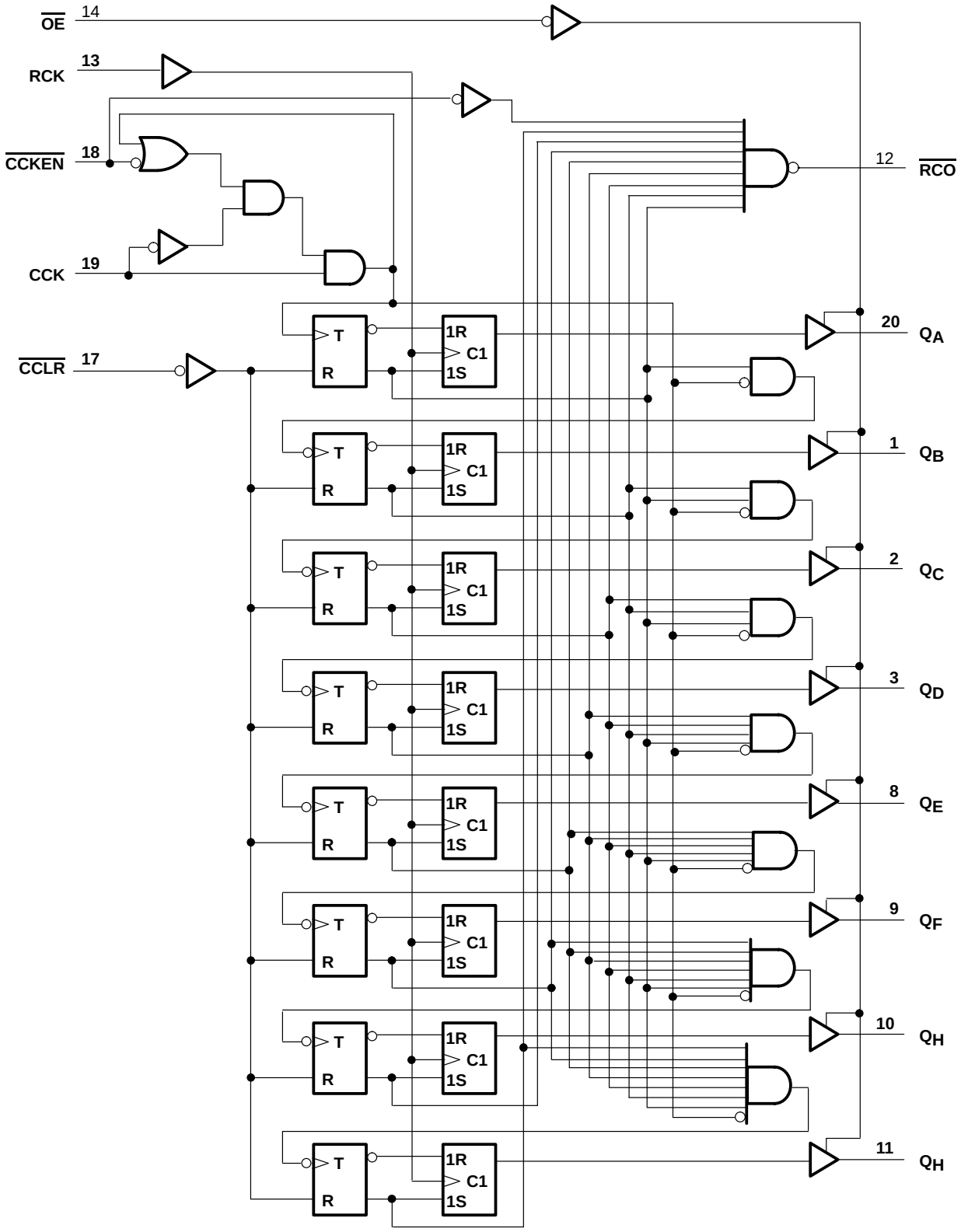
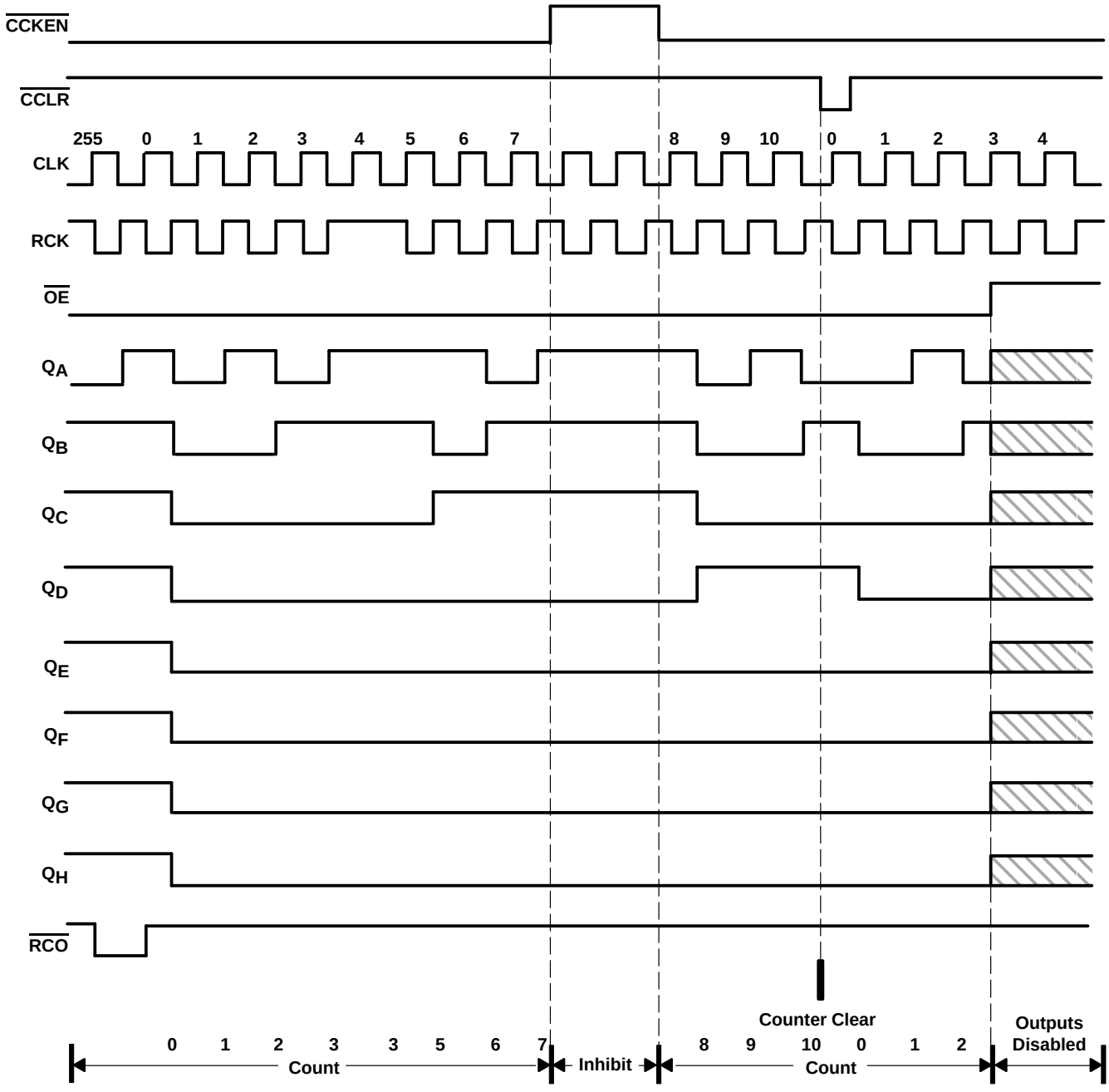
logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±225 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = –24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = –75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			±0.5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3				pF
C_o	$V_O = V_{CC}$ or GND		5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK		0	80	0	80	MHz
t_w	Pulse duration	CCK or RCK high or low	6.3		6.3		ns
		$\overline{\text{CCLR}}$ low	8.4		8.4		
t_{su}	Setup time	$\overline{\text{CCKEN}}$ low before CCK↑	5.1		5.1		ns
		$\overline{\text{CCLR}}$ high before CCK↑	1.6		1.6		
		CCK↑ before RCK↑§	5.5		5.5		
t_h	Hold time	$\overline{\text{CCKEN}}$ low after CCK↑	0.6		0.6		ns

§ This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

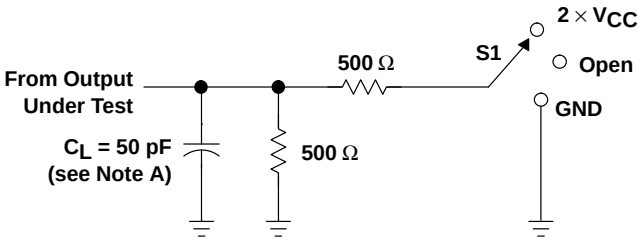
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80			80		MHz
t_{PLH}	CCK	$\overline{RCO}$	4.5	8	11	4.5	13	ns
t_{PHL}			5.1	9	13.8	5.1	16.4	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	3.5	7	11	3.5	13.1	ns
t_{PLH}	RCK	Q	4.6	8	11.1	4.6	13	ns
t_{PHL}			3.9	7.6	11.8	3.9	13.9	
t_{PZH}	$\overline{OE}$	Q	4	8.3	13.2	4	15.6	ns
t_{PZL}			3.8	8.2	13.9	3.8	16.2	
t_{PHZ}	$\overline{OE}$	Q	5.3	8	10.3	5.3	11.5	ns
t_{PLZ}			6.1	9.1	11.5	6.1	13	
t_{PLH}	$\overline{CCKEN}$	$\overline{RCO}$	3.8	6.8	9.7	3.8	11.2	ns
t_{PHL}			2.8	7.6	11	2.8	12.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

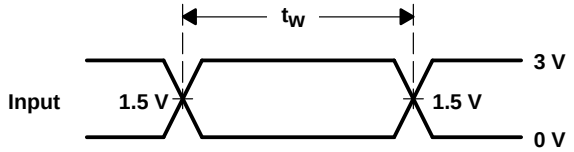
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	66	pF
		Outputs disabled			42	

PARAMETER MEASUREMENT INFORMATION

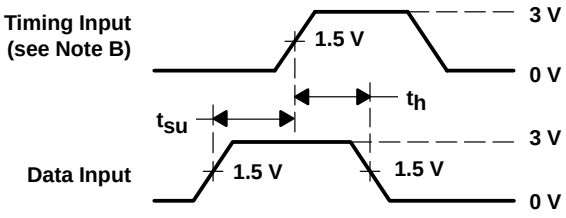


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

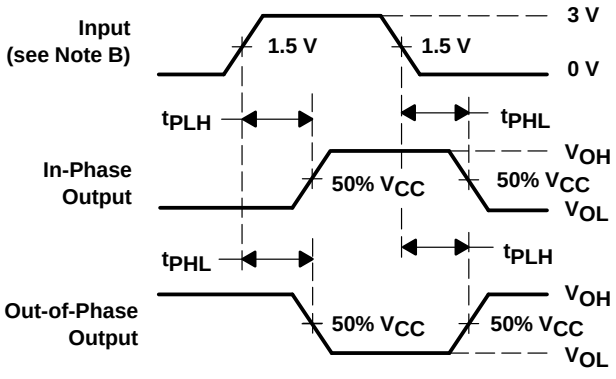
LOAD CIRCUIT



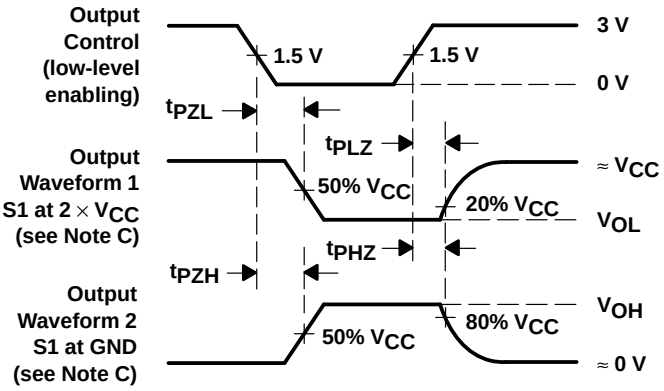
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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