

# 54ACT16841, 74ACT16841 20-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS174A – MAY 1991 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Provide Extra Bus Driving/Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) Packages, 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

## description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ACT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ( $\overline{1OE}$  or  $\overline{2OE}$ ) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$  does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

54ACT16841 . . . WD PACKAGE  
74ACT16841 . . . DGG OR DL PACKAGE  
(TOP VIEW)

$\overline{1OE}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
$\overline{2OE}$	28	29	2LE



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**TEXAS  
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WITH 3-STATE OUTPUTS

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description (continued)

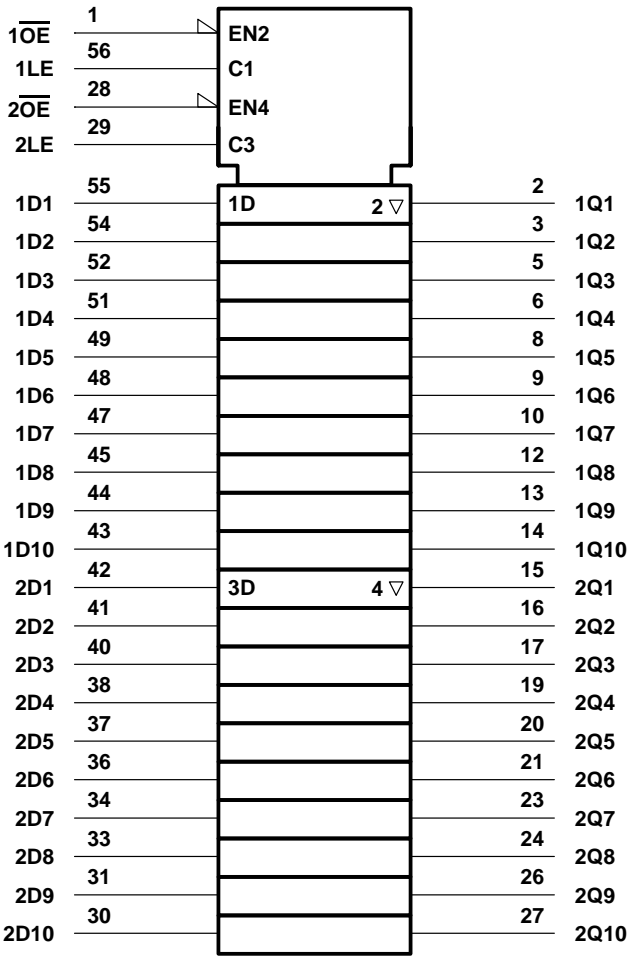
The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16841 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16841 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE  
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

logic symbol†

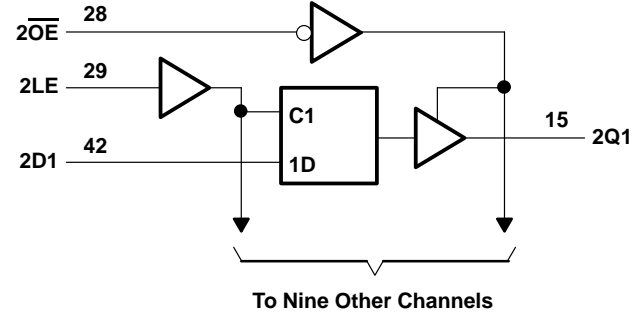
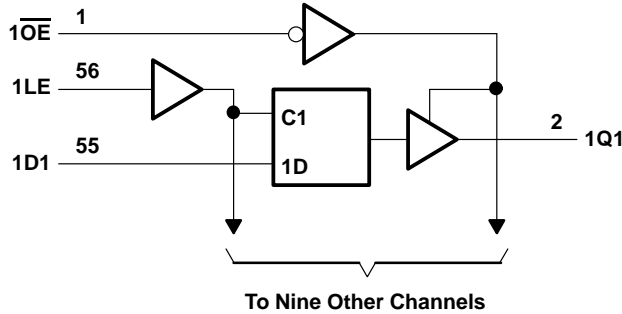


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±500 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

	54ACT16841			74ACT16841			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_I$ Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$ High-level output current			–24			–24	mA
$I_{OL}$ Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$ Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT16841		74ACT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = –24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I <sub>OH</sub> = –75 mA†	5.5 V				3.85		3.85		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I <sub>OL</sub> = 75 mA†	5.5 V				1.65		1.65		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5		±5	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80		80	µA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1		1	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			3					pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			11					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C			54ACT16841		74ACT16841		UNIT
		MIN	MAX		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	4			4		4		ns
t <sub>su</sub>	Setup time, data before LE↓	1.5			1.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓	High	3		3		3		ns
		Low	4.5		4.5		4.5		

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54ACT16841		74ACT16841		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	4	7.1	10.3	4	11.8	4	11.8	ns
t <sub>PHL</sub>			3.2	6.9	11	3.2	12.2	3.2	12.2	
t <sub>PLH</sub>	LE	Q	4.5	7.7	11.3	4.5	12.7	4.5	12.7	ns
t <sub>PHL</sub>			4.3	7.8	11.4	4.3	12.7	4.3	12.7	
t <sub>PZH</sub>	$\overline{OE}$	Q	3.1	6.4	10.1	3.1	11.3	3.1	11.3	ns
t <sub>PZL</sub>			3.8	7.6	12.1	3.8	13.7	3.8	13.7	
t <sub>PHZ</sub>	$\overline{OE}$	Q	4	7.3	9.5	4	10.2	4	10.2	ns
t <sub>PLZ</sub>			4	6.8	8.9	4	9.6	4	9.6	

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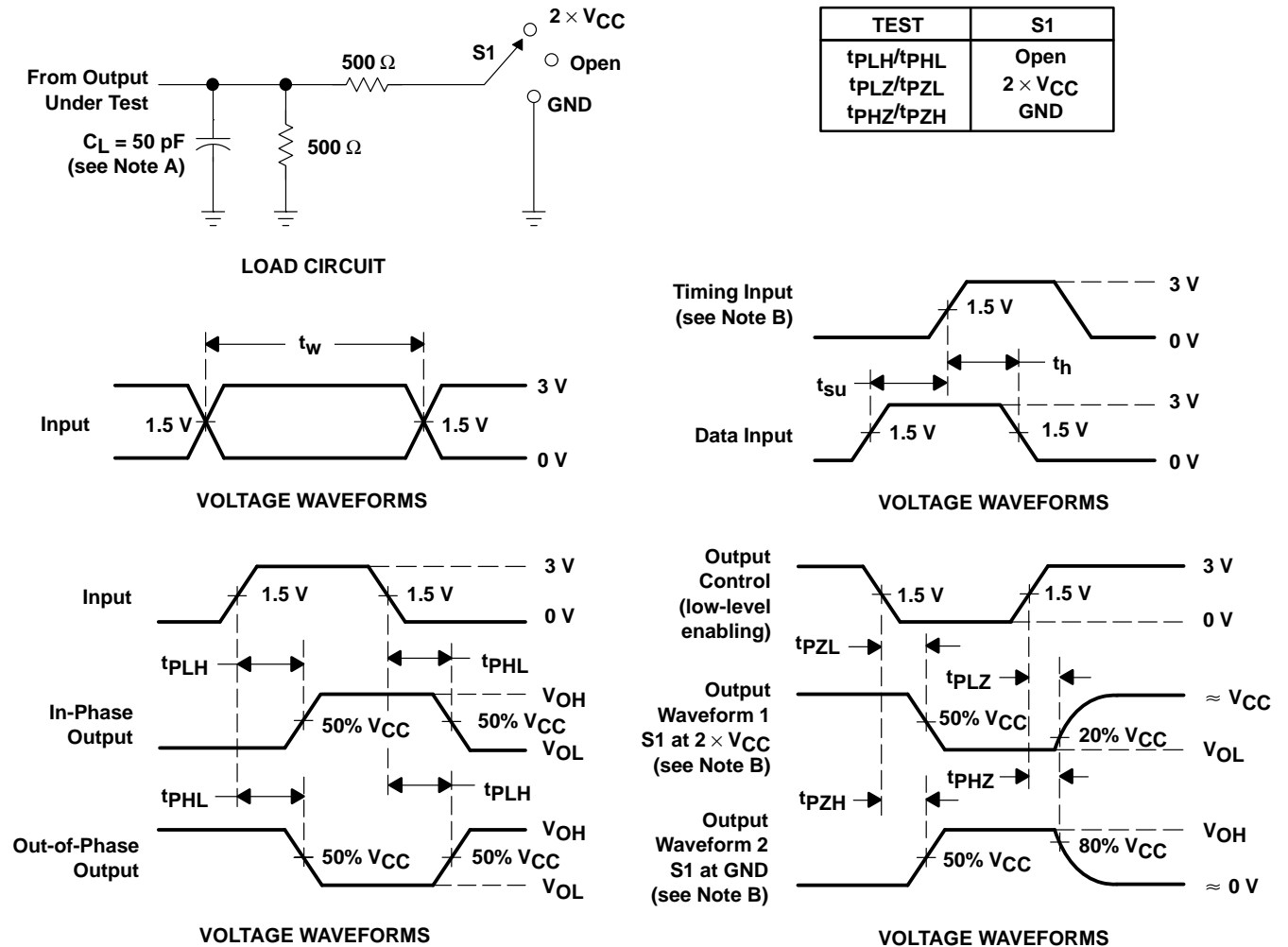
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	41	pF
	Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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