54ACT16827, 74ACT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCAS163A – JUNE 1990 – REVISED APRIL 1996

<ul> <li>Members of the Texas Instruments Widebus™ Family</li> </ul>	54ACT16827 WD PACKAGE 74ACT16827 DL PACKAGE (TOP VIEW)					
<ul> <li>Inputs Are TTL-Voltage Compatible</li> </ul>						
<ul> <li>3-State Outputs Drive Bus Lines Directly</li> </ul>	10E1		56 10E2			
<ul> <li>Flow-Through Architecture Optimizes</li> </ul>	1Y1 [	2	55 1A1			
PCB Layout	1Y2		54 🛛 1A2			
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li> </ul>	GND [	4	53 🛛 GND			
Minimizes High-Speed Switching Noise	1Y3 [		52 A3			
● EPIC <sup>™</sup> (Enhanced-Performance Implanted	-	6	51 A14			
CMOS) 1-µm Process	V <sub>CC</sub>	7	50 V <sub>CC</sub>			
<ul> <li>500-mA Typical Latch-Up Immunity at</li> </ul>	1Y5		49 1A5			
125°C	1Y6 L		48 1A6			
<ul> <li>Package Options Include Plastic 300-mil</li> </ul>	1Y7 [	10 11	47   1A7 46   GND			
Shrink Small-Outline (DL) Packages Using	-	11 12	46 GND 45 1A8			
25-mil Center-to-Center Pin Spacings and	1Y9 [		45 TA8 44 1A9			
380-mil Fine-Pitch Ceramic Flat (WD)	1Y10		43 1A10			
Packages Using 25-mil Center-to-Center	2Y1		42 2A1			
Pin Spacings	=	16	41 2A2			
description	2Y3	17	40 2A3			
	GND [	18	39 🛛 GND			
The 'ACT16827 are noninverting 20-bit buffers	2Y4 [	19	38 2A4			
composed of two 10-bit sections with separate	2Y5 [		37 2A5			
output-enable signals. For either 10-bit buffer	2Y6		36 2A6			
section, the two output-enable (10E1 and 10E2	V <sub>CC</sub> [	22	35 🛛 V <sub>CC</sub>			

output-enable signals. For either 10-bit buffer section, the two output-enable  $(1\overline{OE1} \text{ and } 1\overline{OE2} \text{ or } 2\overline{OE1} \text{ and } 2\overline{OE2})$  inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74ACT16827 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printedcircuit-board area. 

 2Y4
 19
 38
 2A4

 2Y5
 20
 37
 2A5

 2Y6
 21
 36
 2A6

 V<sub>CC</sub>
 22
 35
 V<sub>CC</sub>

 2Y7
 23
 34
 2A7

 2Y8
 24
 33
 2A8

 GND
 25
 32
 GND

 2Y9
 26
 31
 2A9

 2Y10
 27
 30
 2A10

 2OE1
 28
 29
 2OE2

The 54ACT16827 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The 74ACT16827 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

	FUNCTION TABLE (each 8-bit section)									
	INPUTS		OUTPUT							
OE1	OE2	Α	Y							
L	L	L	L							
L	L	Н	н							
н	Х	Х	Z							
Х	Н	Х	Z							



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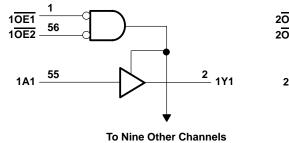
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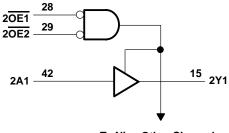
logic symbol<sup>†</sup>

1 <u>0E1</u>	1	&			
10E2	56		EN1		
2 <mark>0E1</mark>	28	&			
20E2	29		EN2		
		Ц	ㅣ _ ㅡ		
1A1	55	ſ	1 1⊽	2	1Y1
1A2	54			3	1Y2
1A3	52			5	1Y3
1A4	51			6	1Y4
1A5	49			8	1Y5
1A6	48	<u> </u>		9	1Y6
1A7	47	<u> </u>		10	1Y7
1A8	45	<u> </u>		12	1Y8
1A9	44			13	1Y9
1A3	43	<u> </u>		14	1Y10
2A1	42		1 2 ▽	15	2Y1
2A1	41		1 2 *	16	2Y2
2A2 2A3	40			17	212 2Y3
2A3 2A4	38			19	213 2Y4
2A4 2A5	37			20	
	36			21	2Y5
2A6	34	<b> </b>		23	2Y6
2A7	33	<b> </b>		24	2Y7
2A8	31	┣───		26	2Y8
2A9	30	┞───		27	2Y9
2A10					2Y10

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)





**To Nine Other Channels** 



## 54ACT16827, 74ACT16827 **20-BIT BUFFÉRS/DRIVERS** WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### recommended operating conditions (see Note 3)

		54ACT16827		54ACT16827		27	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2		W	2			V
VIL	Low-level input voltage			0.8			0.8	V
VI	Input voltage	0	24	V <sub>CC</sub>	0		VCC	V
Vo	Output voltage	0	1	VCC	0		VCC	V
ЮН	High-level output current		200	-24			-24	mA
IOL	Low-level output current		0	24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
ТА	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



## 54ACT16827, 74ACT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Т	A = 25°C	;	54ACT	16827	74ACT	16827	UNIT
FARAMETER	TEST CONDITIONS	vcc	MIN	TYP	P MAX	MIN	MAX	MIN	MAX	
	1	4.5 V	4.4			4.4		4.4		
	I <sub>OH</sub> = -50 μA	5.5 V	5.4			5.4		5.4		
VOH	I <sub>ОН</sub> = –24 mA	4.5 V	3.94			3.8		3.8		V
	10H = -24  mA	5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V				3.85		3.85		1
	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
VOL	I <sub>OL</sub> = 24 mA	4.5 V			0.36	4	0.44		0.44	14
		5.5 V			0.36	C >	0.44		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V				$\gamma_{Q_i}$	1.65		1.65	
lj	$V_I = V_{CC}$ or GND	5.5 V			±0.1	R	±1		±1	μA
I <sub>OZ</sub>	$V_{O} = V_{CC}$ or GND	5.5 V			±0.5	1	±5		±5	μA
ICC	$V_{I} = V_{CC} \text{ or GND}, \qquad I_{O} = 0$	5.5 V			8		80		80	μA
$\Delta I_{CC}^{\ddagger}$	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1		1	mA
Ci	$V_I = V_{CC}$ or GND	5 V		4.5						pF
Co	$V_{O} = V_{CC}$ or GND	5 V		16						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Т	T <sub>A</sub> = 25°C 54ACT16827		16827	74ACT16827		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	А	v	3.6	7.4	9.8	3.6	41	3.6	11	-
<sup>t</sup> PHL	A	T	2.8	7.4	9.8	2.8	10.8	2.8	10.8	ns
<sup>t</sup> PZH	OE	v	3	7.9	10.4	3	<b>Q</b> 11.7	3	11.7	-
<sup>t</sup> PZL		T	4	9.6	12.4	4)	14	4	14	ns
<sup>t</sup> PHZ	OE	v	5.8	9.1	11.3	5.8	12.4	5.8	12.4	ns
<sup>t</sup> PLZ	OE	Ι	5.3	8.5	10.5	5.3	11.5	5.3	11.5	115

## operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CO	TYP	UNIT	
C <sub>pd</sub> Power dissipation capacitance	Outputs enabled	$C_{1} = 50 \text{ pc}$	f_ 1 MU-	41	ъĘ
	Outputs disabled	C <sub>L</sub> = 50 pF, f = 1 MHz		10	р⊦

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 $2 \times V_{CC}$ TEST **S**1 0 **S1** tPLH/tPHL Open **500** Ω O Open From Output tPLZ/tPZL  $2 \times V_{CC}$  $\Lambda \Lambda$ **Under Test**  $^{\circ}$  GND GND tPHZ/tPZH  $C_L = 50 \text{ pF}$ **500** Ω (see Note A) ÷ LOAD CIRCUIT Output 3 V 3 V Control Input 5 V 1.5 V 1.5 V 1.5 V (low-level 0 V 0 V enabling) <sup>t</sup>PZL -<sup>t</sup>PHL <sup>t</sup>PLH tPLZ -Output VOH ≈ Vcc In-Phase Waveform 1 50% V<sub>CC</sub> 50% V<sub>CC</sub> 50% V<sub>CC</sub> 20% V<sub>CC</sub> S1 at  $2 \times V_{CC}$ Output VOL Vol (see Note B) tPHZ -<sup>t</sup>PLH <sup>t</sup>PZH → Output ۷он ۷он 80% V<sub>C</sub>C **Out-of-Phase** Waveform 2 50% V<sub>CC</sub> 50% V<sub>CC</sub> 50% VCC S1 at GND Output Vol ≈ 0 V (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** 

### PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub> = 3 ns, t<sub>f</sub> = 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

### Figure 1. Load Circuit and Voltage Waveforms



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