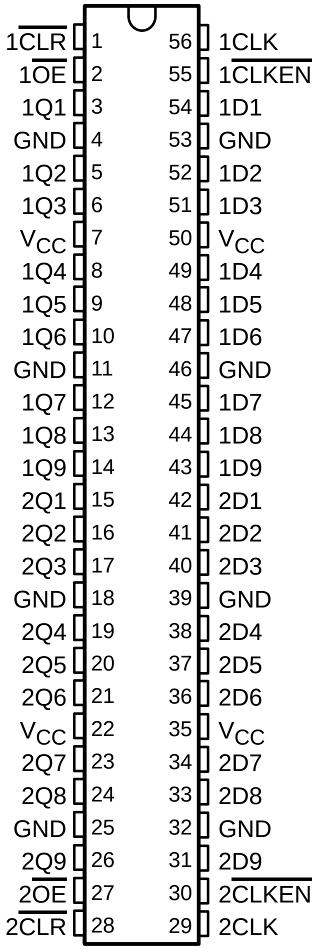
54ACT16823, 74ACT16823
18-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS160A – APRIL 1991 – REVISED APRIL 1996

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16823 . . . WD PACKAGE
74ACT16823 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

The ’ACT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16823 is packaged in theTI shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16823 is characterized for operation over the full military temperature range of 55°C to 125°C. The 74ACT16823 is characterized for operation from –40°C to 85°C

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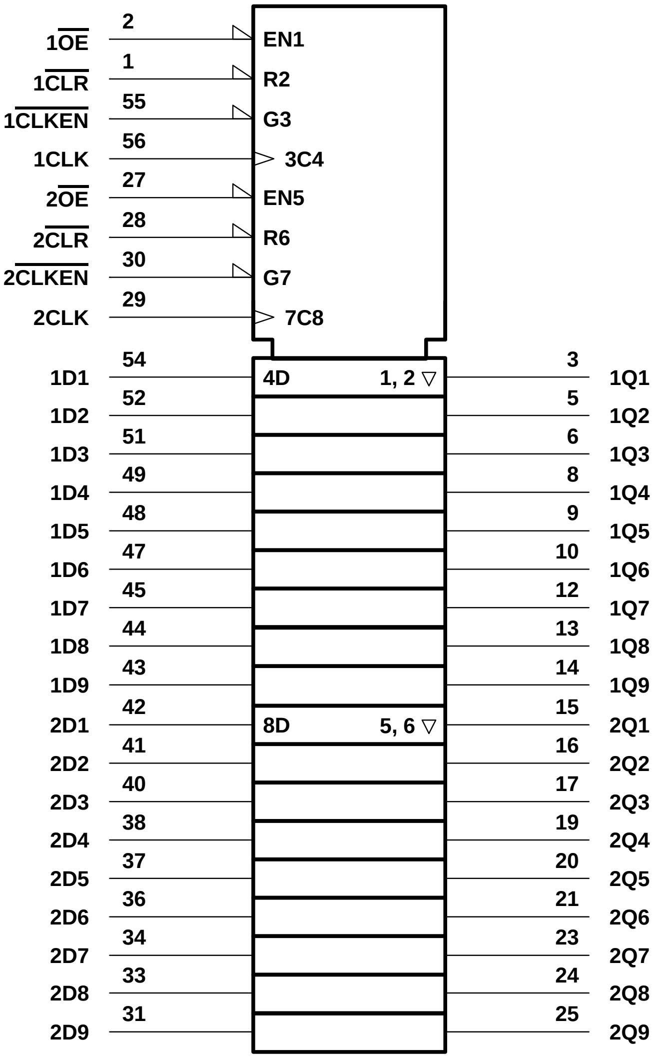
TEXAS INSTRUMENTS

FUNCTION TABLE
(each 9-bit stage)

INPUTS					OUTPUT
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



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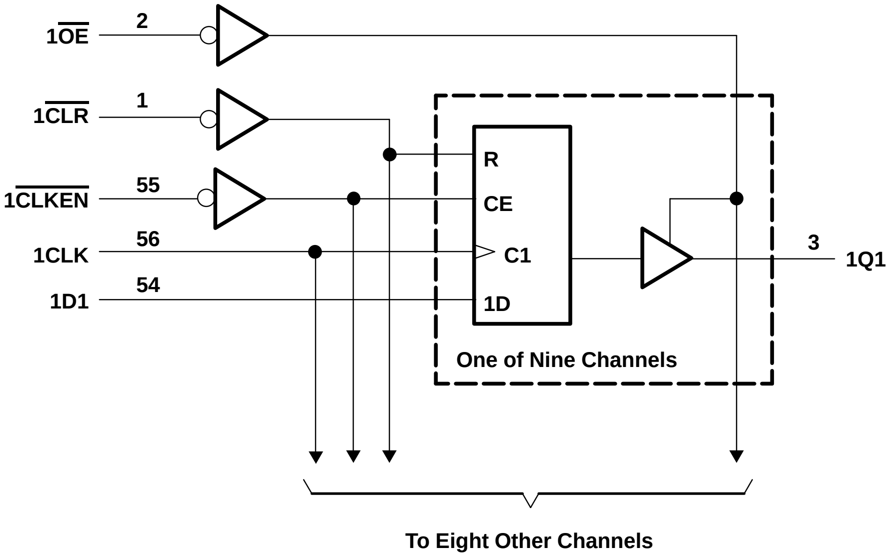
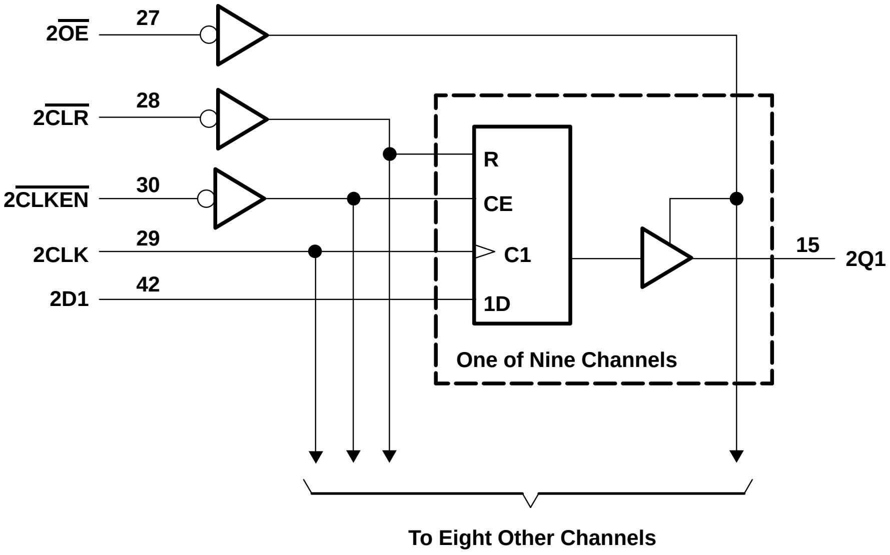
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . 1.4 W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 2)

		54ACT16823			74ACT16823			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	54ACT16823 MIN	54ACT16823 MAX	74ACT16823 MIN	74ACT16823 MAX	UNIT
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I_{OH}= –75 mA†	5.5 V				3.85		3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3						pF
C_o	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C MIN	T_A = 25°C MAX	54ACT16823 MIN	54ACT16823 MAX	74ACT16823 MIN	74ACT16823 MAX	UNIT
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	$\overline{\text{CLR}}$ low	3.3		3.3		3.3		ns
		CLK high or low	5.5		5.5		5.5		
t_{su}	Setup time before CLK↑	$\overline{\text{CLR}}$ inactive	0.5		0.5		0.5		ns
		Data	7		7		7		
		$\overline{\text{CLKEN}}$ low	3.5		3.5		3.5		
t_h	Hold time after CLK↑	Data	0.5		0.5		0.5		ns
		$\overline{\text{CLKEN}}$ high or low	2.5		2.5		2.5		

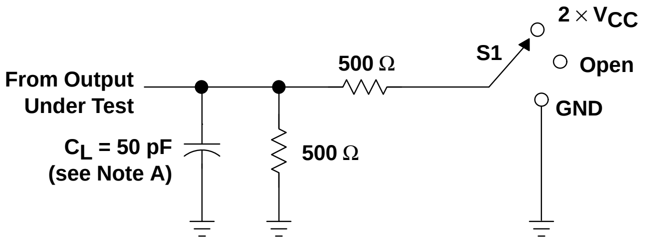
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16823		74ACT16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	CLK	Q	4.2	7.5	10.6	4.2	12.1	4.2	12.1	ns
t_{PHL}			4.8	8.3	11.5	4.8	12.9	4.8	12.9	
t_{PHL}	$\overline{\text{CLR}}$	Q	3.4	7.3	11.2	3.4	12.5	3.4	12.5	ns
t_{PZH}	$\overline{\text{OE}}$	Q	2.4	5.9	9.5	2.4	10.7	2.4	10.7	ns
t_{PZL}			3.3	7.1	11.3	3.3	12.8	3.3	12.8	
t_{PHZ}	$\overline{\text{OE}}$	Q	5.5	7.6	9.7	5.5	10.3	5.5	10.3	ns
t_{PLZ}			4.6	6.7	8.8	4.6	9.4	4.6	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

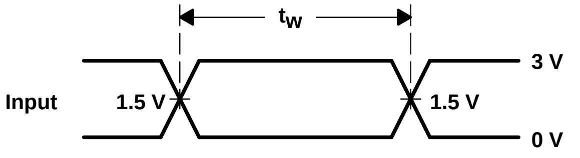
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		24	

PARAMETER MEASUREMENT INFORMATION

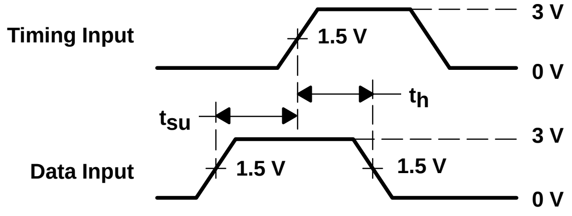


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



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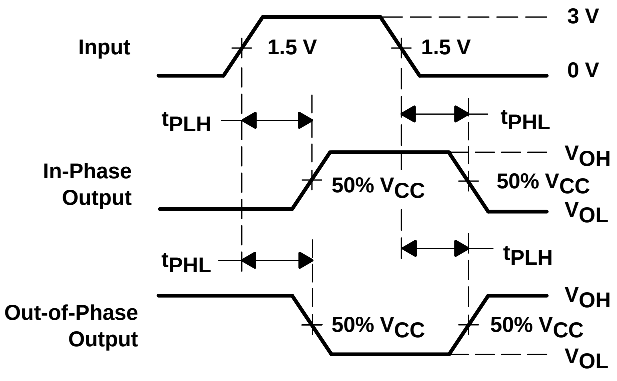
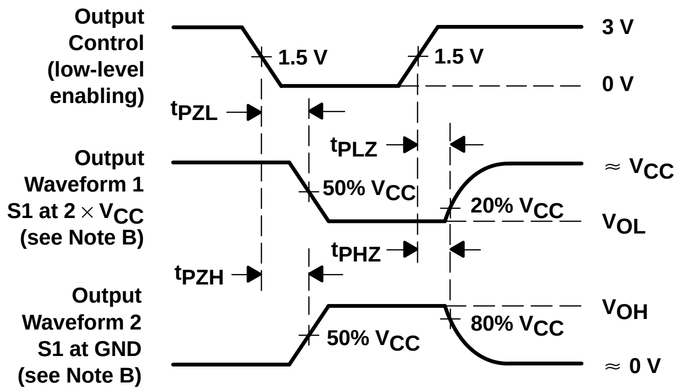


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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