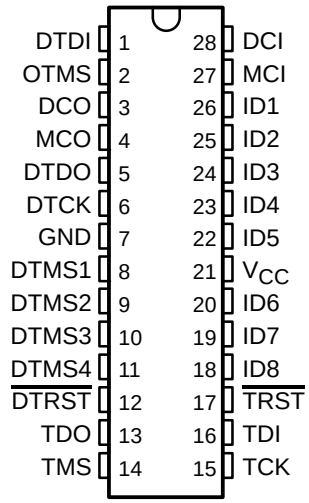
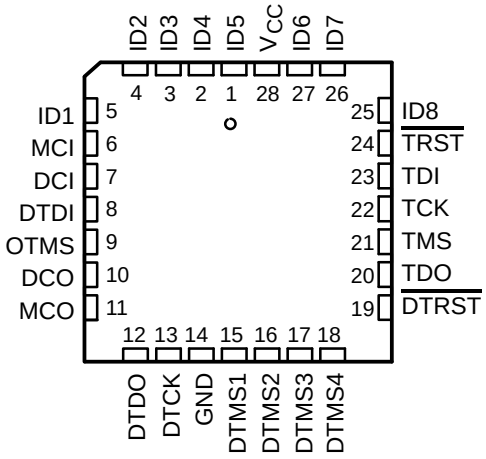
- **Members of theTexas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus**
- **Allow Partitioning of System Scan Paths**
- **Can Be Cascaded Horizontally or Vertically**
- **Select One of Four Secondary Scan Paths to Be Included in a Primary Scan Path**
- **Provide Communication Between Primary and Remote Test Bus Controllers**
- **Include 8-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals**
- **Include 8-Bit Identification Bus for Scan Path Identification**
- **Inputs Are TTL Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ACT8999 . . . JT PACKAGE
SN74ACT8999 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ACT8999 . . . FK PACKAGE
(TOP VIEW)



description

The ’ACT8999 are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components facilitates testing of complex circuit-board assemblies.

The ’ACT8999 enhance the scan capability of TI’s SCOPE™ family by allowing augmentation of a system’s primary scan path with secondary scan paths (SSPs), which can be individually selected by the ’ACT8999 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select one of four secondary scan paths. This has the effect of shortening the scan path to allow maximum test throughput when an individual subsystem (board or box) is to be tested. Any of the device’s six data registers or the instruction register can be placed in the device’s scan path, i.e., placed between test data input (TDI) and test data output (TDO) for subsequent shift and scan operations.

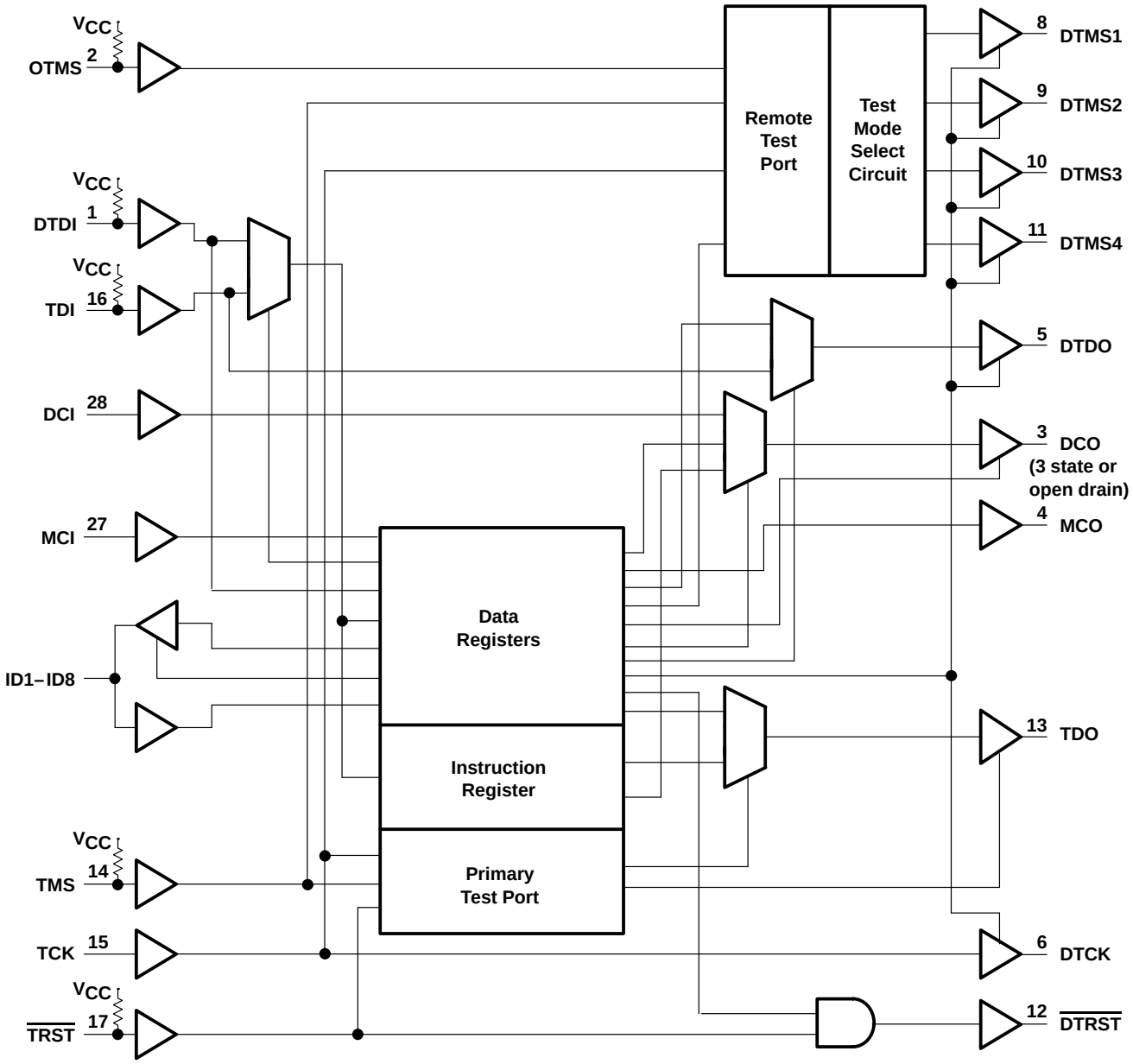
All operations of the device except counting are synchronous to the test clock (TCK). The 8-bit programmable up/down counter can be used to count transitions on the device condition input (DCI) and output interrupt signals via the device condition output (DCO). The device can be configured to count on either the rising or falling edge of DCI.

description (continued)

If a system's test architecture contains more than one test bus controller, the 8-bit bidirectional bus can be used to interface a higher-level primary bus controller (PBC) with one or more lower-level remote bus controllers (RBCs). A protocol allows the PBC to pass control of the 'ACT8999 to an RBC, freeing the PBC for other tasks. The 8-bit bus also can be hardwired to provide one of 256 codes for subsystem identification. The test access port (TAP) controller is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8999 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8999 is characterized for operation from 0°C to 70°C.

functional block diagram



Pin numbers shown are for the DW, JT, and NT packages.

functional block description

The ’ACT8999 implements two separate functions in one package. The primary function of the device is to include a selected secondary scan path in the system’s primary scan path to enable a PBC to perform controlling and observing test functions on the selected path. This is accomplished by driving the TMS terminal(s) of a secondary scan path with one of the DTMS pins of the device. This approach allows a system to have built-in testability at all levels without requiring that the primary-system scan path always include all subsystem scan paths. As a result, test throughput is improved and the amount of test data that must be interpreted is reduced. The device includes error-detection circuitry that prevents the user from inadvertently activating more than one secondary scan path at a time.

Another function of the device is provided by the 8-bit identification bus. This bus can be hardwired with pullup and pulldown resistors to supply an identification code to the test controller(s) to verify that test operations are being performed on the proper portion of the system. The bus can also transfer data and instructions to another device, such as a local or remote bus controller, and pass control of the scan-path select function to that device. This frees the primary controller to activate another secondary scan path elsewhere in the system or perform higher-level test control functions. When the RBC is ready to return control of the device, interrupt signals alert the primary controller.

The least-significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most-significant bit (MSB) is the last bit shifted in (nearest to TDI). The ’ACT8999 is divided into functional blocks as detailed below.

test ports

The test ports decode the signals on TCK, TMS, OTMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. Each test port includes a TAP controller that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP controller state diagram is shown in Figure 1. Two test ports are included on the ’ACT8999, allowing different test controllers to command different sections of the device.

TMS circuit

The TMS circuit decodes bits in the select and control registers to determine which one, if any, of the DTMS pins (which provide mode-select signals to the secondary scan path(s)) follow the TMS pin or OTMS pin. The unselected DTMS pins are set by the circuit to a static high or low level.

instruction register

The instruction register (IR) is an 8-bit-wide serial-shift register that issues commands to the device. Data is input to the instruction register via TDI or DTDI and shifted out via TDO. All device operations are initiated by loading the proper instruction or sequence of instructions into the IR.

data registers

Six parallel data registers are included in the ’ACT8999: bypass, control, counter, boundary-scan, ID-bus, and select. The ID bus register is a part of the boundary-scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO. Table 1 summarizes the registers in the ’ACT8999.

Table 1. Register Summary

REGISTER NAME	LENGTH (BITS)	FUNCTION
Instruction	8	Issue command information to the device
Remote Instruction	8	Issue command information to the select register
Control	13	Configuration and enable control
Counter	8	Count events on DCI, output interrupts via DCO
Select	8	Select one of four DTMS pins to follow TMS or OTMS
Boundary Scan	15	Capture and force test data at device periphery
ID Bus	8	Pass test commands and data between a PBC and RBC(s)
Bypass	1	Remove the ’ACT8999 from the scan path

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
DCI	I	Device condition input. DCI receives interrupt and protocol signals from an RBC and/or the secondary scan path(s). When the counter register is instructed to count up or down, DCI is configured as the counter clock.
DCO	O	Device condition output. DCO is configured by the control register to output protocol and interrupt signals to a PBC. It also can be configured by the control register to output an error signal if the instruction register or select register are loaded with invalid values. DCO is further configured by the control register as: Active high or active low (reset condition = active low) Open drain or 3-state (reset condition = open drain)
DTCK	O	Device test clock. DTCK outputs the buffered test clock TCK to the secondary scan path(s).
DTDI	I	Device test data input. DTDI receives the serial test data output of the selected secondary scan path. An internal pullup forces DTDI to a high logic level if it is left unconnected.
DTDO	O	Device test data output. DTDO outputs serial test data to the TDI input(s) of the secondary scan path(s).
DTMS1 DTMS2 DTMS3 DTMS4	O	Device test mode select 1–4. Either one or none of these four outputs can be selected to follow TMS or OTMS to include a secondary scan path in the primary scan path. The unselected DTMS outputs can be independently set to a static high or low logic level. The TMS circuit monitors input from the select register to determine the configuration of the DTMS outputs.
$\overline{\text{DTRST}}$	O	Device test reset. This active-low output transmits a reset signal to the secondary scan path(s). $\overline{\text{DTRST}}$ can be asserted by a bit in the control register or by setting $\overline{\text{TRST}}$ low.
GND		Ground
ID1 ID2 ID3 ID4 ID5 ID6 ID7 ID8	I/O	Identification 1–8. This 8-bit data bus can be used to communicate with an RBC and pass data and control instructions. By wiring pullup and pulldown resistors to these terminals, one of 255 unique identification codes can be assigned to the device to allow a test controller to determine the identity of the subsystem under test.
MCI	I	Master condition input. MCI receives interrupt and protocol singals from a PBC.
MCO	O	Master condition output. MCO transmits interrupt and protocol signals to an RBC and/or the secondary scan path(s). MCO also outputs an active-low error signal during the Pause-DR TAP state if an RBC loads an invalid value in the select register.
OTMS	I	Optional test mode select. OTMS can be used instead of TMS to control the select register. This is useful when a remote bus controller is available to control the secondary scan path(s). An internal pullup forces OTMS to a high level if left unconnected.
TCK	I	Test clock. One of four terminals required by IEEE Standard 1149.1. All operations of the 'ACT8999 except for the count function are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI	I	Test data input. One of four terminals required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or selected data register. TDI is typically driven by the TDO output of the primary bus controller. An internal pullup forces TDI to a high level if it is left unconnected.
TDO	O	Test data output. One of four terminals required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or selected data register. TDO is typically connected to the TDI input of the next scannable device in the primary scan path.
TMS	I	Test mode select. One of four terminals required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8999 through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
$\overline{\text{TRST}}$	I	Test reset. This active-low input inplements the optional reset terminal of IEEE Standard 1149.1. When asserted, $\overline{\text{TRST}}$ causes the 'ACT8999 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. $\overline{\text{TRST}}$ is also output without inversion via $\overline{\text{DTRST}}$. An internal pullup forces $\overline{\text{TRST}}$ to a high level if left unconnected.
V_{CC}		Supply voltage

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

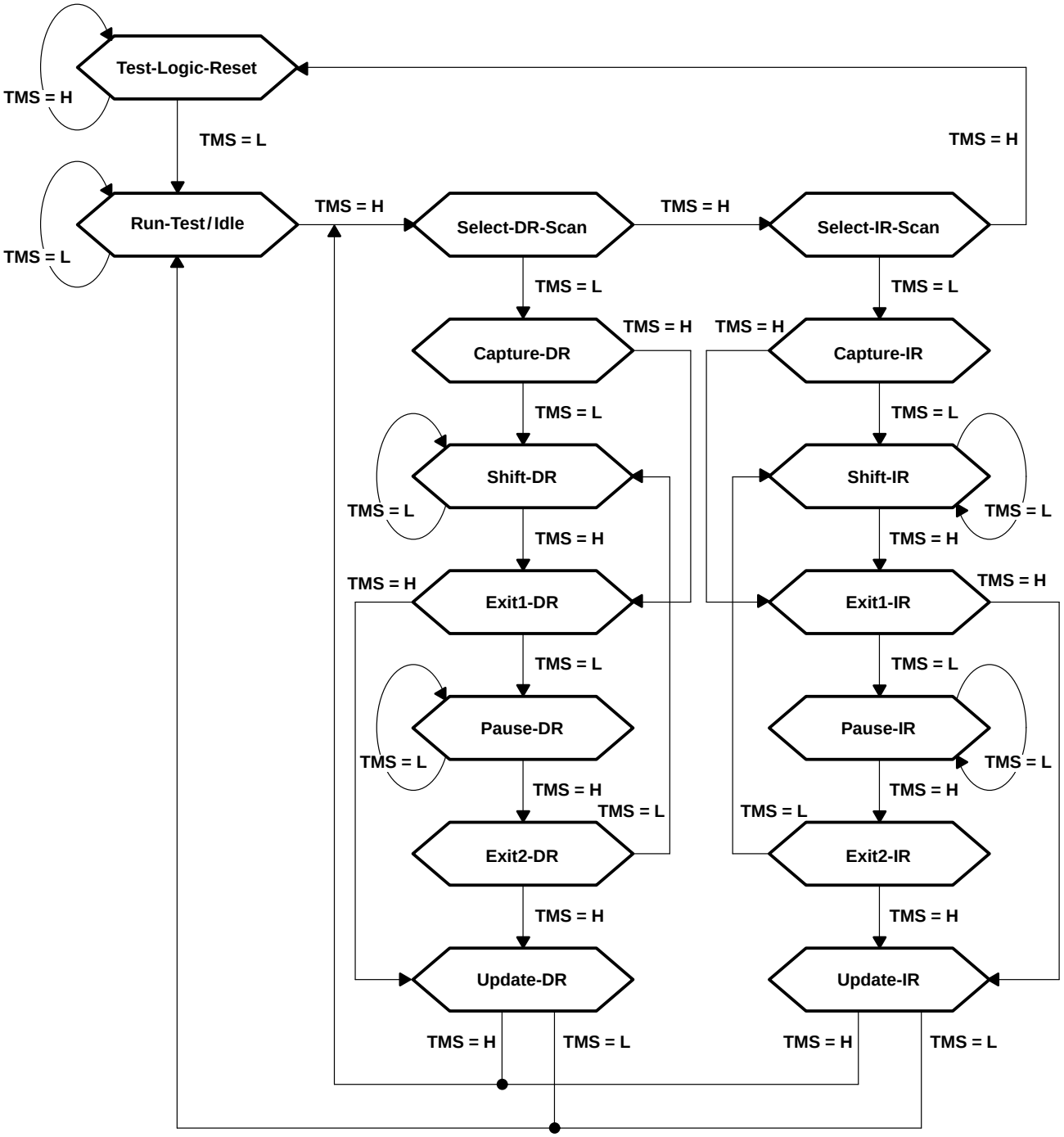


Figure 1. TAP-Controller State Diagram

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if the test mode select (TMS) input is high. The TMS pin has an internal pullup that forces it to a high level if it is left unconnected or if a board defect causes it to be open circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle. The 8-bit programmable up/down counter can be operated in this state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. TDO enables to the value present in the least-significant bit of the selected data register.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state suspends and resumes shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state, and will enable to a high level.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR. TDO changes from the active state to the high-impedance state on the falling edge of TCK in Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state suspends and resumes shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

instruction register description

The instruction register (IR) is an 8-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the ’ACT8999 and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal ($\overline{\text{IRERR}}$) is generated internally as shown in Table 3. The ’ACT8999 can be configured to output $\overline{\text{IRERR}}$ via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4. Figure 2 shows the order of scan for the IR.

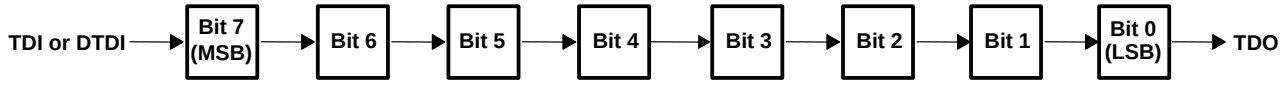


Figure 2. Instruction-Register Bits and Order of Scan

Table 2. Instruction-Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	00	EXTEST	Boundary scan	Boundary scan	Test
10000001	81	BYPASS	Bypass scan	Bypass	Normal
10000010	82	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	03	INTEST	Boundary scan	Boundary scan	Test
10000100	84	BYPASS†	Bypass scan	Bypass	Normal
00000101	05	BYPASS†	Bypass scan	Bypass	Normal
00000110	06	BYPASS†	Bypass scan	Bypass	Normal
10000111	87	BYPASS†	Bypass scan	Bypass	Normal
10001000	88	COUNT	Count	Bypass	Normal
00001001	09	COUNT	Count	Bypass	Normal
00001010	0A	BYPASS†	Bypass scan	Bypass	Normal
10001011	8B	BYPASS†	Bypass scan	Bypass	Normal
00001100	0C	BYPASS†	Bypass scan	Bypass	Normal
10001101	8D	BYPASS	Bypass scan	Bypass	Normal
10001110	8E	SCANCN	Control register scan	Control	Normal
00001111	0F	SCANCN	Control register scan	Control	Normal
11111010	FA	SCANCNT	Counter scan	Counter	Normal
01111011	7B	READCNT	Counter read	Counter	Normal
11111100	FC	SCANIDB	ID bus register scan	ID bus	Normal
01111101	7D	READIDB	ID bus register read	ID bus	Normal
01111110	7E	SCANSEL	Select register scan	Select	Normal
All others		BYPASS	Bypass scan	Bypass	Normal

† A SCOPE opcode exists but is not supported by the 'ACT8999.

Table 3. $\overline{\text{IRERR}}$ Function Table

NO. OF INSTRUCTION REGISTER BITS = 1	$\overline{\text{IRERR}}$
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

Table 4. Instruction-Register Status Word

IR BIT	VALUE‡
7	$\overline{\text{IRERR}}$ (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	$\overline{\text{SRERR}}$ (see Table 8)
1	0
0	1

‡ This value is loaded in the instruction register during the Capture-IR TAP state.

instruction-register opcode description

The operation of the 'ACT8999 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state. All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8999.

boundary scan

This instruction implements the required EXTEST and optional INTEST operations of IEEE Standard 1149.1. The boundary-scan register (which includes the ID-bus register) is placed in the scan path. Data appearing at input pins included in the boundary-scan register is captured. Data previously loaded into the output pins included in the boundary-scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary-scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary-scan register is sampled on the rising edge of TCK in Capture-DR.

count

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be configured by the control register to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

control-register scan

The control register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

counter-register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

counter-register read

The counter register is placed in the scan path. During Capture-DR, the prior preload value of the counter is loaded into the counter register. At Update-DR, the newly shifted value is preloaded to the counter.

ID-bus-register scan

The ID-bus register (a subset of the boundary-scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID-bus register on the rising edge of TCK in Capture-DR.

ID-bus register read

The ID-bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select-register scan

The select register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

control-register description

The control register (CTLR) is a 13-bit serial register that controls the enable and select functions of the ’ACT8999. A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5. The enable and select functions of the control register bits are mapped as follows:

Table 5. Control-Register Bit Mapping

BIT	VALUE	FUNCTION
12	0	Configure counter to count up
	1	Configure counter to count down
11	0	Do not stop counting when the count reaches 00000000
	1	Stop counting when the count reaches 00000000 (count down only)
10	0	Configure DCO as an active-low output
	1	Configure DCO as an active-high output
9, 8	00	DCO = Inactive (level depends on CTLR bit 10)
	01	DCO = ($\overline{\text{IRERR}}$ • $\overline{\text{SRERR}}$)
	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000 (count down) or 11111111 (count up)
	11	DCO = DCI
7	0	Do not mask $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ from DCO
	1	Mask $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ from DCO
6	0	Configure DCO as an open-drain output
	1	Configure DCO as a 3-state output
5	0	Disable DCO
	1	Enable DCO
4	0	Configure DCI as an active-low input
	1	Configure DCI as an active-high input
3	0	Enable DTCK, DTDO, and DTMS(1–4)
	1	Disable DTCK, DTDO, and DTMS(1–4)
2	0	Disable ID(1–8)
	1	Enable ID(1–8)
1	0	Disable RBC
	1	Enable RBC
0	0	$\overline{\text{DTRST}}$ = $\overline{\text{TRST}}$
	1	$\overline{\text{DTRST}}$ = L

Bit 12 – $\overline{\text{Up}}$/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 11 – Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 12 = 0.

Bit 10 – DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active low).

Bit 9/Bit 8 – DCO Source Select 1/DCO Source Select 0

DCO can be used to output two error signals generated by the 'ACT8999: $\overline{\text{IRERR}}$ (see Table 3) and $\overline{\text{SRERR}}$ (see Table 8). Bits 9 and 8 can be set to output $\overline{\text{IRERR}}$ via DCO on the falling edge of TCK in the Pause-IR state and $\overline{\text{SRERR}}$ via DCO on the falling edge of TCK in the Pause-DR state. DCO also can be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 7 – Parity Mask

The internal error signals can be masked from appearing on DCO even if bits 9 and 8 are set such that $\overline{\text{IRERR}}$ and $\overline{\text{SRERR}}$ are output in the Pause-IR and Pause-DR states (reset condition = do not mask $\overline{\text{IRERR}}$ or $\overline{\text{SRERR}}$).

Bit 6 – DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The 3-state configuration allows the DCO output to be connected to a bus.

Bit 5 – DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 4 – DCI Polarity Select

DCI can be configured as an active-low or active-high input (reset condition = active low).

Bit 3 – Device Test Pins Output Enable (active low)

DTCK, DTDO, and DTMS(1–4) pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Bit 2 – ID Bus Enable

The ID bus (ID1–8) is a bidirectional bus. The output buffers are enabled and disabled with this bit (reset condition = output buffers disabled).

Bit 1 – Remote-Bus-Controller (RBC) Enable

An RBC can issue protocol and data instructions to the select register if the 'ACT8999 is configured to allow it (reset condition = RBC disabled). When an RBC is enabled, the TAP in the select register operates according to the OTMS signal.

Bit 0 – Device Test Reset

$\overline{\text{DTRST}}$ can be configured to output a reset signal independently of the level on $\overline{\text{TRST}}$ (reset condition = no reset signal issued).

Several control-register bits affect the functionality of the DCO output. The DCO function table is given in Table 6. Figure 3 shows the order of scan for the control register.

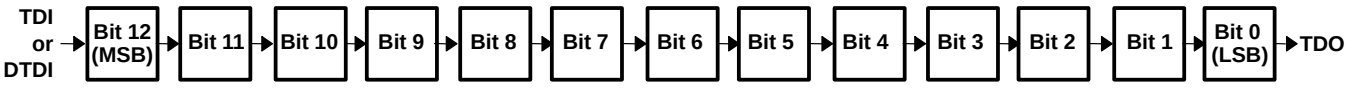


Figure 3. Control-Register Bits and Order of Scan

Table 6. DCO Function Table

DCI	INTERNAL SIGNALS†			CONTROL REGISTER BITS‡							DCO
	$\overline{\text{IRERR}}$	$\overline{\text{SRERR}}$	$\overline{\text{CE}}$	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	
X	X	X	X	X	X	X	X	0	0	X	H
X	X	X	X	X	X	X	X	1	0	X	Z
X	X	X	X	0	0	0	X	X	1	X	H
X	X	X	X	1	0	0	X	X	1	X	L
X	X	X	X	0	0	1	1	X	1	X	H
X	X	X	X	1	0	1	1	X	1	X	L
X	0	X	X	0	0	1	0	X	1	X	L in Pause-IR§, H otherwise
X	X	0	X	0	0	1	0	X	1	X	L in Pause-DR§, H otherwise
X	1	1	X	0	0	1	0	X	1	X	H
X	0	X	X	1	0	1	0	X	1	X	H in Pause-IR§, L otherwise
X	X	0	X	1	0	1	0	X	1	X	H in Pause-DR§, L otherwise
X	1	1	X	1	0	1	0	X	1	X	L
X	X	X	0	0	1	0	X	X	1	X	L
X	X	X	0	1	1	0	X	X	1	X	H
X	X	X	1	0	1	0	X	X	1	X	H
X	X	X	1	1	1	0	X	X	1	X	L
L	X	X	X	1	1	1	X	X	1	0	H
L	X	X	X	1	1	1	X	X	1	1	L
L	X	X	X	0	1	1	X	X	1	0	L
L	X	X	X	0	1	1	X	X	1	1	H
H	X	X	X	1	1	1	X	X	1	0	L
H	X	X	X	1	1	1	X	X	1	1	H
H	X	X	X	0	1	1	X	X	1	0	H
H	X	X	X	0	1	1	X	X	1	1	L

† These signals are generated as described elsewhere in this data sheet.
‡ The control register must contain these values after the TAP has passed through its most recent Update-DR state.
§ DCO becomes active on the falling edge of TCK as the TAP enters the appropriate pause state (Pause-IR or Pause-DR) and becomes inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (Exit2-IR or Exit2-DR).

select register description

The select register (SR) is an 8-bit serial register that determines which one, if any, of the DTMS lines follows the TMS or OTMS input. A reset operation forces all bits to a logic 0. The register is divided into four 2-bit sections, each of which controls one DTMS output. Figure 4 shows the mapping of the bits to the DTMS outputs and the order of scan. For each DTMS pin, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of DTMS2 and bit 2 is the LSB of DTMS2).

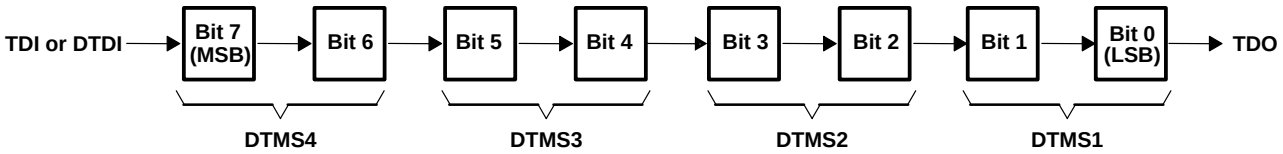


Figure 4. Select Register Bits and Order of Scan

select register description (continued)

Only one of the four DTMS outputs can be selected to drive a secondary scan path with TMS or OTMS. If the SR is loaded with an invalid value, an error signal ($\overline{\text{SRERR}}$) is generated internally as shown in Table 8. If the TAP enters the Pause-DR state, $\overline{\text{SRERR}}$ may be output via DCO (see Table 8). If the TAP enters the Update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level.

When a new 8-bit value is loaded into the SR, the configuration of one or more DTMS pins may change. If the new value of the SR configures a DTMS pin to a static (high or low) level, it assumes that level on the falling edge of TCK in the Update-DR TAP state. This condition is independent of any previous SR configurations. If the new value of the SR forces a DTMS pin to follow TMS (i.e., select a single secondary scan path) and a DTMS pin is currently in the TMS/OTMS-follow mode, the transfer of the DTMS line occurs on the falling edge of TCK in the Update-DR TAP state. However, if the new configuration forces a DTMS pin to follow TMS/OTMS while no other DTMS pin is selected, the DTMS pin does begin following TMS/OTMS until the falling edge of TCK in the Run-Test/Idle TAP state; therefore, when an SSP is initially selected, the TAP state should travel from Update-DR to Run-Test/Idle, not from Update-DR to Select-DR-Scan. Additionally, when deselecting from any DTMS output the TAP state must proceed back through Capture-DR to fully disconnect from SSP operations.

The SR can also be accessed from an RBC. A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR. The SR bit decoding is shown in Table 7.

Table 7. Select-Register Bit Decoding

MSB	LSB	DTMS SOURCE
0	0	H
0	1	L
1	0	OTMS
1	1	TMS

Table 8. $\overline{\text{SRERR}}$ Function Table

SELECT REGISTER BITS								$\overline{\text{SRERR}}$
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0	X	0	X	0	X	0	X	1
1	X	0	X	0	X	0	X	1
0	X	1	X	0	X	0	X	1
0	X	0	X	1	X	0	X	1
0	X	0	X	0	X	1	X	1
1	X	1	X	X	X	X	X	0
1	X	X	X	1	X	X	X	0
1	X	X	X	X	X	1	X	0
X	X	1	X	1	X	X	X	0
X	X	1	X	X	X	1	X	0
X	X	X	X	1	X	1	X	0

boundary-scan register/ID-bus register description

The boundary-scan register (BSR) is a 15-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary-scan cells (BSCs). Table 9 lists the device signal for each of the 15 BSCs that comprise the BSR. A reset operation does not affect the contents of the BSR.

Table 9. Boundary-Scan Register Bit Mapping

BIT	TERMINAL NAME	SIGNAL DESCRIPTION
14	MCI	Master condition in
13	MCO	Master condition out
12	DCI	Device condition in
11	$\overline{\text{DCOTS}}$†	Enable control for DCO in 3-state configuration (active low)
10	$\overline{\text{DCOOD}}$†	Enable control for DCO in open-drain configuration (active low)
9	DCO	Device condition out
8	$\overline{\text{IDBOE}}$†	Enable control for ID bus (active low)
7	ID8	Identification bus bit 8
6	ID7	Identification bus bit 7
5	ID6	Identification bus bit 6
4	ID5	Identification bus bit 5
3	ID4	Identification bus bit 4
2	ID3	Identification bus bit 3
1	ID2	Identification bus bit 2
0	ID1	Identification bus bit 1

† This internal signal cannot be observed from the I/O pins of the device.

The eight BSCs connected to the ID(1–8) pins form a subset of the BSR called the ID-bus register (IDBR). The IDBR can be scanned without accessing the remaining BSCs of the BSR. The IDBR is used when the ID bus is enabled to allow communication between a PBC and one or more RBCs. Figure 5 shows the order of scan for the BSR and IDBR.

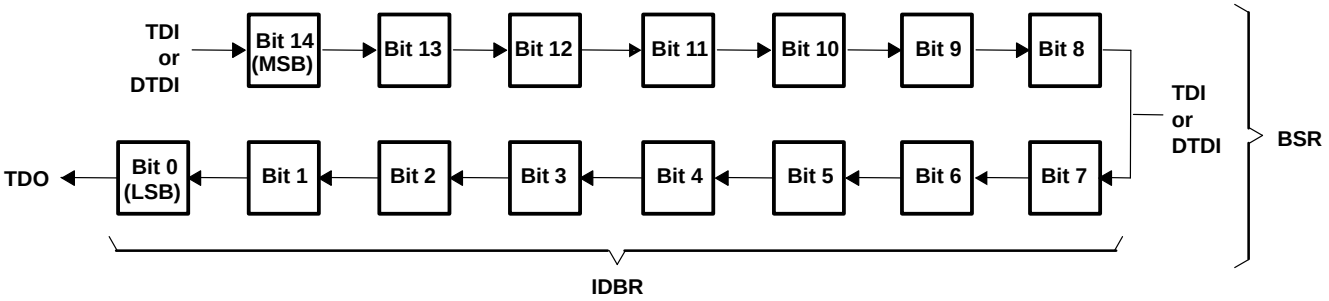


Figure 5. Boundary-Scan Register Bits and Order of Scan

bypass register description

The bypass register (BR) is a 1-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8999 from the primary scan path when it is not needed for the current test operation or other function of the PBC. A selected secondary scan path remains active in the primary scan path as described in the data flow description. At power up, the BR is placed in the scan path. Figure 6 shows the order of scan for the bypass register.

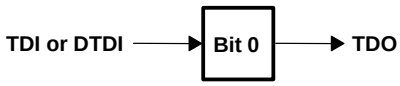


Figure 6. Bypass-Register Bit and Order of Scan

counter register description

The counter register (CNTR) is an 8-bit serial register and an associated 8-bit parallel-load up/down counter. A reset operation forces all bits of the shift register to logic 0 but does not affect the counter. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out via the shift register. The CNTR can be used to count events occurring on the secondary scan path(s) using DCI as a counter clock and can output interrupt signals via DCO when the count has reached its end value.

An internal signal, $\overline{CE}$, is generated as a logic 0 when the count reaches its end value (i.e., 00000000 for count down, 11111111 for count up). For any other count value, $\overline{CE}$ is a logic 1. Many of the features of the CNTR are configured by a bit in the CTLR, including:

- Count direction up or down (control register bit 12; reset condition count up)
- Stop counting upon counting down to 00000000 (control register bit 11; reset condition = do not latch on zero)
- Output $\overline{CE}$ signals at DCO (control register bits 8 and 9; reset condition = do not output $\overline{CE}$ at DCO)
- Edge of DCI on which to trigger (control register bit 4, reset condition = positive edge)

Figure 7 shows the order of scan for the CNTR.

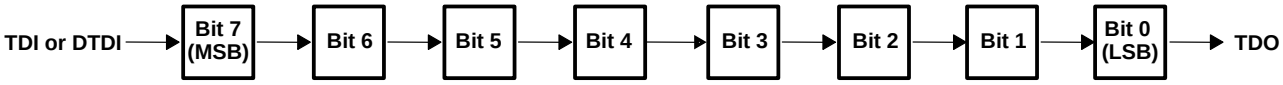


Figure 7. Counter-Register Bits and Order of Scan

enabling a remote bus controller

Bit 1 in the control register allows a remote bus controller to control parts of the ’ACT8999. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The RTP operates according to the same state diagram as the primary test port but only has access to the select register. Operation of the RTP is synchronous to TCK. OTMS is the RTP mode-select pin.

The RTP contains an 8-bit instruction register. Data is shifted in via DTDI and shifted out via DTDO. As shown in Table 10, only one instruction selects something other than the bypass register to be included in the scan path. When SCANSEL is executed, the select register is placed between DTDI and DTDO. The function of the select register and the decoding of the select register bits by the TMS circuit is identical, regardless of which test port accesses the register.

Table 10. Remote-Test-Port Instruction-Register Opcodes

BINARY CODE BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
01111110	SCANSEL	Select-register scan	Select
All other	BYPASS	Bypass scan	Bypass

An internal error signal ($\overline{\text{RSRERR}}$) is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the $\overline{\text{RSRERR}}$ is active and the remote TAP enters the Pause-DR state. The function table for $\overline{\text{RSRERR}}$ is shown in Table 11.

Table 11. $\overline{\text{RSRERR}}$ Function Table

SELECT REGISTER BITS								$\overline{\text{RSRERR}}$	MCO†
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
0	X	0	X	0	X	0	X	1	MCI
1	X	0	X	0	X	0	X	1	MCI
0	X	1	X	0	X	0	X	1	MCI
0	X	0	X	1	X	0	X	1	MCI
0	X	0	X	0	X	1	X	1	MCI
1	X	1	X	X	X	X	X	0	L
1	X	X	X	1	X	X	X	0	L
1	X	X	X	X	X	1	X	0	L
X	X	1	X	1	X	X	X	0	L
X	X	1	X	X	X	1	X	0	L
X	X	X	X	1	X	1	X	0	L

† This table is valid only when the remote TAP is in the Pause-DR state. Under any other condition, MCO = MCI.

The RTP does not have access to the control register, so it cannot disable itself. The PBC must reset bit 1 in the control register to return control of the select register to the primary test port.

data flow description

The direction of serial data flow in the ’ACT8999 is dependent on the current instruction. Figure 8 shows the data flow for the different operating modes of the device. When a secondary scan path is selected, the ’ACT8999 adds one bit of delay from TDI to DTDO.

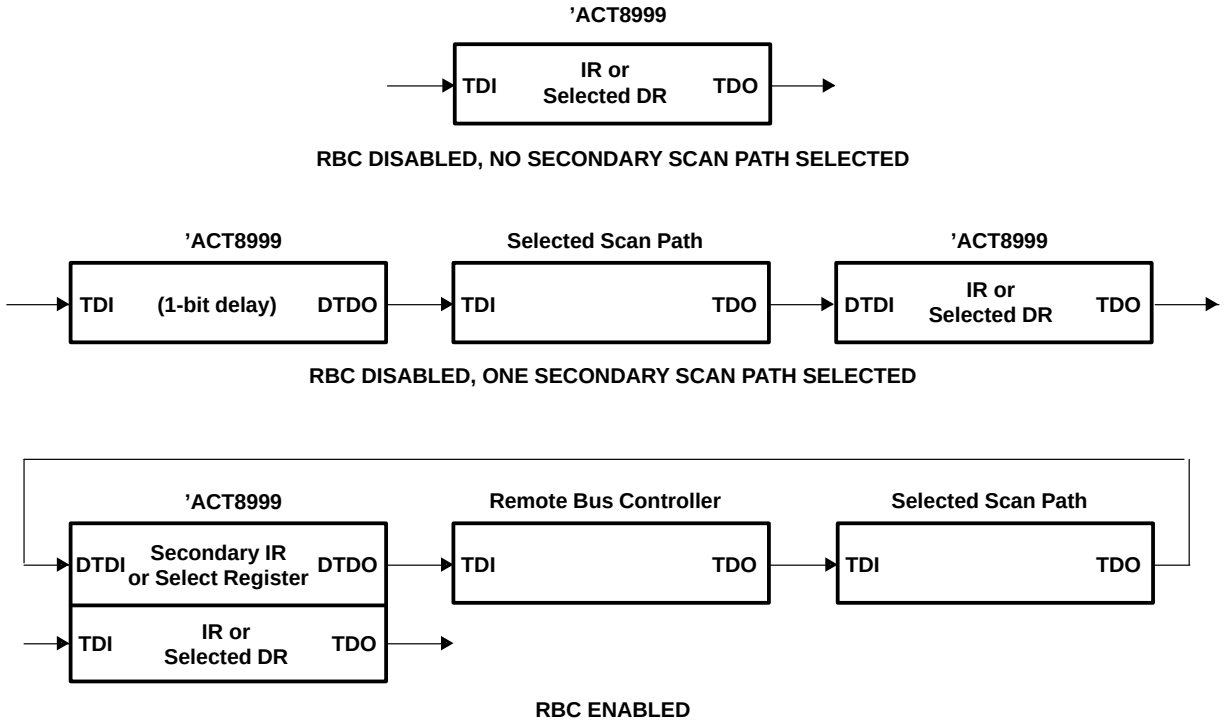


Figure 8. Data Flow in the ’ACT8999

bus-communication protocol

The 8-bit identification bus [ID(1–8)] allows data transfer between a PBC and an RBC. Control register bit 2 configures the ’ACT8999 to transmit or receive command and test data via the IDBR. The DCI, DCO, MCI, and MCO pins are used to signal the PBC and RBC(s) that a data transfer is required. The ’ACT8999 can accommodate either local or global handshake protocol, depending on the number of DCO inputs that the PBC can accommodate.

Figure 9 shows a protocol for local communication between the PBC and an RBC. In this mode, communication is initiated by the PBC by driving the MCI input of the ’ACT8999 to a low level. MCI is buffered and output on MCO, which notifies the RBC that control of a scan path is to be relinquished. Prior to activating the MCI signal, the PBC scans the value 00000000 into the IDBR and enables the output buffers of ID(1–8). When the RBC recognizes that MCO has gone low, it samples the ID bus and looks for the 00000000 value to verify that the PBC is going to issue further commands. Upon verifying the value on the ID bus, the RBC drives DCI low, which is buffered and output via DCO. (In this example, DCI is configured as noninverting and DCO is configured as active low). When the PBC sees that DCO is active, it takes MCI high, forcing MCO high. When the RBC sees that MCO is high, it takes DCO high (inactive) completing one handshake cycle. A similar operation can ensue when the RBC initiates communication with the PBC as shown in Figure 9. Commands and test data can be exchanged between two bus controllers via the ID bus.

Figure 10 shows one way of using the ID bus to interface a PBC to multiple RBCs. The timing is similar to the local communication example in Figure 9, except that the PBC waits for all RBCs to acknowledge transmissions before switching MCI.

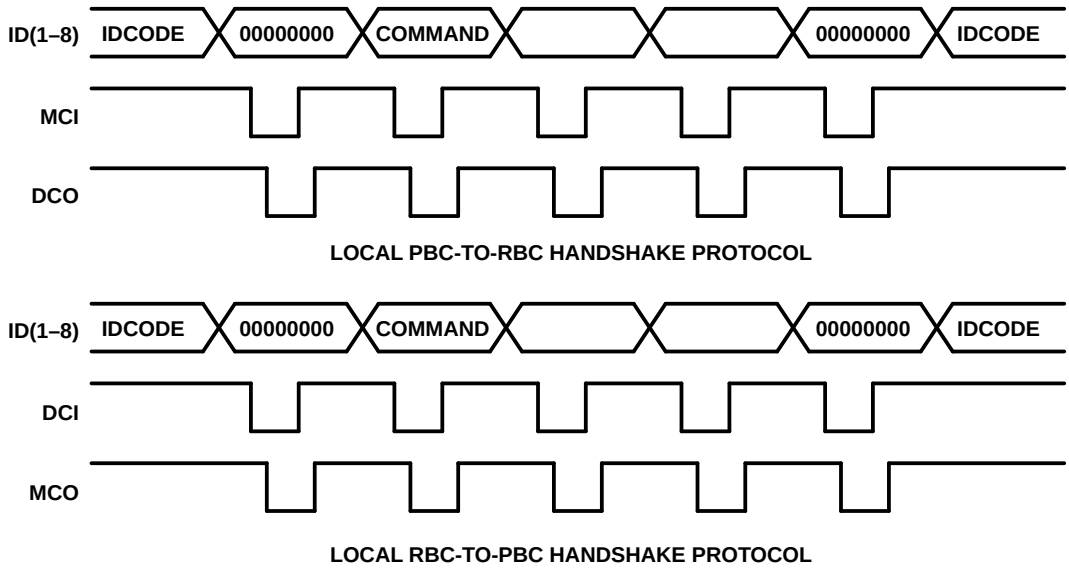


Figure 9. Local Bus-Communication Protocol

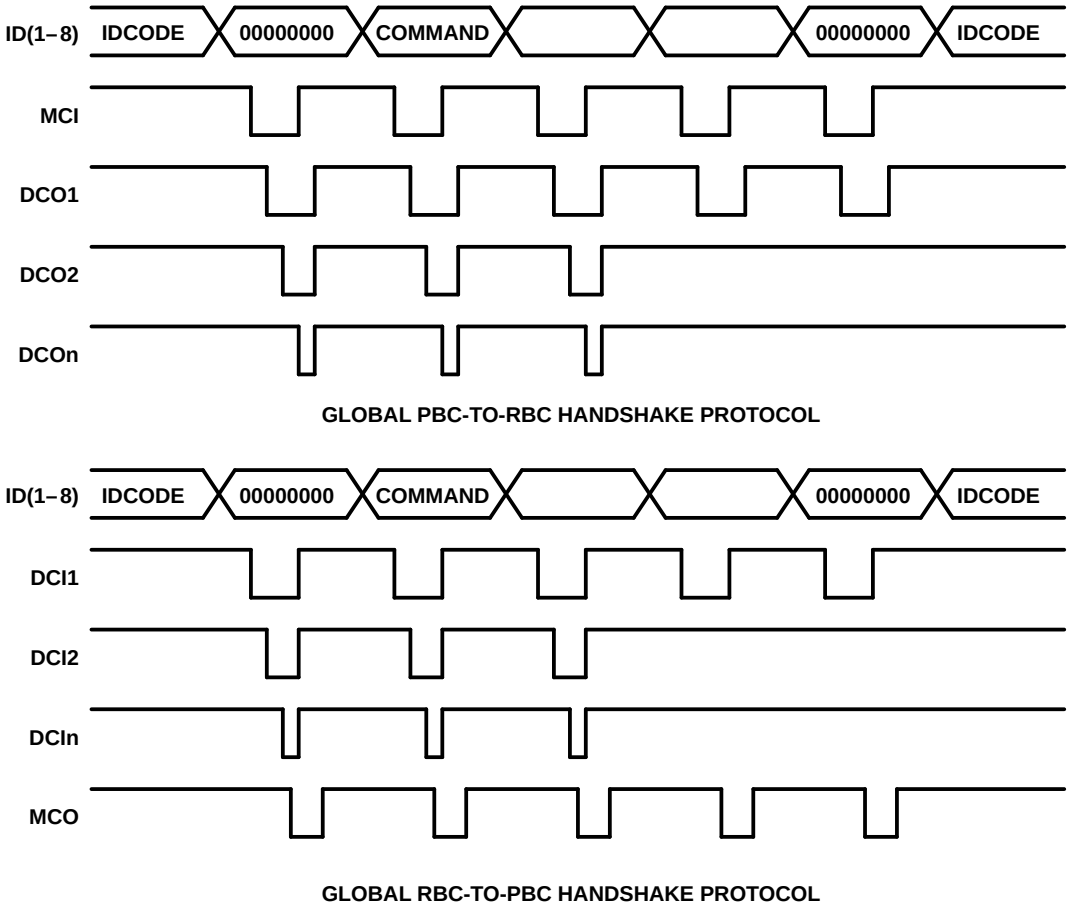


Figure 10. Global Bus-Communication Protocol

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage rating may be exceeded if the input and output clamp-current rating are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

recommended operating conditions

			SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	ID(1–8)		–1.5		–2	mA
		TDO, DTDO, MCO		–7		–10	
		DTMS(1–4), DCO (3 state), $\overline{\text{DTRST}}$, DTCK		–11		–16	
I_{OL}	Low-level output current	ID(1–8)		1.5		2	mA
		TDO, DTDO, MCO		7		10	
		DTMS(1–4), DCO (3 state or open drain)		11		16	
		$\overline{\text{DTRST}}$		16		24	
		DTCK		32		48	
T_A	Operating free-air temperature		–55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54ACT8999		SN74ACT8999			UNIT
				MIN	MAX	MIN	TYP†	MAX	
V_{OH}	ID(1–8)	I_{OH} = –1.5 mA	4.5 V	3.6					V
		I_{OH} = –2 mA	4.5 V			3.7			
	TDO, DTDO, MCO	I_{OH} = –7 mA	4.5 V	3.6					
		I_{OH} = –10 mA	4.5 V			3.7			
	DTMS(1–4), DCO (3 state), $\overline{\text{DTRST}}$, DTCK	I_{OH} = –11 mA	4.5 V	3.6					
		I_{OH} = –16 mA	4.5 V			3.7			
V_{OL}	ID(1–8)	I_{OL} = 1.5 mA	4.5 V		0.5				V
		I_{OL} = 2 mA	4.5 V					0.5	
	TDO, DTDO, MCO	I_{OL} = 7 mA	4.5 V		0.5				
		I_{OL} = 10 mA	4.5 V					0.5	
	DTMS(1–4), DCO (3 state or open drain)	I_{OL} = 11 mA	4.5 V		0.5				
		I_{OL} = 16 mA	4.5 V					0.5	
	$\overline{\text{DTRST}}$	I_{OL} = 16 mA	4.5 V		0.5				
		I_{OL} = 24 mA	4.5 V					0.5	
	DTCK	I_{OL} = 32 mA	4.5 V		0.5				
		I_{OL} = 48 mA	4.5 V					0.5	
I_{OZ}‡	ID(1–8), DTDO, DTMS(1–4), DCO, DTCK	V_O = V_{CC} or GND	5.5 V		±10			±5	µA
I_{OH}	DCO (open drain)	V_O = V_{CC}	5.5 V		20			10	µA
I_I	MCI, DCI, TCK	V_I = V_{CC} or GND	5.5 V		±1			±1	µA
	TDI, DTDI, TMS, OTMS, $\overline{\text{TRST}}$	V_I = V_{CC}	5.5 V		±1			±1	
		V_I = GND	5.5 V	–0.1	–20	–0.1	–0.1	–20	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V		100			100	µA
ΔI_{CC}§		One input at V_I = 3.4 V, Other inputs at V_{CC} or GND	5.5 V		1			1	mA
C_i		V_I = V_{CC} or GND					6		pF
C_{io}		V_O = V_{CC} or GND					15		pF
C_o	MCI, DCI, TCK	V_O = V_{CC} or GND					15		pF
C_o	DCO	V_O = V_{CC} or GND					10		pF

† Typical values are at V_{CC} = 5 V.
‡ For I/O, the parameter I_{OZ} includes the input-leakage current. For DCO, the parameter I_{OZ} includes the open-drain output-leakage current.
§ This is the increase in supply current for each input being driven at TTL levels rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12)

			SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	20	0	20	MHz
		DCI (count mode)	0	20	0	20	
t_w	Pulse duration	TCK high or low	16		16		ns
		DCI high or low (count mode)	9		9		
		$\overline{\text{TRST}}$ low	10		10		
t_{su}	Setup time	TMS before TCK↑	9		9		ns
		OTMS before TCK↑	12		12		
		TDI before TCK↑	11		11		
		DTDI before TCK↑	5		5		
		MCI before TCK↑	5		5		
		DCI before TCK↑	9		9		
		Any ID before TCK↑	3		3		
t_h	Hold time	TMS after TCK↑	2		2		ns
		OTMS after TCK↑	2		2		
		TDI after TCK↑	4		4		
		DTDI after TCK↑	4		4		
		MCI after TCK↑	5		5		
		DCI after TCK↑	5		5		
		Any ID after TCK↑	5		5		
t_d	Delay time	Power up to TCK↑	100*		100		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

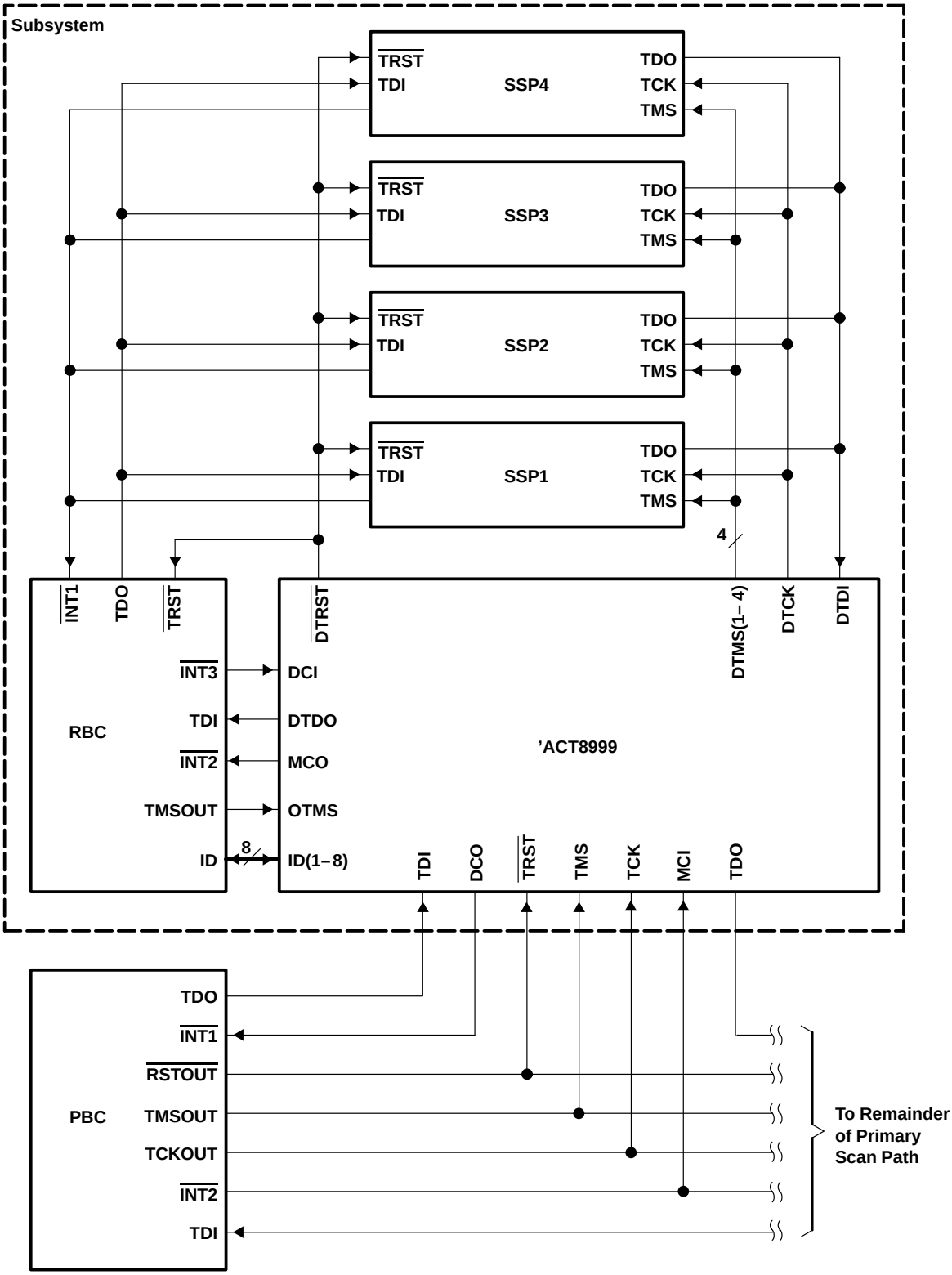
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	TCK		20		20		MHz
	DCI (count mode)		20		20		
t_{PLH}	TCK	DTCK	3	16	3	14	ns
t_{PHL}			3	19	3	17	
t_{PLH}	TCK↓	TDO	7	30	7	28	ns
t_{PHL}			7	29	8	27	
t_{PLH}	TCK↓	DTDO	7	31	7	29	ns
t_{PHL}			7	29	8	27	
t_{PLH}	TCK↓	Any DTMS	11	40	11	38	ns
t_{PHL}			11	37	11	35	
t_{PLH}	TCK↓	$\overline{\text{DTRST}}$	9	35	10	33	ns
t_{PHL}			9	35	10	33	
t_{PLH}	TCK↓	Any ID	20	64	22	61	ns
t_{PHL}			22	65	24	62	
t_{PLH}	TCK↓	MCO	9	34	9	32	ns
t_{PHL}			9	31	9	29	
t_{PLH}	TCK↓	DCO (open drain)	14	45	18	42	ns
		DCO (3 state)	10	40	11	38	
t_{PHL}		DCO (open drain)	10	39	11	37	
		DCO (3 state)	10	37	11	35	
t_{PLH}	TMS	Any DTMS	5	22	6	20	ns
t_{PHL}			4	23	5	21	
t_{PLH}	OTMS	Any DTMS	5	22	6	20	ns
t_{PHL}			4	23	5	21	
t_{PLH}	MCI	MCO	7	26	8	24	ns
t_{PHL}			6	25	7	23	
t_{PLH}	DCI	DCO (open drain)	8	32	9	30	ns
		DCO (3 state)	8	30	10	28	
t_{PHL}		DCO (open drain)	8	34	9	32	
		DCO (3 state)	8	30	9	28	
t_{PLH}	$\overline{\text{TRST}}$	$\overline{\text{DTRST}}$	4	20	5	18	ns
t_{PHL}			5	25	6	23	

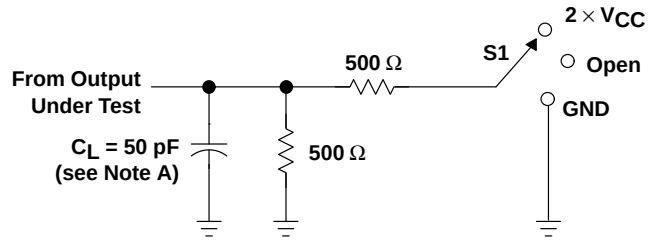
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 11 and 12) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8999		SN74ACT8999		UNIT
			MIN	MAX	MIN	MAX	
t_{PHZ}	TCK↓	TDO	3	17	4	15	ns
t_{PLZ}			3	18	5	16	
t_{PHZ}	TCK↓	DTDO	3	18	3	16	ns
t_{PLZ}			7	26	7	24	
t_{PHZ}	TCK↓	Any DTMS	7	26	8	24	ns
t_{PLZ}			7	28	7	26	
t_{PHZ}	TCK↓	DCO	9	28	12	26	ns
t_{PLZ}			7	31	7	29	
t_{PHZ}	TCK↓	Any ID	12	38	14	36	ns
t_{PLZ}			9	34	10	32	
t_{PHZ}	DCI	Any ID	8	27	9	25	ns
t_{PLZ}			10	33	15	31	
t_{PZH}	TCK↓	TDO	9	35	9	33	ns
t_{PZL}			9	36	11	34	
t_{PZH}	TCK↓	DTDO	10	39	11	37	ns
t_{PZL}			10	40	12	38	
t_{PZH}	TCK↓	Any DTMS	8	34	9	32	ns
t_{PZL}			8	34	9	32	
t_{PZH}	TCK↓	DCO	12	46	14	43	ns
t_{PZL}			10	38	11	36	
t_{PZH}	TCK↓	Any ID	20	73	22	70	ns
t_{PZL}			22	58	24	65	
t_{PZH}	MCI	Any ID	18	65	20	62	ns
t_{PZL}			20	62	20	59	

APPLICATION INFORMATION

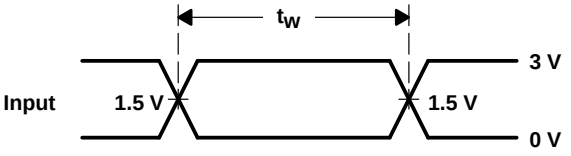


PARAMETER MEASUREMENT INFORMATION

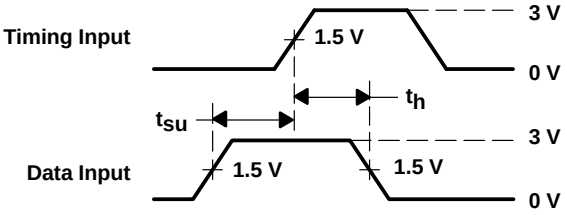


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

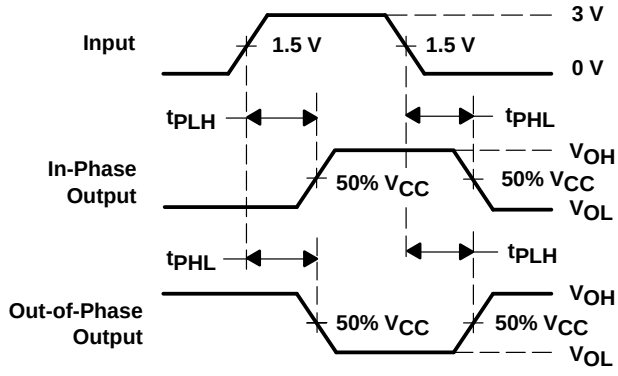
LOAD CIRCUIT



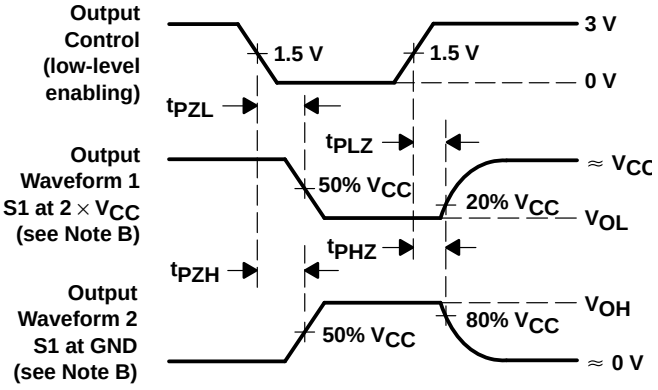
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

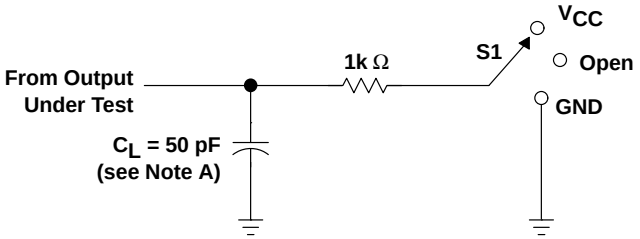


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one input transition per measurement.

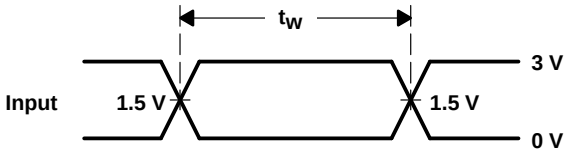
Figure 11. Load Circuit and Voltage Waveforms (For All Pins Except ID-Bus Pins)

PARAMETER MEASUREMENT INFORMATION

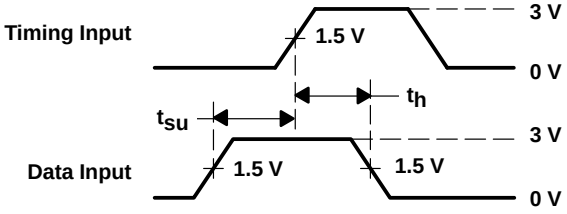


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{CC} GND

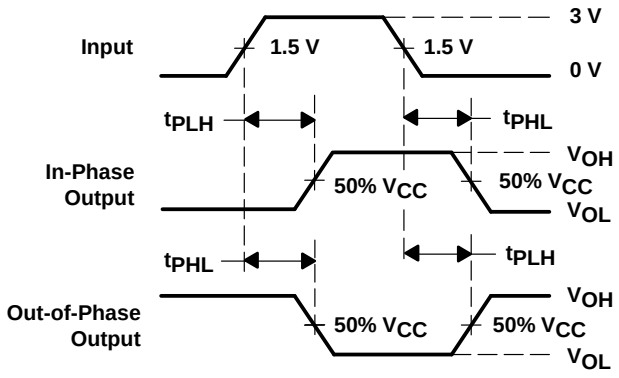
LOAD CIRCUIT



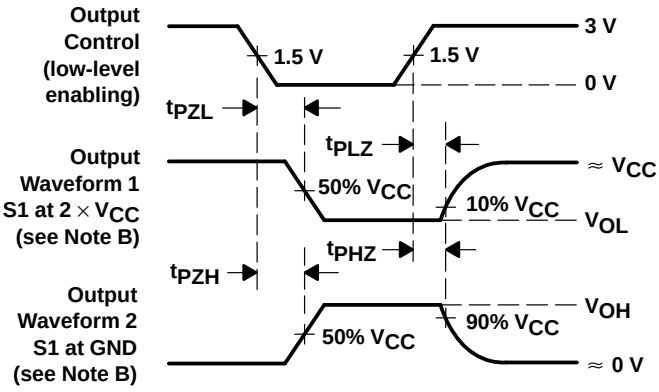
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity may be either high-to-low-to-high or a low-to-high-to-low.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 12. Load Circuit and Voltage Waveforms (ID-Bus Pins)

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