- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- 1024 Words × 18 Bits
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7884

- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High-Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) and Space-Saving 80-Pin Thin Quad Flat (PN) Packages





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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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(TOP VIEW) VCC 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 NC **D** 1 60 VCC GND 2 59 VCC GND 3 58 **[** NC Q16 🛛 4 Q3 57 Q17 5 Q2 56 6 55 GND Vcc OR 17 54 🔲 Q1 GND 8 53 🗌 Q0 VCC 9 52 Vcc RESET 10 10 51 HF 50 OE 11 IR 49 RDEN2 12 GND RDEN1 13 48 ∏ GND RDCLK 14 47 AF/AE GND 15 46 🔲 Vcc D17 16 45 🗌 WRTEN2 D16 17 44 WRTEN1 D15 1 18 43 **[** WRTCLK 19 NC GND 42 NC 20 41 NC 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

PN PACKAGE

NC - No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024×18 -bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts or requests) to their respective system clock.

The SN74ACT7811 is characterized for operation from 0°C to 70°C.



logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the FN package.



functional block diagram





Terminal Functions

| NAME NO. Amost-full/almost-empty/flag. The AF/AE boundary is defined by the almost-full/almost value (X). This value can be programmed during reset or the default value of 256 can be is high when the FIPO contains (X + 1) or less words or (1025 - X) or more words. AF/A the FIPO contains by the FIPO contains (X + 1) or less words or (1025 - X) or more words. AF/A the FIPO contains between (X + 2) and (1024 - X) words. AF/AE 33 O User:defined X AF/AE 33 O User:defined X Step 1: Take DAF from high to low. Step 2: If RESET is not already low, take RESET low. Step 2: If RESET is not already low, take RESET low. Step 3: Step 4: To readma AF/AE using the default value of X = 256, hold DAF high during the default value of X = 256, hold DAF high during the almost-full/almost-empty offset value (X). With DAF held low, allow pulses on RESE AF/AE flag using X. D0-D17 26-19, 17, 15-7 I Dationputs full/almost-empty offset value (X). With DAF held low, allow pulses on RESE AF/AE flag using X. IR 35 O Half-full/ga_IR is high when the FIFO contains 51 or more words and is low when i almost-full/almost-empty offset value (X) on a high-to-low transition of the DAF. IR 35 O of less words. ID=D17 26-19, 17, 15-7 I Data inputs for 18-bitwide data to be stored in the memory. Dat | TE | ERMINAL [†] | | DECODISTICAL | | | | |
|--|----------|--------------------------------|-----|---|--|--|--|--|
| AF/AE 33 O value (X). This value can be programmed during reset or the default value of 256 can br is high when the FIFO contains (X + 1) or less words or (1026 – X) or more words. AF/A the FIFO contains between (X + 2) and (1024 – X) words. Programming procedure for AF/AE – The almost-ful/almost-empty files is programme reset cycle. The almost-ful/almost-empty offset value (X) is either a user-defined value of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X AF/AE 33 O Step 1: Take DAF from high to low. Step 2: If RESET is not already low, take RESET low. Step 2: With DAF held low, take RESET low. Step 2: With DAF held low, take RESET low. Default X To redefine AF/AE using the default value of X = 256, hold DAF high during th Define almost full/innost-empty offset value (X). With DAF held low, a low pulse on RESE AF/AE flag using X. D0-D17 26-19, 17, 15-7 I Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0-D6 a AF/AE flag using X. IR 36 O Half-full flag. HF is high when the FIFO is not full and low when the device is full. D is driven how on the rising edge of the second WRTCLK pulse after the first valie read. OE 2 I Output-ready flag. R is high when the FIFO is not empty and tow when it is empty. GR set store on the rising edge of the second WRTCLK pulse after the first valie read. OL 0 Output-ready flag. R is high when the FIFO is not empty and tow when it is empty. GR is store on the rising edge of the second WRTCLK pulse after the first valie read. | NAME NO. | | 1/0 | DESCRIPTION | | | | |
| Number Obs Step 1: Take DAF from high to low. Step 2: If RESET is not already low, take RESET low. Step 3: With DAF held low, take RESET high. This defines the AF/AE using Step 4: To retain the current offset for the next reset, keep DAF low. Default X To redefine AF/AE using the default value of X = 256, hold DAF high during the almost full. The high-to-low transition of DAF stores the binary value of data almost-full/almost-empty offset value (X). With DAF held low, a low pulse on RESE AF/AE flag using X. D0-D17 26-19, 17, 15-7 I Dafa Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0-D8 a almost-full/almost-empty offset value (X) on a high-to-low transition of the DAF. HF 36 0 IR 35 0 IR 35 0 IR 35 0 IR 36 0 IR 35 0 IR 0 0 IR 0 0 IR 35 0 IR 0 0 IR 0 0 IR 0 0 IR 0 0 IR< | | | | Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default | | | | |
| DAF 27 I almost-full/almost-empty offset value (X). With DAF held low, a low pulse on RESE AF/AE flag using X. D0-D17 26-19, 17, 15-7 I Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0-D8 a almost-full/almost-empty offset value (X) on a high-to-low transition of the DAF. HF 36 0 Half-full flag. HF is high when the FIFO contains 513 or more words and is low when i or less words. IR 35 0 Half-full flag. HF is high when the FIFO is not full and low when the device is full. Dri is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on to f the second WRTCLK pulse after the FIFO is filled and IR IR is driven high on the second WRTCLK pulse after the first valid read. OE 2 I Output enable. The data-out (Q0-Q17) outputs are in the high-impedance state when must be high before the rising edge of RDCLK to read a word from memory. OR 66 0 Output enable. The data-out (Q0-Q17) outputs are in the high-impedance state when must be high before the rising edge of RDCLK to read a word from memory. Qu-Q17 38-39, 41-42, 44, Q0-Q17 0 0 A6-47, 49-50, 52-55, 55-56, 58-59, 61, 63-64 0 0 Data outputs. The first data word to be loaded into the FIFO. Sin word to Q0-Q17 on the first mata word is written into the FIFO. OR is also driven synchronizing clock for all data transfers out of the FIFO. OR is also driven synch respect th RDCLK pulse after the first word is wr | AF/AE | 33 | 0 | Step 1: Take DAF from high to low. Step 2: If RESET is not already low, take RESET low. Step 3: With DAF held low, take RESET high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep DAF low. | | | | |
| D0-D17 26-19, 17, 15-7 1 almost-full/almost-empty offset value (X) on a high-to-low transition of the DAF. HF 36 0 Half-full flag, HF is high when the FIFO contains 513 or more words and is low when i or less words. IR 35 0 Input-ready flag, IR is high when the FIFO is not full and low when the device is full. Du is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on to the second WRTCLK pulse after the first valid read. OE 2 1 Output enable. The data-out (Q0-Q17) outputs are in the high-impedance state when must be high before the rising edge of RDCLK to read a word from memory. OR 66 0 Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. OR 66 0 Output-ready flag. OR is high when the FIFO is more to Q0-Q17 or third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low edge of the first RDCLK pulse after the list word is written into the FIFO. OR is set low edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD OE, and the OR are high. RDCLK 5 1 Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE and RDEN2 as the OR are high. RDCLK 5 1 Read enable. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN1 and RDEN2 are not used to read the | DAF | 27 | I | Define almost full. The high-to-low transition of \overline{DAF} stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With \overline{DAF} held low, a low pulse on \overline{RESET} defines the AF/AE flag using X. | | | | |
| HF 36 O or less words. IR 35 O or less words. IR 35 O Input-ready flag. IR is high when the FIFO is not full and low when the device is full. Duis driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on to of the second WRTCLK pulse after the FIFO is filled and IR IR is driven high on the second WRTCLK pulse after the first valid read. OE 2 I Output enable. The data-out (QO-Q17) outputs are in the high-impedance state when must be high before the rising edge of RDCLK to read a word from memory. OR 66 O Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the risin third RDCLK pulse to occur after the first word is read. Q0-Q17 38-39, 41-42, 44, 46-47, 49-50, 52-53, 55-56, 58-59, 61, 63-64 O O OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the risin the RDCLK pulse after the last word is read. Q0-Q17 46-47, 49-50, 52-53, 55-56, 58-59, 61, 63-64 O O Data outputs. The first data word to be loaded into the FIFO is moved to Q0-Q17 on to of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD OE, and the OR are high. RDELK 5 I Read clock. Data is read out of me | D0-D17 | 26–19, 17, 15–7 | I | Data inputs for 18-bit-wide data to be stored in the memory. Data lines $D0-D8$ also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the \overline{DAF} . | | | | |
| IR 35 O is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on to of the second WRTCLK pulse after RESET goes high. After the FIFO is filled and IR IR is driven high on the second WRTCLK pulse after RESET goes high. After the FIFO is filled and IR IR is driven high on the second WRTCLK pulse after the first valid read. OE 2 I Output enable. The data-out (Q0-Q17) outputs are in the high-impedance state when must be high before the rising edge of RDCLK to read a word from memory. OR 66 Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the first word is written into the FIFO. OR is set low or dege of the first DCLK pulse to occur after the last word is read. Q0-Q17 38-39, 41-42, 44, 46-47, 49-50, 52-53, 55-56, 58-59, 61, 63-64 Data outputs. The first data word to be loaded into the FIFO is moved to Q0-Q17 on to of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD DE, and the OR are high. RDCLK 5 I Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE and RDEN2 control inputs are high. RDCLK is a free-running clock and funct synchronizing clock for all data transfers out of the FIFO. OR is also driven synch respect to RDCLK. RDEN1, 4 I Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read in memory of memory. RDEN1 and RDEN2 are not used to read the first w | HF | 36 | 0 | Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or less words. | | | | |
| OE 2 1 must be high before the rising edge of RDCLK to read a word from memory. OR 66 O Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the risin third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low edge of the first RDCLK pulse after the last word is read. Q0-Q17 38-39, 41-42, 44, 46-47, 49-50, 52-53, 55-56, 58-59, 61, 63-64 O Data outputs. The first data word to be loaded into the FIFO is moved to Q0-Q17 on the rising edge of RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD OE, and the OR are high. RDCLK 5 1 Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE and RDEN2 control inputs are high. RDCLK is a free-running clock and funct synchronizing clock for all data transfers out of the FIFO. OR is also driven synch respect to RDCLK. RDEN1, 4 1 Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to re of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN1 and RFAE is high. The FIFO must be reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon powerup. With DAF at a low of th | IR | 35 | ο | Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after RESET goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read. | | | | |
| OR 66 O OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low edge of the first RDCLK pulse after the last word is read. Q0-Q17 38-39, 41-42, 44, 46-47, 49-50, 52-53, 55-56, 58-59, 61, 63-64 O Data outputs. The first data word to be loaded into the FIFO is moved to Q0-Q17 on the of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD OE, and the OR are high. RDCLK 5 I Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE and RDEN2 control inputs are high. RDCLK is a free-running clock and function synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronizing clock for all data transfers out of the first word stored in memory respect to RDCLK. RDEN1, 4 I Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read free memory. RDEN1 and RDEN2 are not used to read the first word stored in memory WRTCLK cycles. This ensures that the internal read and write pointers are reset and IR are low and AF/AE is high. The FIFO must be reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset upon power up. With DAF at a low of the reset | OE | 2 | I | Output enable. The data-out $(Q0-Q17)$ outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory. | | | | |
| Q0-Q17 46-47, 49-50, 52-53, 55-56, 58-56, 58-59, 61, 63-64 O of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 affect this operation. Following data is unloaded on the rising edge of RDCLK when RD OE, and the OR are high. RDCLK 5 I Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE and RDEN2 control inputs are high. RDCLK is a free-running clock and function synchronizing clock for all data transfers out of the FIFO. OR is also driven synch respect to RDCLK. RDEN1, 4 I Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to re of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN2 3 I Read enable. RDEN1 and RDEN2 are not used to read the first word stored in memory. RESET 1 Reset is accomplished by taking RESET low and generating a minimum of four WRTCLK cycles. This ensures that the internal read and write pointers are reset and IR are low and AF/AE is high. The FIFO must be reset upon power up. With DAF at a low | OR | 66 | ο | Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read. | | | | |
| RDCLK 5 I and RDEN2 control inputs are high. RDCLK is a free-running clock and fund synchronizing clock for all data transfers out of the FIFO. OR is also driven synchrospect to RDCLK. RDEN1, 4 I Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to re of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN2 3 I Read enable. RDEN1 and RDEN2 are not used to read the first word stored in memory. RDEN1 A reset is accomplished by taking RESET low and generating a minimum of four WRTCLK cycles. This ensures that the internal read and write pointers are reset and IR are low and AF/AE is high. The FIFO must be reset upon power up. With DAF at a low | Q0-Q17 | 46–47, 49–50, 52–53, 55–56, | ο | Data outputs. The first data word to be loaded into the FIFO is moved to $Q0-Q17$ on the rising edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and the OR are high. | | | | |
| RDEN2 3 of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. A reset is accomplished by taking RESET low and generating a minimum of four WRTCLK cycles. This ensures that the internal read and write pointers are reset and IR are low and AF/AE is high. The FIFO must be reset upon power up. With DAF at a low | RDCLK | 5 | I | Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE, and RDEN1 and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK. | | | | |
| WRTCLK cycles. This ensures that the internal read and write pointers are reset and IR are low and AF/AE is high. The FIFO must be reset upon power up. With DAF at a lo | , | | Ι | Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory. | | | | |
| | RESET | 1 | I | A reset is accomplished by taking $\overrightarrow{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overrightarrow{\text{DAF}}$ at a low level, a low pulse on $\overrightarrow{\text{RESET}}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overrightarrow{\text{DAF}}$ at a high level, a low-level pulse on $\overrightarrow{\text{RESET}}$ defines the AF/AE status of X = 256. | | | | |

[†] Terminals listed are for the FN package.

Terminal Functions (Continued)

| TERMINAL [†] | | 1/0 | DESCRIPTION | | | | |
|-----------------------|----------|-----|--|--|--|--|--|
| NAME | NO. | 1/0 | DESCRIPTION | | | | |
| WRTCLK | 29 | I | Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK. | | | | |
| WRTEN1, WRTEN2 | 30 31 | I | Write enables. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X). | | | | |

[†] Terminals listed are for the FN package.



[†]X is the binary value of D0–D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X





Figure 2. Reset Cycle: Define AF/AE Using the Default Value





Figure 3. Write Cycle



1

0







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| Supply voltage range, V _{CC} | |
|--|----------------|
| Input voltage, V _I | |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, T _A | 0°C to 70°C |
| Storage temperature range, T _{stg} | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|------|
| VCC | Supply voltage | 4.5 | 5.5 | V |
| VIH | High-level input voltage | 2 | | V |
| VIL | Low-level input voltage | | 0.8 | V |
| ЮН | High-level output current | | -8 | mA |
| I _{OL} | Low-level output current | | 16 | mA |
| Т _А | Operating free-air temperature | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | | |
|------------------------------|--|---------------------------------|-----|---|-----|----|--|
| VOH | V _{CC} = 4.5 V, | I _{OH} = – 8 mA | 2.4 | | | V | |
| VOL | V _{CC} = 4.5 V, | I _{OL} = 16 mA | | | 0.5 | V | |
| Ц | V _{CC} = 5.5 V, | VI =VCC or 0 V | | | ±5 | μA | |
| I _{OZ} | V _{CC} = 5.5 V, | VO =VCC or 0 V | | | ±5 | μA | |
| | $V_{I} = V_{CC} - 0.2 V \text{ or } 0 V$ | | | | 400 | μA | |
| ^I CC [§] | One input at 3.4 V, | Other inputs at V_{CC} or GND | | | 1 | mA | |
| Ci | VI = 0 V, f = 1 MHz | | | 4 | | pF | |
| Co | V _O = 0 V, f = 1 MHz | | | 8 | | pF | |

[‡] All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}$ C.

§ I_{CC} tested with outputs open



| | | | ÁCT78 | 811-15 | ÁCT78 | 811-18 | ÁCT78 | 811-20 | ÁCT78 | 811-25 | UNIT | |
|-----------------|-----------------|--|-------|--------|-------|--------|-------|--------|-------|--------|------|--|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNIT | |
| fclock | Clock frequency | | 40 | | 35 | | 28.5 | | 16.7 | | MHz | |
| | | D0-D17 high or low | 10 | | 12 | | 14 | | 20 | | | |
| | | WRTCLK high | 7 | | 8.5 | | 10 | | 17 | | | |
| | | WRTCLK low | 10 | | 11 | | 14 | | 23 | | | |
| | | RDCLK high | 7 | | 8.5 | | 10 | | 17 | | | |
| tw | Pulse duration | RDCLK low | 10 | | 11 | | 14 | | 23 | | ns | |
| vv | | DAF high | 10 | | 10 | | 10 | | 10 | | - | |
| | | WRTEN1, WRTEN2 high or low | 10 | | 10 | | 10 | | 10 | | | |
| | | OE, RDEN1, RDEN2 high or low | 10 | | 10 | | 10 | | 10 | | | |
| | | D0-D17 before WRTCLK↑ | 5 | | 5 | | 5 | | 5 | | | |
| | | WRTEN1, WRTEN2 high before WRTCLK1 | 5 | | 5 | | 5 | | 5 | | | |
| | | OE, RDEN1, RDEN2 high before RDCLK↑ | 5 | | 5 | | 5 | | 5 | | | |
| t _{su} | Setup time | Reset: RESET low before first WRTCLK and RDCLK [↑] | 7 | | 7 | | 7 | | 7 | | ns | |
| | | $\begin{array}{c} \text{Define AF/AE: D0-D8 before} \\ \overline{\text{DAF}} \downarrow \end{array}$ | 5 | | 5 | | 5 | | 5 | | | |
| | | Define AF/AE: DAF↓ before RESET↑ | 7 | | 7 | | 7 | | 7 | | | |
| | | Define AF/AE (default): DAF high before RESET↑ | 5 | | 5 | | 5 | | 5 | | | |
| | | D0-D17 after WRTCLK↑ | 1 | | 1 | | 1 | | 1 | | | |
| | | WRTEN1, WRTEN2 high after WRTCLK1 | 1 | | 1 | | 1 | | 1 | | | |
| | | OE, RDEN1, RDEN2 high after RDCLK↑ | 1 | | 1 | | 1 | | 1 | | | |
| t _h | Hold time | Reset: RESET low after fourth WRTCLK and RDCLK [↑] | 0 | | 0 | | 0 | | 0 | | ns | |
| | | Define AF/AE: D0−D8 after DAF↓ | 1 | | 1 | | 1 | | 1 | | | |
| | | Define AF/AE: DAF low after RESET↑ | 0 | | 0 | | 0 | | 0 | | | |
| | | Define AF/AE (default): DAF high after RESET↑ | 1 | | 1 | | 1 | | 1 | | | |

timing requirements (see Figures 1 through 8)

 $\ensuremath{^{+}}\xspace$ To permit the clock pulse to be utilized for reset purposes



switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

| PARAMETER | FROM (INPUT) | - | FROM (INPUT) | TO (OUTPUT) | | | | CL RL | C = 4.5 = 50 pF = 500 C = 0°C te | 2, | V, | | | UNIT |
|-------------------|---------------------|-------|-----------------|------------------|-----|-------|--------|----------|---|-------|--------|-----|--|------|
| | . , | . , | ´ΑC | :T7811- 1 | 5 | ÁCT78 | 811-18 | ÁCT78 | 311-20 | ÁCT78 | 811-25 | | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| fmax | WRTCLK or RDCLK | | 40 | | | 35 | | 28.5 | | 16.7 | | MHz | | |
| ^t pd | | A | 4 | 12 | 15 | 4 | 18 | 4 | 20 | 4 | 25 | | | |
| t _{pd} † | RDCLK↑ | Any Q | | 10.5 | | | | | | | | ns | | |
| tpd | WRTCLK↑ | IR | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | ns | | |
| tpd | RDCLK↑ | OR | 2 | | 10 | 2 | 12 | 2 | 14 | 2 | 16 | ns | | |
| | WRTCLK [↑] | | 6 | | 20 | 6 | 22 | 6 | 24 | 6 | 26 | | | |
| ^t pd | RDCLK↑ | AF/AE | 6 | | 20 | 6 | 22 | 6 | 24 | 6 | 26 | ns | | |
| ^t PLH | WRTCLK↑ | | 6 | | 19 | 6 | 21 | 6 | 23 | 6 | 25 | | | |
| ^t PHL | RDCLK↑ | HF | 6 | | 19 | 6 | 21 | 6 | 23 | 6 | 25 | ns | | |
| ^t PLH | DEOFT | AF/AE | 3 | | 19 | 3 | 21 | 3 | 23 | 3 | 25 | | | |
| ^t PHL | RESET↓ | HF | 4 | | 21 | 4 | 23 | 4 | 25 | 4 | 27 | ns | | |
| t _{en} | 05 | Amy 0 | 2 | | 11 | 2 | 11 | 2 | 11 | 2 | 11 | | | |
| ^t dis | OE | Any Q | 2 | | 14 | 2 | 14 | 2 | 14 | 2 | 14 | ns | | |

[†] This parameter is measured with $C_L = 30 \text{ pF}$ (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| | PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|---|--|-----|------|
| C _{pd} | Power dissipation capacitance per 1K bits | $C_L = 50 \text{ pF}, \text{ f} = 5 \text{ MHz}$ | 65 | pF |



TYPICAL CHARACTERISTICS



TYPICAL PROPAGATION DELAY TIME

Figure 5







calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7811 can be calculated by:

 $\mathsf{P}_{\mathsf{T}} = \mathsf{V}_{\mathsf{CC}} \times [\mathsf{I}_{\mathsf{CC}} + (\mathsf{N} \times \Delta \mathsf{I}_{\mathsf{CC}} \times \mathsf{dc})] + \Sigma \ (\mathsf{C}_{\mathsf{pd}} \times \mathsf{V}_{\mathsf{CC}}^2 \times \mathsf{f}_{\mathsf{i}}) + \Sigma \ (\mathsf{C}_{\mathsf{L}} \times \mathsf{V}_{\mathsf{CC}}^2 \times \mathsf{f}_{\mathsf{o}})$

where:

| ICC | = | power-down I _{CC} maximum |
|-----------------------|---|---|
| N | = | number of inputs driven by a TTL device |
| ΔI_{CC} | = | increase in supply current |
| dc | = | duty cycle of inputs at a TTL high level of 3.4 V |
| C _{pd} CL | = | power dissipation capacitance |
| CĽ | = | output capacitive load |
| f _i | = | data input frequency |
| f _o | = | data output frequency |



APPLICATION INFORMATION

expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

After the first data word is loaded into the FIFO, the word is unloaded and the output-ready flag (OR) output goes high after (N \times 3) read-clock (RDCLK) cycles, where N is the number of devices used in depth expansion.

After the FIFO is filled, the input-ready flag (IR) output goes low, the first word is unloaded, and the IR flag output is driven high after (N \times 2) write-clock cycles, where N is the number of devices used in depth expansion.



Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2



Figure 8. Word-Width Expansion: 1024 Words \times 36 Bits



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| PARA | IETER | R1, R2 | c∟† | S1 |
|------------------|------------------------------|--------|-------|--------|
| | ^t PZH 500 Ω 50 pF | | Open | |
| ten | ^t PZL | 500 22 | 50 pF | Closed |
| A | ^t PHZ | 500 Ω | 50 mF | Open |
| ^t dis | ^t PLZ | 500 22 | 50 pF | Closed |
| ^t pd | | 500 Ω | 50 pF | Open |

VOLTAGE WAVEFORMS

[†] Includes probe and test fixture capacitance





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