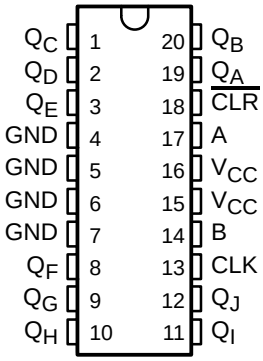
- **Inputs Are TTL-Voltage Compatible**
- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Fully Synchronous Data Transfers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74ACT11898 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	...	Q_J
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{JO}
H	↑	H	H	H	Q_{AN}		Q_{IN}
H	↑	L	X	L	Q_{AN}		Q_{IN}
H	↑	X	L	L	Q_{AN}		Q_{IN}

H = high level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{J0} = the level of Q_A, Q_B, Q_J respectively, before the indicated steady-state inputconditions were established.
Q_n, Q_{in} = the level or Q_A or Q_J before the most recent ↑ transition of the clock; indicates aone-bit shift.t

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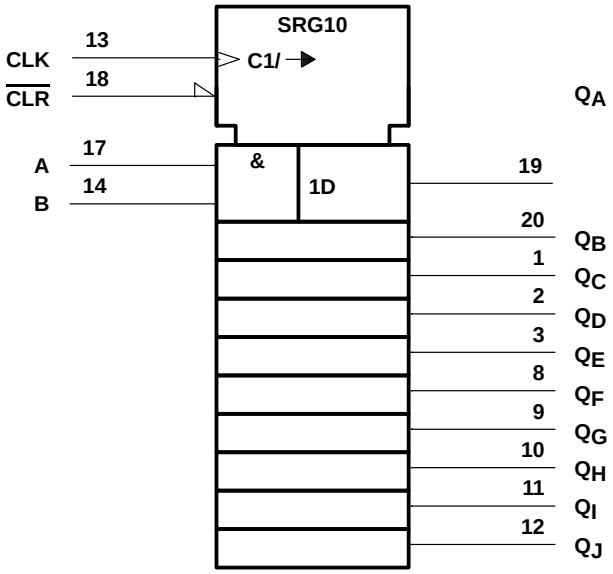
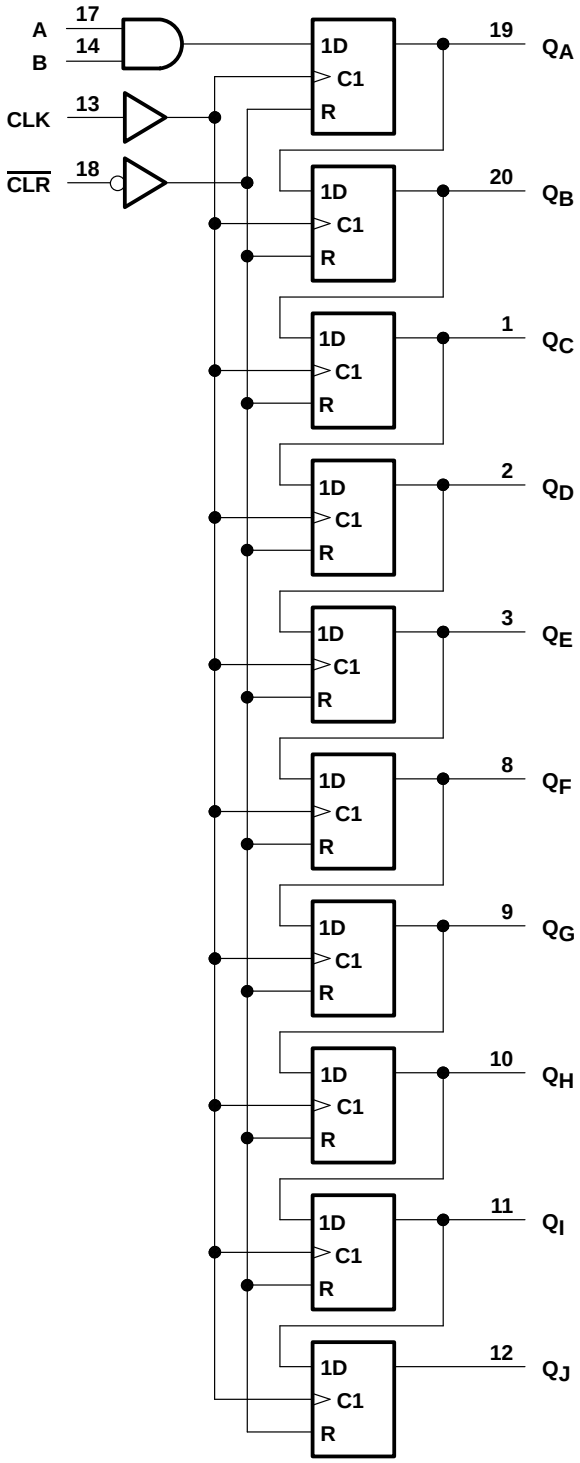
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±250 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA‡	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡	5.5 V					1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	40	0	40	ns
t_w	Pulse duration	$\overline{CLR}$ low	4.5		4.5		ns
		CLK high or low	12.5		12.5		
t_{su}	Setup time before CLK↑	Data	10		10		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time, data after CLK↑		0		0		ns

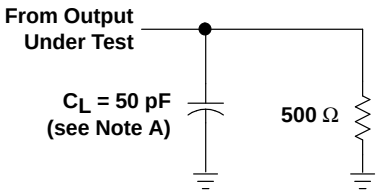
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			20	65		40		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4.6	6.7	11.1	3.8	12.1	ns
t_{PLH}	CLK	Any Q	4.1	5.5	8.8	2.7	9.7	ns
t_{PHL}			4.4	6.3	9.4	3.1	10.6	

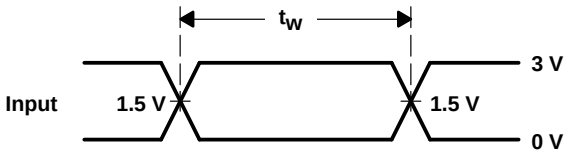
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	117	pF

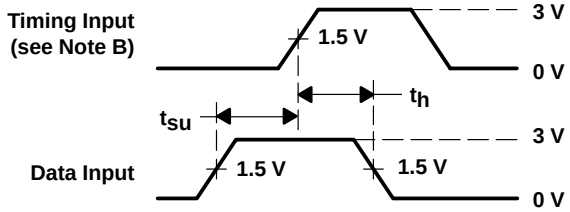
PARAMETER MEASUREMENT INFORMATION



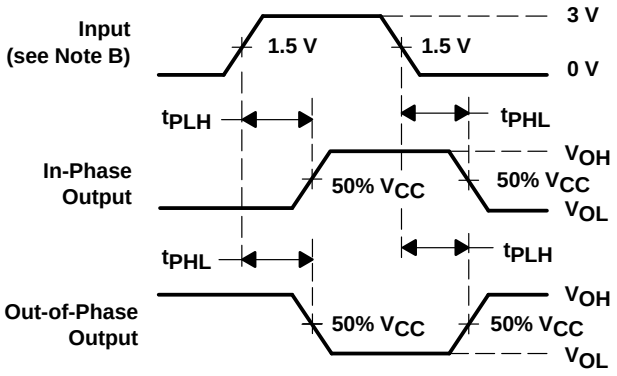
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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