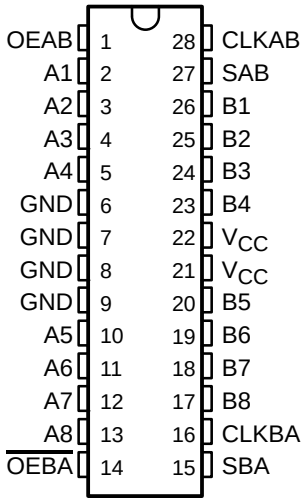
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11651.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all the other data sources to the two sets of bus lines are at high impedance, each set will remain at its last state.

The 74AC11651 is characterized for operation from –40°C to 85°C.

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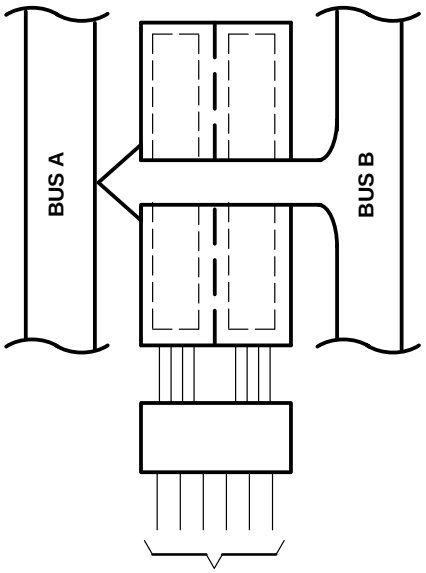
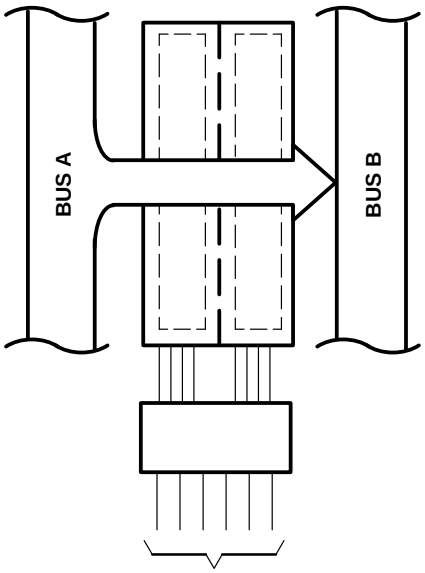


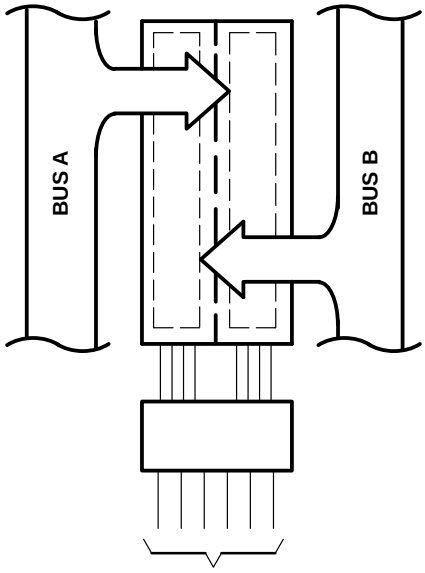
1	14	28	16	27	15
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



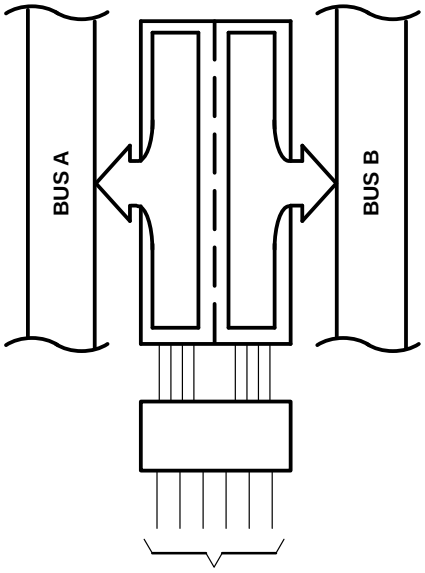
1	14	28	16	27	15
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1	14	28	16	27	15
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1	14	28	16	27	15
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

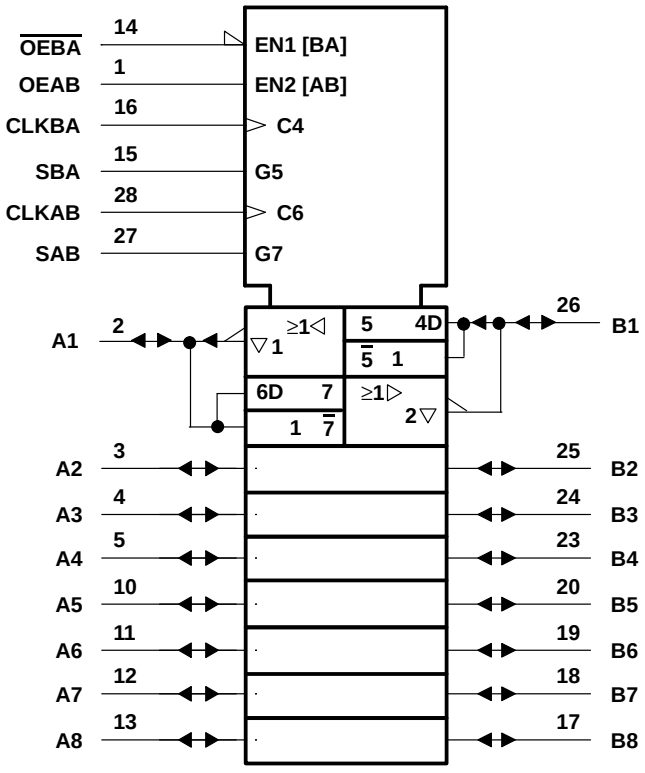
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Output	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

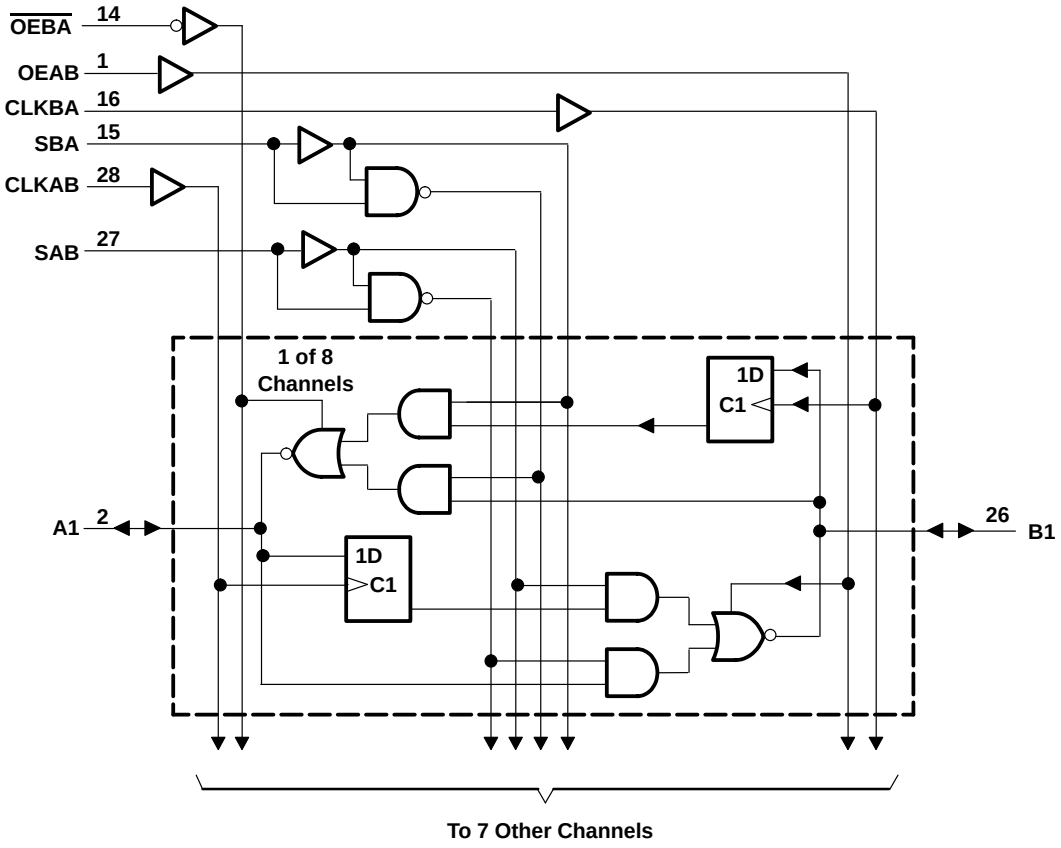
‡ When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 µA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	µA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	45	0	45	MHz
t_w	Pulse duration, CLK high or low	10		10		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	6.5		6.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	90	0	90	MHz
t_w	Pulse duration, CLK high or low	5.5		5.5		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	4.5		4.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			45			45		MHz
t_{PLH}	A or B	B or A	3.2	7.7	12.1	3.2	14	ns
t_{PHL}			4.3	9.5	14.6	4.3	16.1	
t_{PLH}	CLKBA or CLKAB	A or B	4.6	9.8	15	4.6	17.2	ns
t_{PHL}			5.4	11.5	17.5	5.4	19.2	
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.8	8.6	13.3	3.8	15.3	ns
t_{PHL}			4.8	10.2	15.5	4.8	17.1	
t_{PLH}	SBA or SAB† (A or B low)	A or B	3.4	8.1	12.7	3.4	14.6	ns
t_{PHL}			5	10.3	15.5	5	17.1	
t_{PZH}	OEBA	A	4.6	9.8	14.9	4.6	16.9	ns
t_{PZL}			5.3	12.1	18.9	5.3	21.3	
t_{PHZ}	OEBA	A	4.4	6.6	8.8	4.4	9.2	ns
t_{PLZ}			3.8	5.8	7.8	3.8	8.1	
t_{PZH}	OEAB	B	4.9	10.2	15.5	4.9	17.6	ns
t_{PZL}			5.5	12.2	18.8	5.5	21.2	
t_{PHZ}	OEAB	B	4.4	6.7	8.9	4.4	9.3	ns
t_{PLZ}			3.5	5.7	7.8	3.5	8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

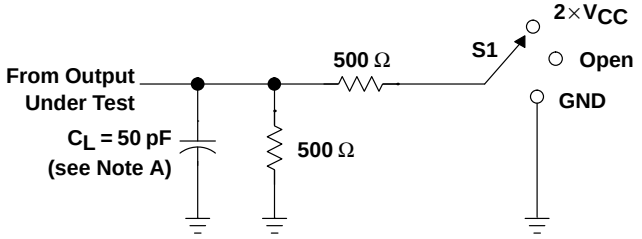
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			90			90		MHz
t_{PLH}	A or B	B or A	2.6	5.3	8	2.6	9.1	ns
t_{PHL}			3.5	6.5	9.4	3.5	10.5	
t_{PLH}	CLKBA or CLKAB	A or B	3.8	6.8	10	3.8	11.4	ns
t_{PHL}			4.7	8.1	11.5	4.7	12.8	
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.2	6	8.8	3.2	10.1	ns
t_{PHL}			3.9	7	10.1	3.9	11.2	
t_{PLH}	SBA or SAB† (A or B low)	A or B	2.9	5.7	8.5	2.9	9.5	ns
t_{PHL}			4.1	7.2	10.3	4.1	11.4	
t_{PZH}	OEBA	A	3.9	6.9	9.8	3.9	11.1	ns
t_{PZL}			4.2	7.6	11	4.2	12.5	
t_{PHZ}	OEBA	A	4.1	5.9	7.6	4.1	8	ns
t_{PLZ}			3.5	5.2	6.8	3.5	7.1	
t_{PZH}	OEAB	B	4.2	5.9	10.4	4.2	11.8	ns
t_{PZL}			4.5	8	11.4	4.5	12.9	
t_{PHZ}	OEAB	B	4.2	6	7.8	4.2	8.2	ns
t_{PLZ}			3.3	5.1	6.9	3.3	7.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

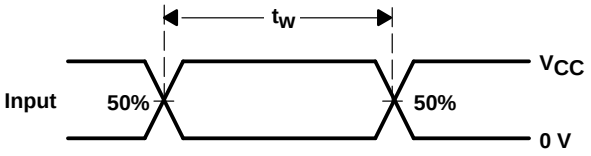
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	64	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

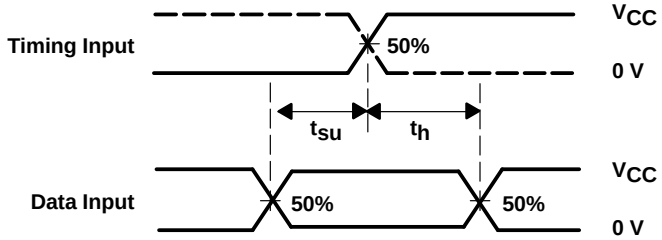


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

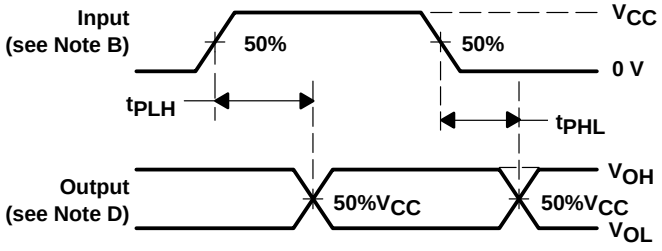
LOAD CIRCUIT FOR OUTPUTS



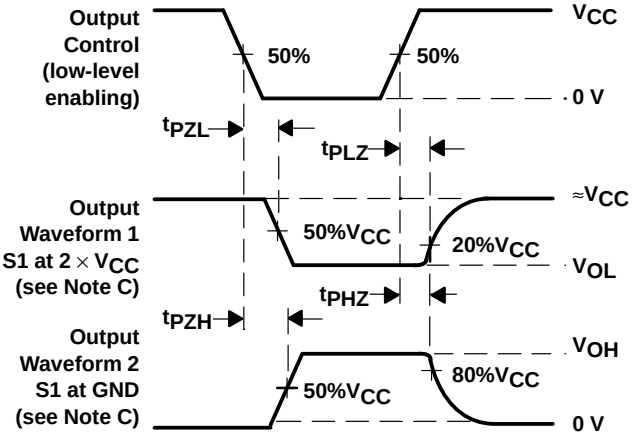
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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