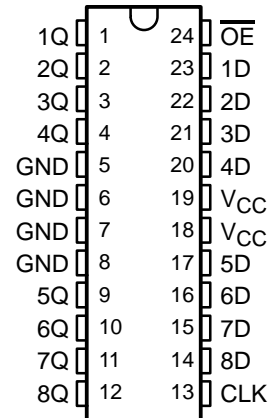


74ACT11478 METASTABLE-RESISTANT OCTAL D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS131 – APRIL 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Specifically Designed for Data Synchronization Applications
- Improved Metastable Characteristics Provide Greater System Reliability
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

The 74ACT11478 is an 8-bit dual-rank synchronizer circuit designed specifically for data synchronization applications where the normal setup and hold time specifications are frequently violated.

Synchronization of two digital signals operating at different frequencies is a common system problem. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. This solution, however, causes the setup and hold time specifications associated with the flip-flop to be violated. When the setup or hold time specification is violated, the output response is uncertain.

A flip-flop is metastable if its output hangs up in the region between V_{IL} and V_{IH} . The metastable condition lasts until the flip-flop recovers into one of its two stable states. With conventional flip-flops, this recovery time can be longer than the specified maximum propagation delay.

The problem of metastability is typically solved by adding an additional layer of synchronization. This type of dual ranking is employed in the 74ACT11478. The probability of the second stage entering the metastable state is exponentially reduced by this dual-rank architecture. The 74ACT11478 provides a one-chip solution for system designers in asynchronous applications.

The 74ACT11478 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

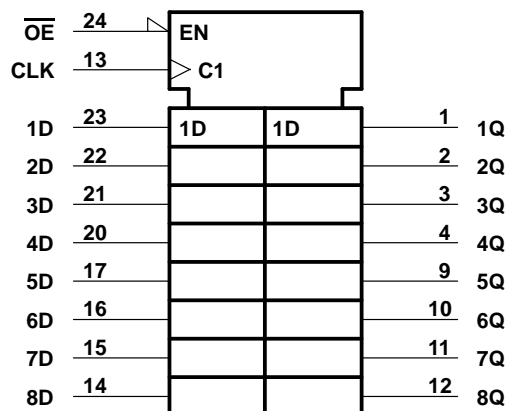
INPUTS			OUTPUT
\overline{OE}	CLOCK†	D	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	H	X	Q_O

† Data presented at the D input requires two clock cycles to appear at the Q output.

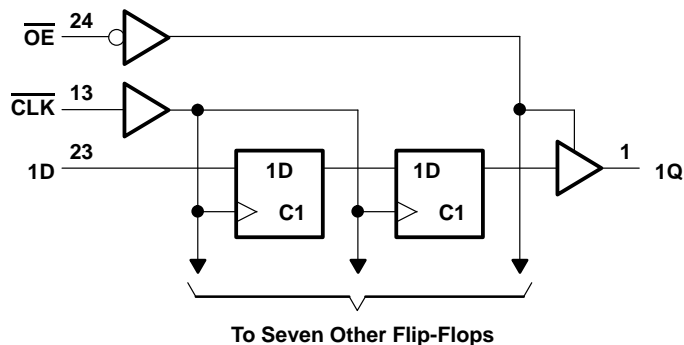
METASTABLE-RESISTANT OCTAL D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS131 – APRIL 1990 – REVISED APRIL 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	– 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		− 24	mA
I _{OL}	Low-level output current		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns /V
T _A	Operating free-air temperature	− 40	85	°C

74ACT11478

METASTABLE-RESISTAND OCTAL D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS131 – APRIL 1990 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = – 50 µA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I _{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I _{OH} = – 75 mA [†]	5.5 V				3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I _{OL} = 75 mA [†]	5.5 V					1.65	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.5		± 5	µA
I _I	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	µA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1	mA
C _i	V _I = V _{CC} or GND	5 V		4.5				pF
C _o	V _O = V _{CC} or GND	5 V		12				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f _{clock}	Clock frequency	0	75	0	75	MHz
t _w	Pulse duration	CLK high		4	4	ns
		CLK low		5	5	
t _{su}	Setup time, data before CLK [↑]	2.7		2.7		ns
t _h	Hold time, data after CLK [↑]	1.5		1.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f _{max}			7.5			75		MHz
t _{PLH}	CLK	Q	4.3	7.4	10.1	4.3	11.6	ns
t _{PHL}			5.6	9.4	12.6	5.6	14.2	
t _{PZH}	\overline{OE}	Q	3.7	7.5	11.1	3.7	12.6	ns
t _{PZL}			4.7	9.2	13.7	4.7	15.8	
t _{PHZ}	\overline{OE}	Q	4.4	7.2	9.2	4.4	9.8	ns
t _{PLZ}			4.7	6.6	8.7	4.7	9.3	



**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

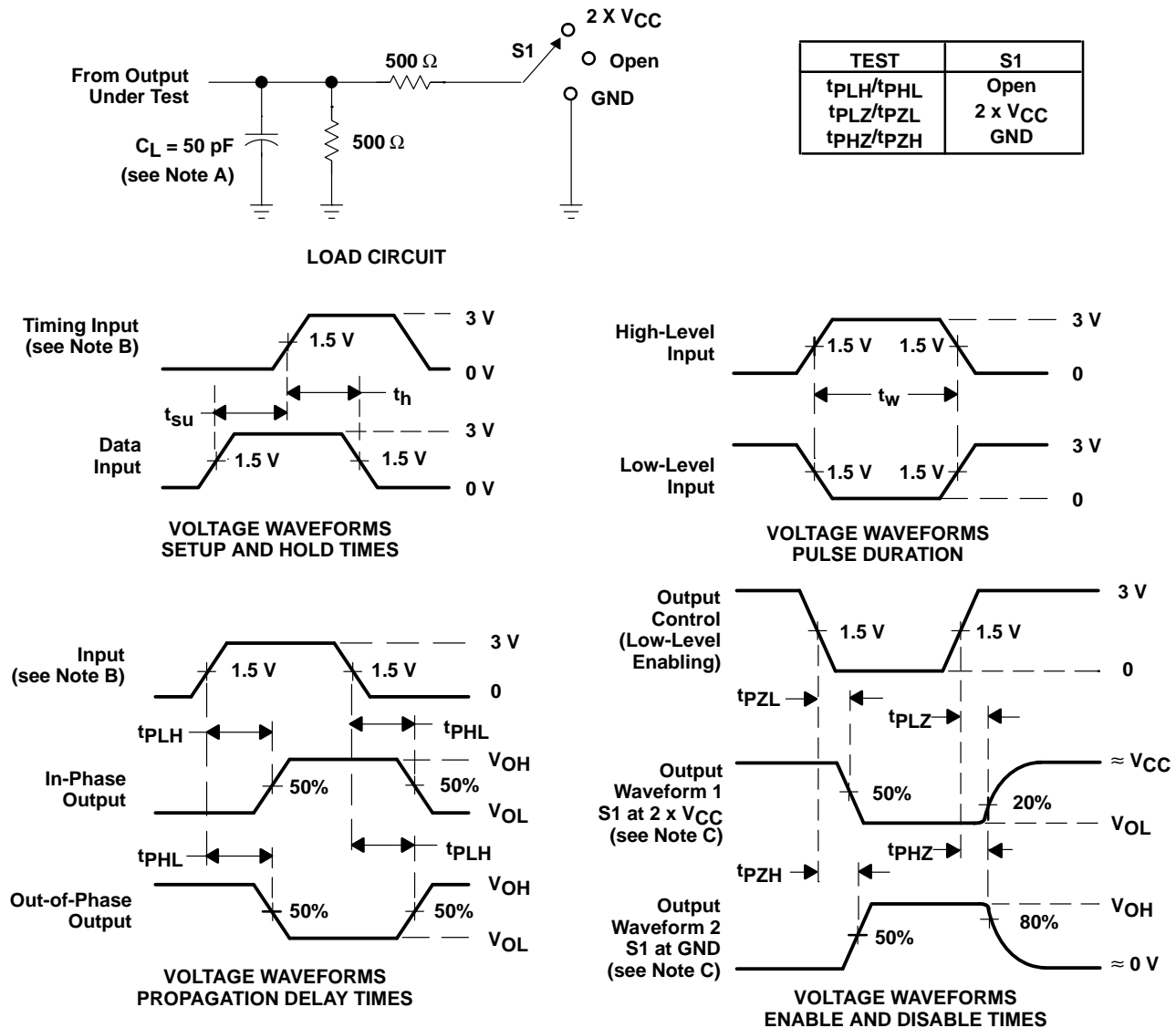
METASTABLE-RESISTANT OCTAL D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS131 – APRIL 1990 – REVISED APRIL 1993

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	76	pF
	Outputs enabled		64	

PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.