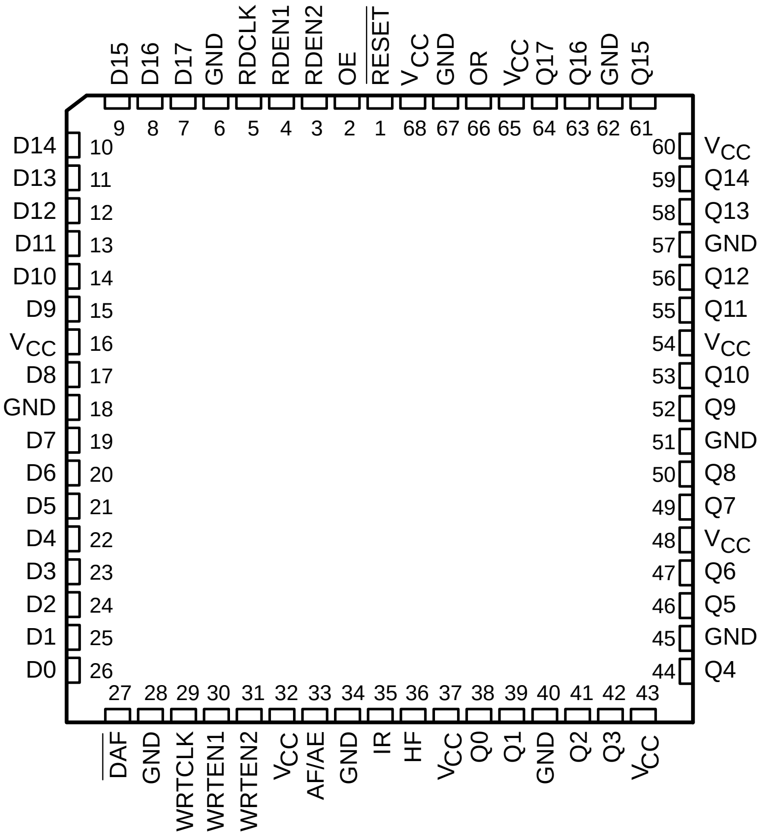
SN74ACT7801
1024 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS111 – D3489, APRIL 1990 – REVISED MAY 1991

- **Member of the Texas Instruments *Widebus*™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **1024 Words × 18 Bits**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **High-Output Drive for Direct Bus Interface**
- **3-State Outputs**
- **Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat Package (PN)**

FN PACKAGE
(TOP VIEW)



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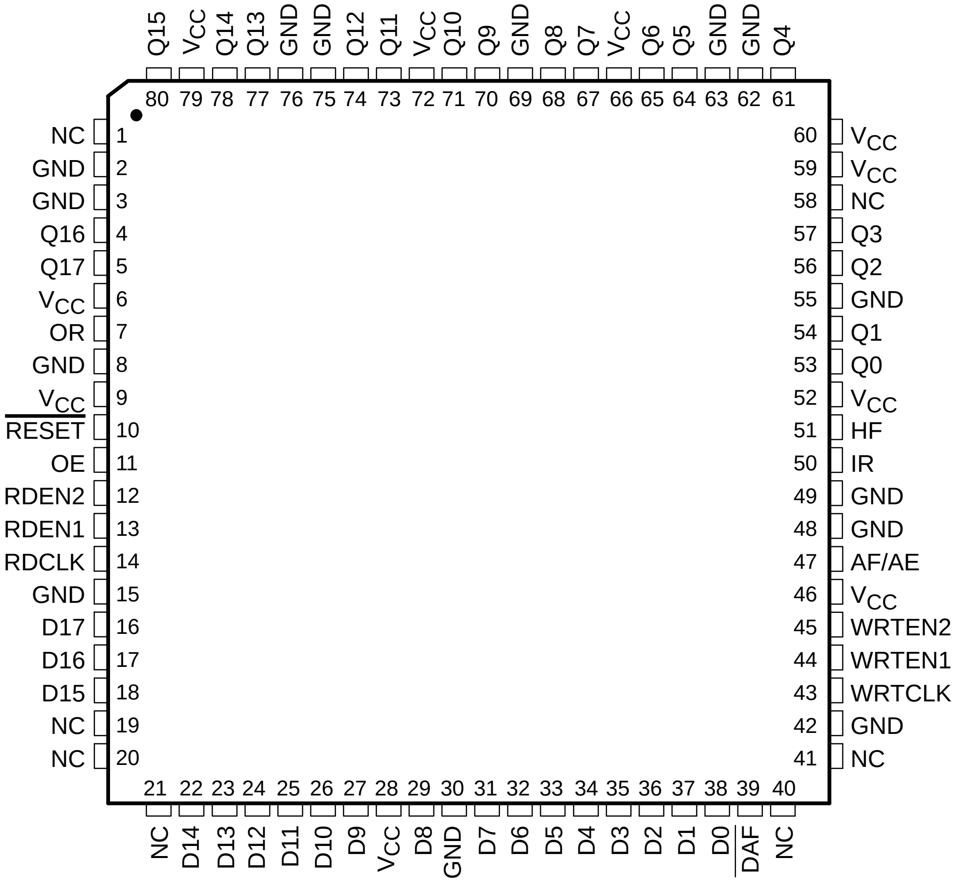
**PN PACKAGE
(TOP VIEW)**



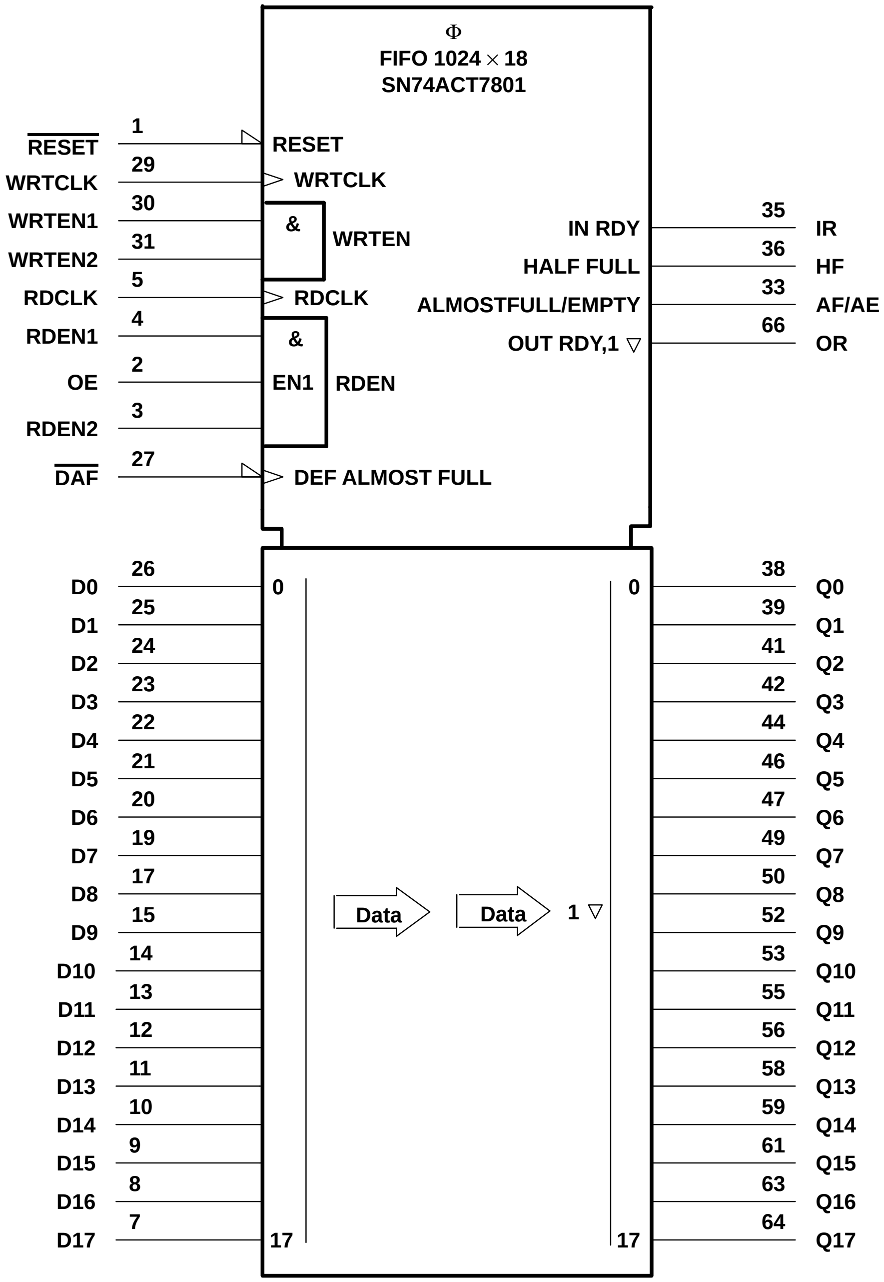
NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7801 is a 1024- × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

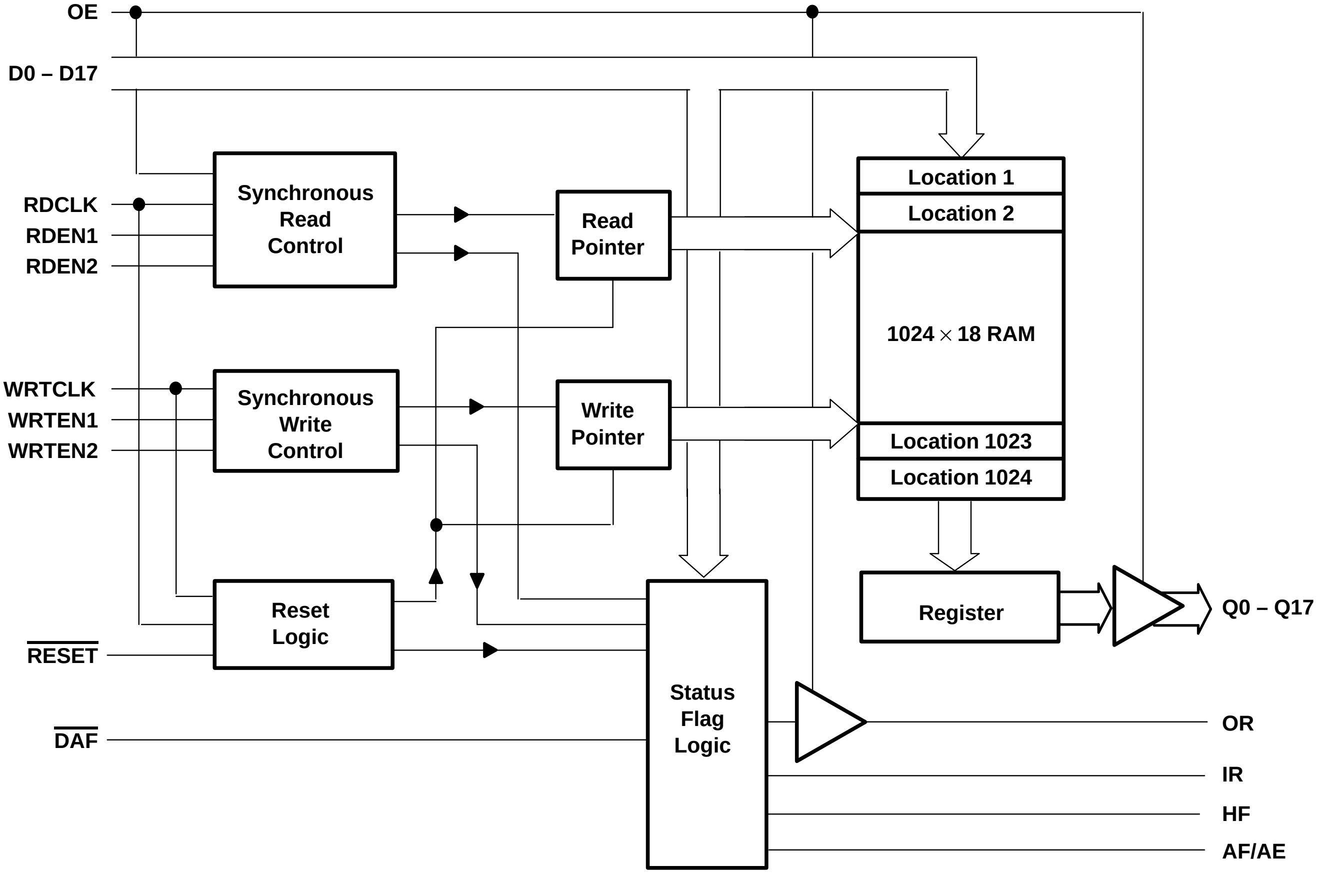
The SN74ACT7801 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



functional description

inputs

data in (D0–D17)

Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0–D8 also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the define almost-full ($\overline{\text{DAF}}$) input.

reset ($\overline{\text{RESET}}$)

A reset is accomplished by taking reset ($\overline{\text{RESET}}$) low and generating a minimum of four read-clock (RDCLK) and write-clock (WRTCLK) cycles. This ensures that the internal read and write pointers are reset and that the output-ready flag (OR), the half-full flag (HF), and the input-ready flag (IR) are low; the almost-full/almost-empty flag (AF/AE) is high. The FIFO must be reset upon power up. With the define almost-full ($\overline{\text{DAF}}$) input at a low level, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

write enables (WRTEN1, WRTEN2)

The write enables (WRTEN1, WRTEN2) must be high before the rising edge of write clock (WRTCLK) for a word to be written into memory. The write enables do not affect the storage of the almost-full/almost-empty offset value (X).

functional description (continued)

write clock (WRTCLK)

Data is written into memory on a low-to-high transition of the write clock (WRTCLK) if the input-ready flag output (IR) and the write-enable control inputs (WRTEN1, WRTEN2) are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. The IR flag output is also driven synchronously with respect to the WRTCLK signal.

read enables (RDEN1, RDEN2)

Both read enables (RDEN1, RDEN2) must be high before the rising edge of read clock (RDCLK) to read a word out of memory. The read enables are not used to read the first word stored in memory.

read clock (RDCLK)

Data is read out of memory on a low-to-high transition at the read-clock (RDCLK) input if the output-ready flag output (OR) and the output-enable (OE) and read-enable (RDEN1, RDEN2) control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. The OR flag is also driven synchronously with respect to the RDCLK signal.

define almost-full ($\overline{\text{DAF}}$)

The high-to-low transition of the define almost-full ($\overline{\text{DAF}}$) input stores the binary value of data inputs D0–D8 as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on the reset ($\overline{\text{RESET}}$) input defines the almost-full/almost-empty flag (AF/AE) using X.

output enable (OE)

The data-out (Q0–Q17) outputs and the output-ready flag (OR) are in the high-impedance state when the output enable (OE) input is low. OE must be high before the rising edge of read clock (RDCLK) to read a word from memory.

outputs

data out (Q0–Q17)

The first data word to be loaded into the FIFO is moved to the data out (Q0– Q17) register on the rising edge of the third read clock (RDCLK) pulse to occur after the first valid write. The read-enable (RDEN1, RDEN2) inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, and the output-ready flag (OR) are high.

input-ready flag (IR)

The input-ready flag (IR) is high when the FIFO is not full and low when the device is full. During reset, the IR flag is driven low on the rising edge of the second write clock (WRTCLK) pulse. The IR flag is driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.

output-ready flag (OR)

The output-ready flag (OR) is high when the FIFO is not empty and low when it is empty. During reset, the OR flag is set low on the rising edge of the third read clock (RDCLK) pulse. The OR flag is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.

half-full status flag (HF)

The half-full flag (HF) is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.

functional description (continued)

almost-full/almost-empty status flag (AF/AE)

The almost-full/almost-empty flag (AF/AE) is defined by the almost-full/almost-empty offset value (X). The AF/AE flag is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. The AF/AE flag is low when the FIFO contains between (X + 2) and (1024 – X) words.

programming procedure for AF/AE

The almost-full/almost-empty flag (AF/AE) is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default value of X = 256. Below are instructions to program AF/AE using both methods.

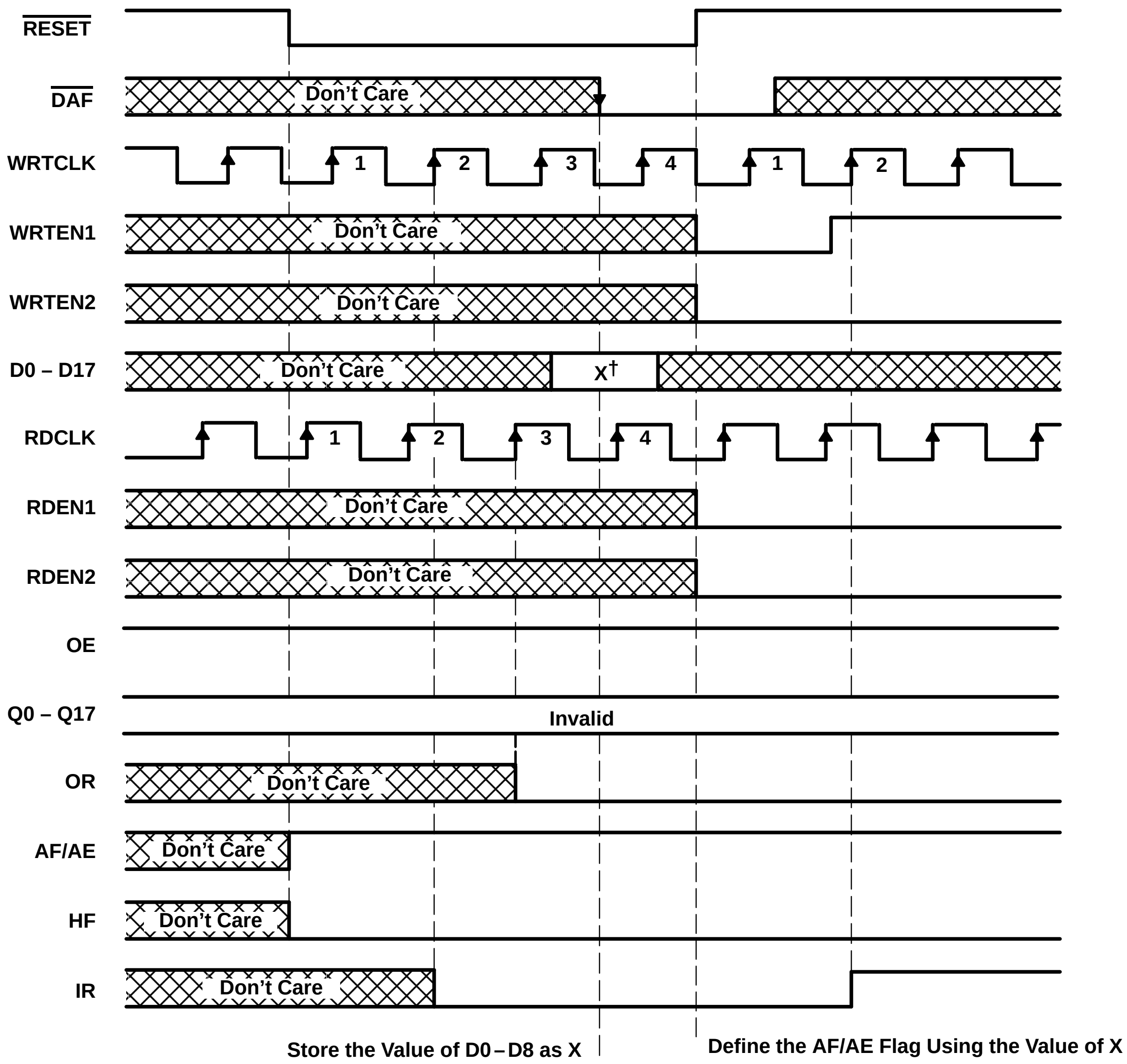
user-defined X:

1. Take $\overline{\text{DAF}}$ from high to low.
2. If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low.
3. With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE flag using X.
4. To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

default X:

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

timing diagrams



† X is the binary value of D0 – D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X

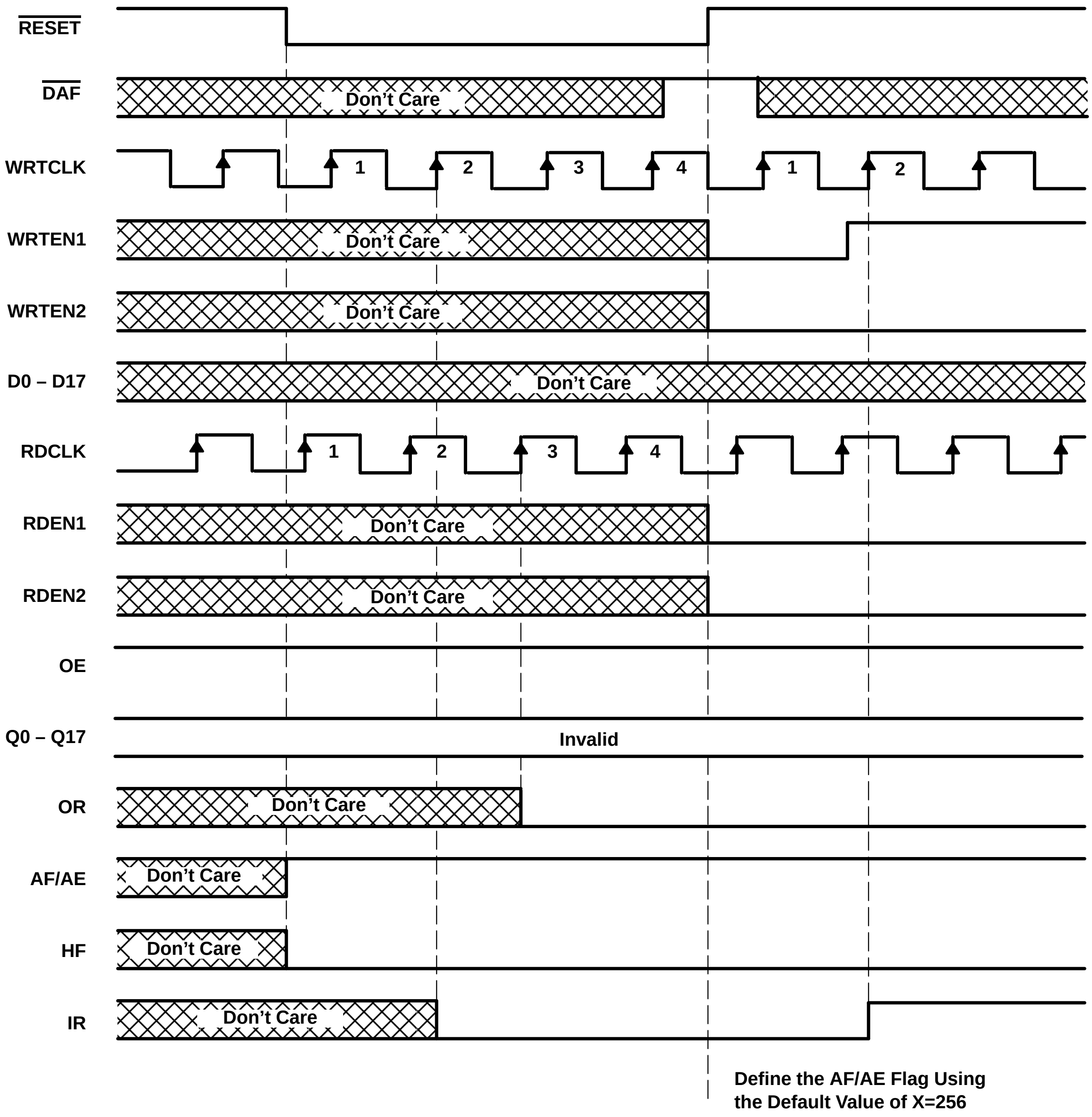


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

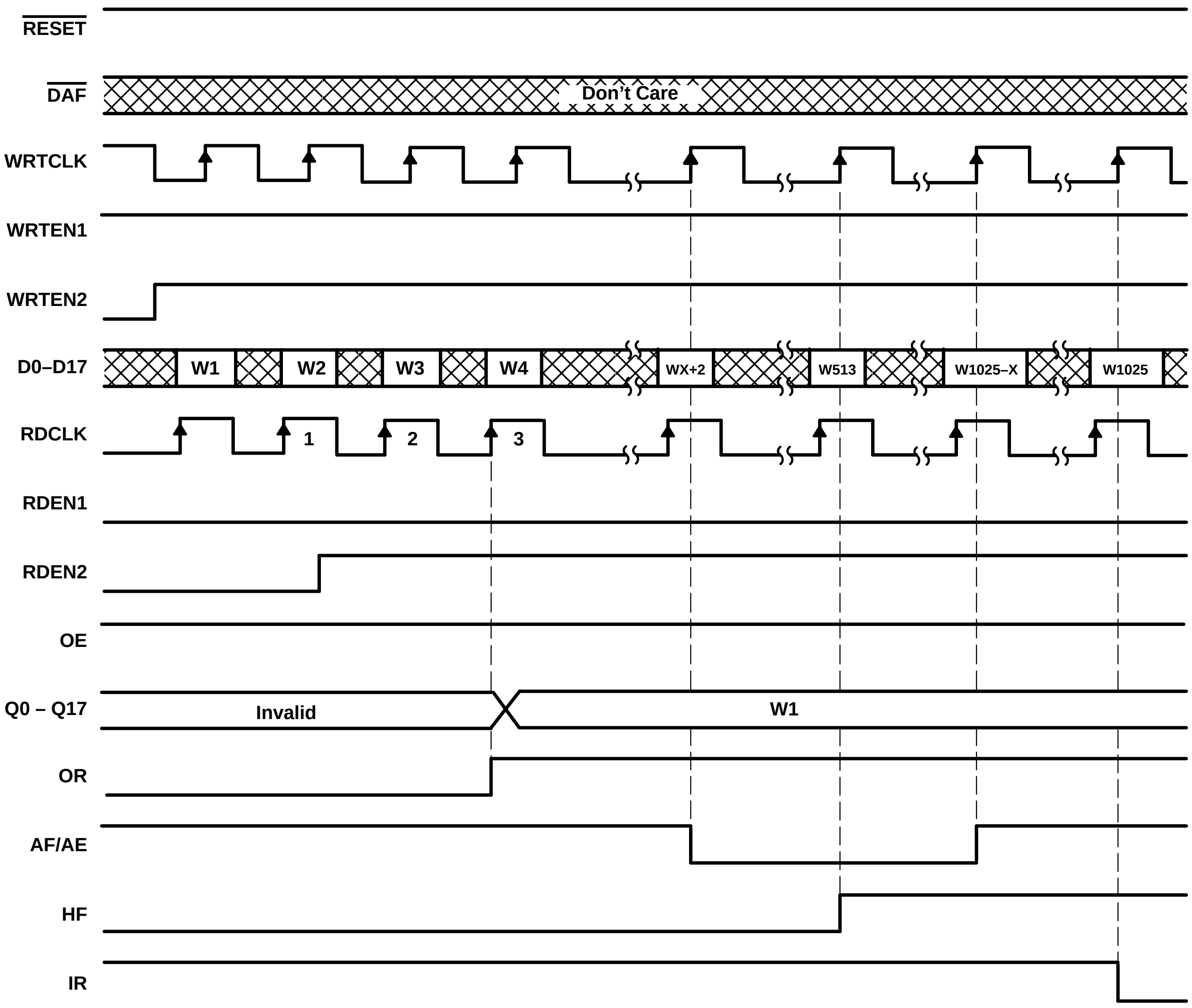


Figure 3. Write

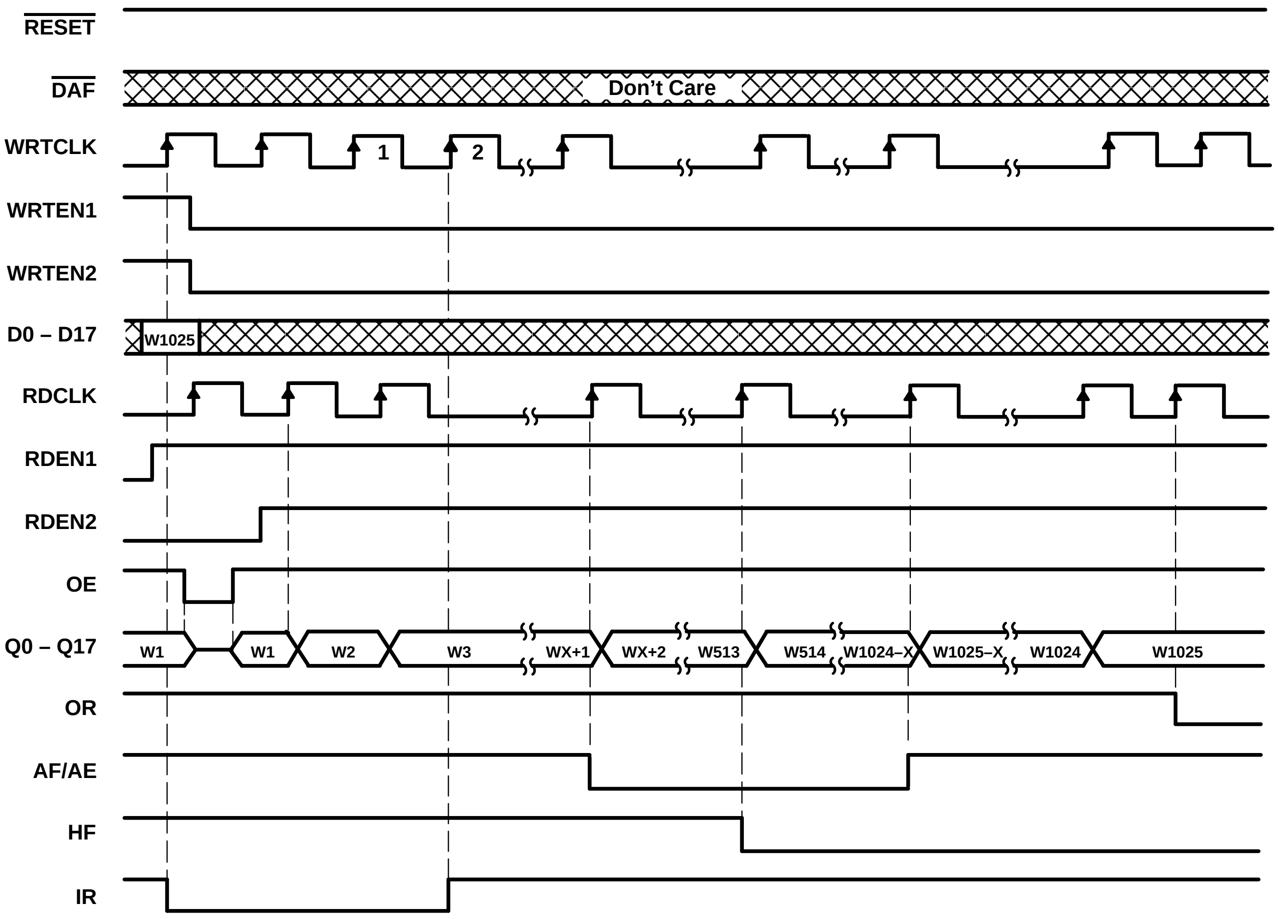


Figure 4. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage, V_I . . . . 7 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			′ACT7801-15		′ACT7801-18		′ACT7801-20		UNIT
			MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current			–8		–8		–8	mA
I_{OL}	Low-level output current			16		16		16	mA
f_{clock}	Clock frequency		40		35		28.5		MHz
t_w	Pulse duration	Data in (D0–D17) high or low	10		12		14		ns
		WRTCLK high	7		8.5		10		
		WRTCLK low	15		15		15		
		RDCLK high	7		8.5		10		
		RDCLK low	15		15		15		
		$\overline{\text{DAF}}$ high	10		10		10		
		WRTEN1, WRTEN2 high or low	10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		
t_{su}	Setup time	Data in (D0–D17) before WRTCLK↑	5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK and RDCLK↑	7		7		7		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	5		5		5		
t_h	Hold time	Data in (D0–D17) after WRTCLK↑	1		1		1		ns
		WRTEN1, WRTEN2 after WRTCLK↑	1		1		1		
		OE, RDEN1, RDEN2 after RDCLK↑	1		1		1		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK and RDCLK↑	0		0		0		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	1		1		1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	1		1		1		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC1}[‡]	Supply current	f_{clock} = 25 MHz[§]			200	230	mA
I_{CC2}[‡]	Standby current	V_{IH} = WRTCLK,	V_I = V_{IH} or V_{IL}		20	25	mA
I_{CC3}[‡]	Power-down current	V_I = V_{CC} – 0.2 V or 0				400	µA
C_i		V_I = 0,	f = 1 MHz		4		pF
C_o		V_O = 0,	f = 1 MHz		8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	′ACT7801-15			′ACT7801-18		′ACT7801-20		UNIT
			MIN	TYP[†]	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		40			35		28.5		MHz
t_{pd}	RDCLK↑	Any Q	5	12	15	5	18	5	20	ns
t_{pd}[¶]				10.5						
t_{pd}	WRTCLK↑	IR	4		10	4	12	4	14	ns
t_{pd}	RDCLK↑	OR	4		10	4	12	4	14	ns
t_{pd}	WRTCLK↑	AF/AE	7		20	7	22	7	24	ns
	RDCLK↑		7		20	7	22	7	24	
t_{PLH}	WRTCLK↑	HF	6		19	6	21	6	23	ns
t_{PHL}	RDCLK↑		6		19	6	21	6	23	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	4		19	4	21	4	23	ns
t_{PHL}		HF	4		21	4	23	4	25	
t_{en}	OE	Any Q, OR	4		11	4	11	4	11	ns
t_{dis}			2		14	2	14	2	14	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡] I_{CC} tested with outputs open.
[§] For frequencies greater than 25 MHz, I_{CC} = 230 mA + (6 mA × [f – 25 MHz]).
[¶] This parameter is measured with C_L = 30 pF (see Figure 5).

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

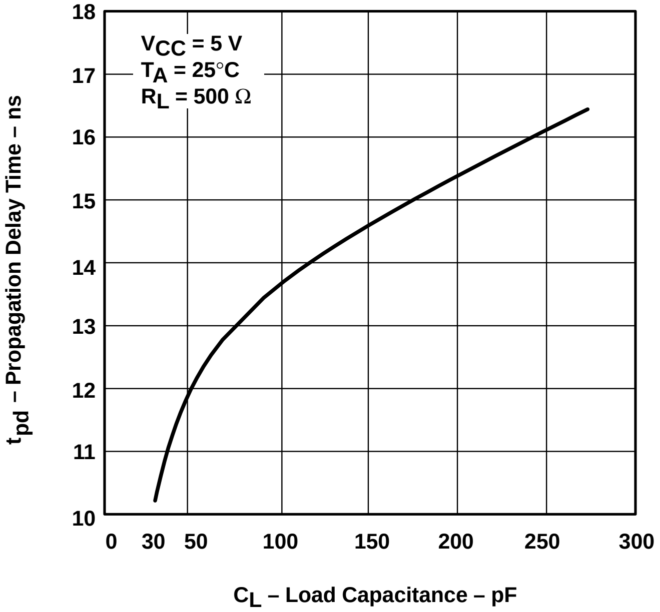


Figure 5

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

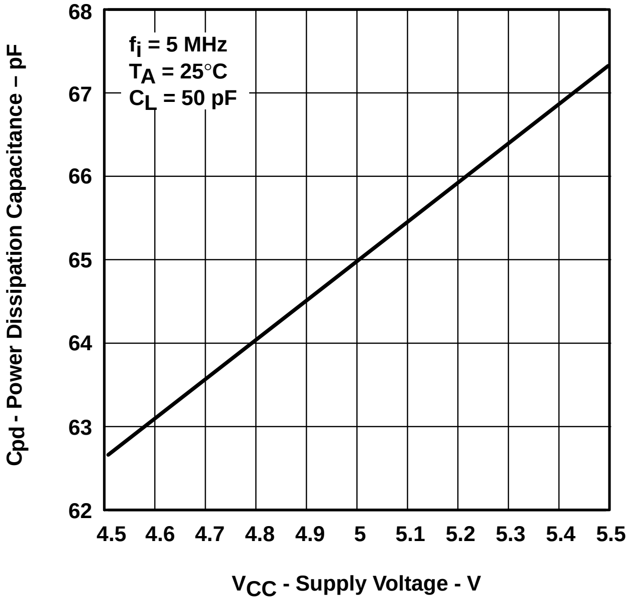


Figure 6

calculating power dissipation

With I_{CCF} taken from Figure 6, the maximum power dissipation based on all data outputs changing states on each read may be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times fi) + \Sigma(C_L \times V_{CC}^2 \times fo)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
Δ I_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

expanding the SN74ACT7801

The SN74ACT7801 is expandable in width and depth. Expanding in word depth offers special timing considerations:

1. After the first data word is loaded into the FIFO, the word is unloaded, and the output-ready flag output (OR) goes high after (N × 3) read clock (RDCLK) cycles, where N is the number of devices used in depth expansion.
2. After the FIFO is filled, the input-ready flag output (IR) goes low, the first word is unloaded, and the IR flag output is driven high after (N × 2) write clock cycles, where N is the number of devices used in depth expansion.

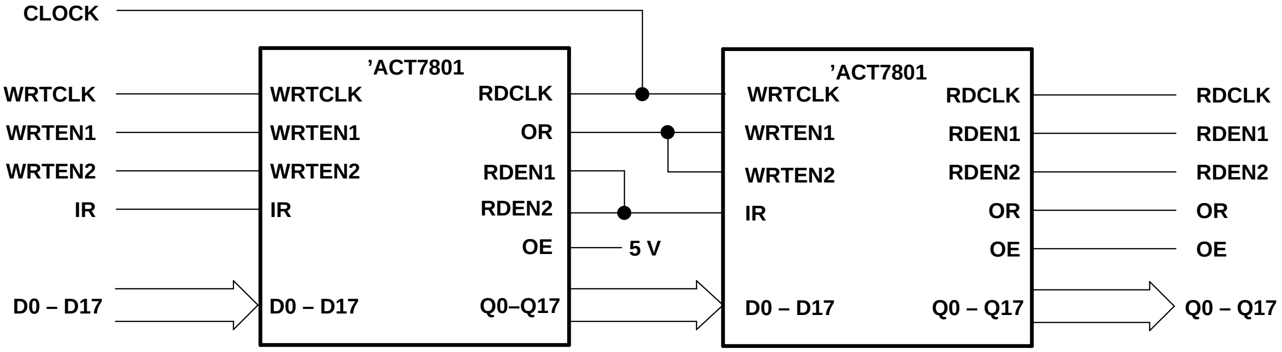


Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2

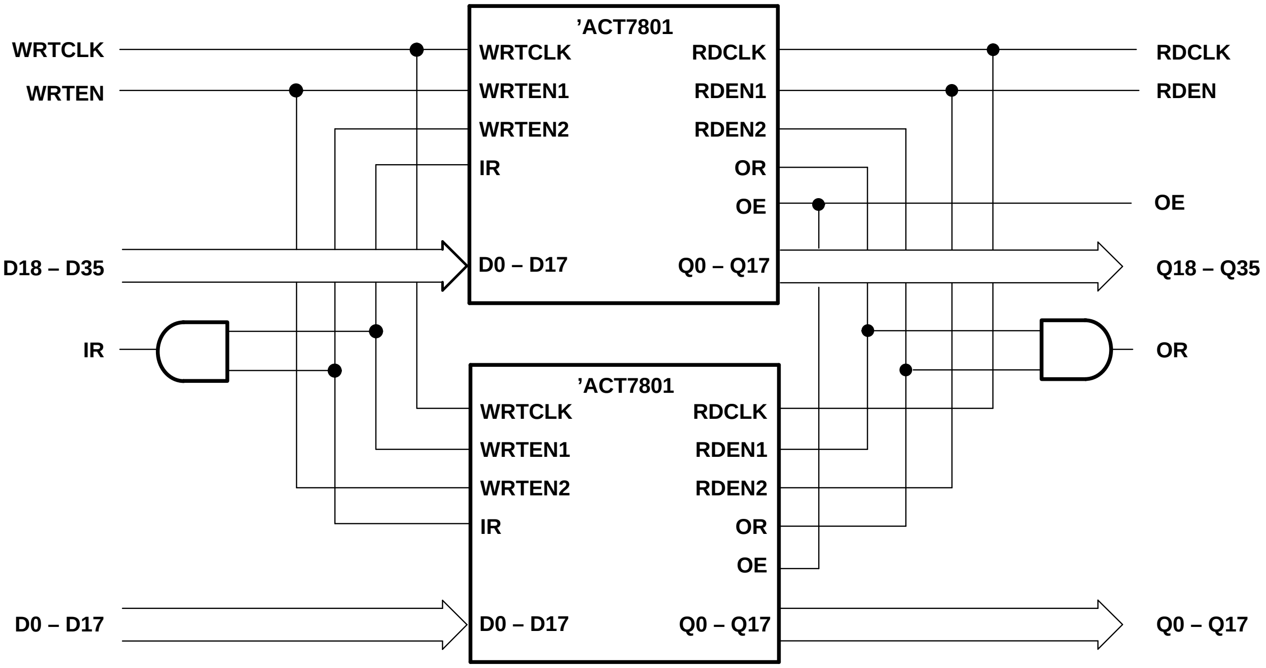


Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

PARAMETER MEASUREMENT INFORMATION

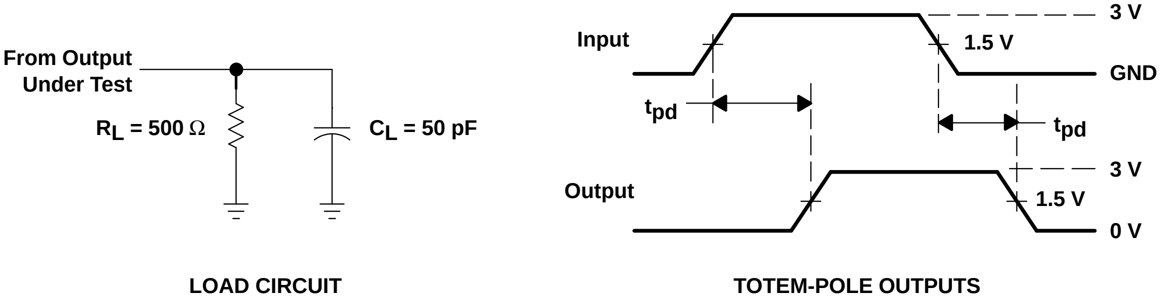
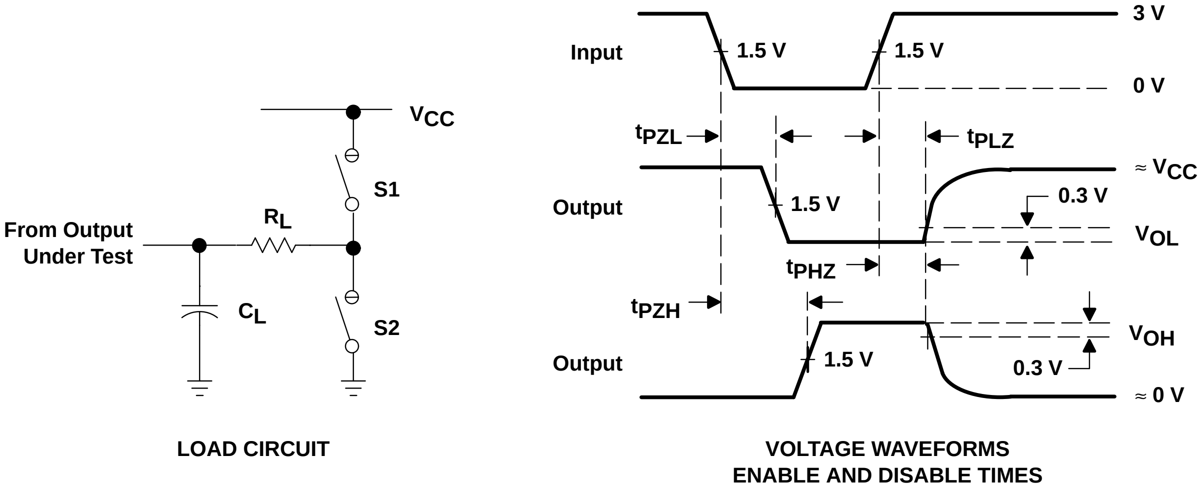


Figure 9. Standard CMOS Outputs (OR, Half Full, AF/AE)



PARAMETER		R_L	C_L[†]	S1	S2
t_{en}	t_{PZH}	500 Ω	50 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		–	50 pF	Open	Open

[†] Includes probe and test-fixture capacitance.

Figure 10. 3-State Outputs (Any Q, OR)

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