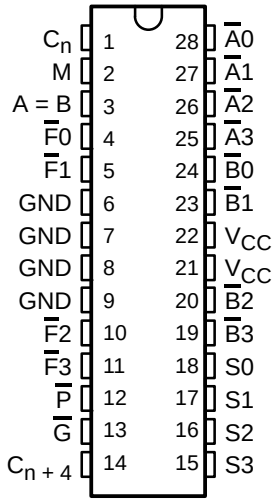
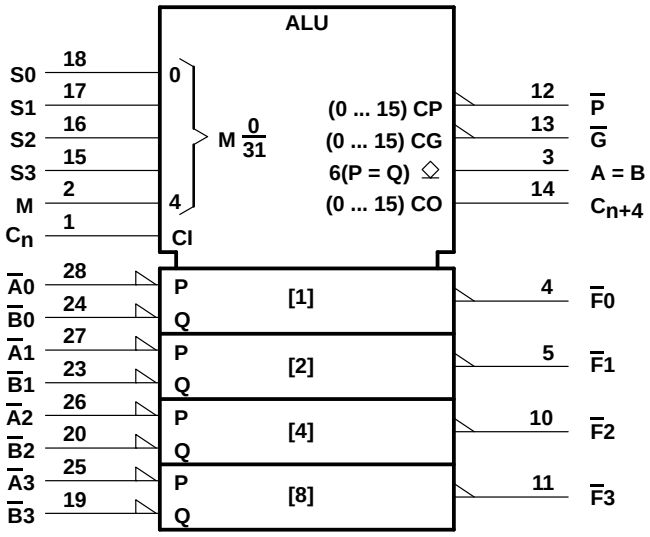
SCAS086 – D3200, OCTOBER 1989 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **New Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Full Look Ahead for High-Speed Operations on Long Words**
- **Arithmetic Operating Modes:**
  - **Addition**
  - **Subtraction**
  - **Shift Operand A One Position**
  - **Magnitude Comparison**
  - **Plus Twelve Other Arithmetic Operations**
- **Logic Function Modes:**
  - **Exclusive-OR**
  - **Comparator**
  - **AND, NAND, OR, NOR**

DW PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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description

The 74ACT11181 is an arithmetic logic unit (ALU)/function generator that has a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs $\overline{G}$ and $\overline{P}$ for the four bits in the package. When used in conjunction with the 'ACT11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading 'ACT11882 circuits with these ALUs to provide multilevel full-carry look-ahead operation is illustrated under signal designations.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 74ACT11181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PACKAGE	PIN NUMBERS AND DESIGNATIONS															
DW, JT, or NT	25	26	27	28	19	20	23	24	11	10	5	4	1	14	12	13
FK	4	5	6	7	26	27	2	3	18	17	12	11	8	2	19	20
Active-low data (Table 1)	$\overline{A}3$	$\overline{A}2$	$\overline{A}1$	$\overline{A}0$	$\overline{B}3$	$\overline{B}2$	$\overline{B}1$	$\overline{B}0$	$\overline{F}3$	$\overline{F}2$	$\overline{F}1$	$\overline{F}0$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A – B – 1, which requires an end-around or forced carry to provide A – B.

The 74ACT11181 can also be used as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). When performing this comparison, the ALU must be in the subtract mode with C_n = H. The A = B output is open drain so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed not only to incorporate all of the designer's requirements for arithmetic operation but also to provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected using the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

signal designations

In both Figures 1 and 2, the polarity indicators (◺) indicate that the associated input or output data is active low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and should be used with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 74ACT11181 and 'ACT11881 together with the 'ACT11882 can be used with the signal designations of either Figure 1 or Figure 2.

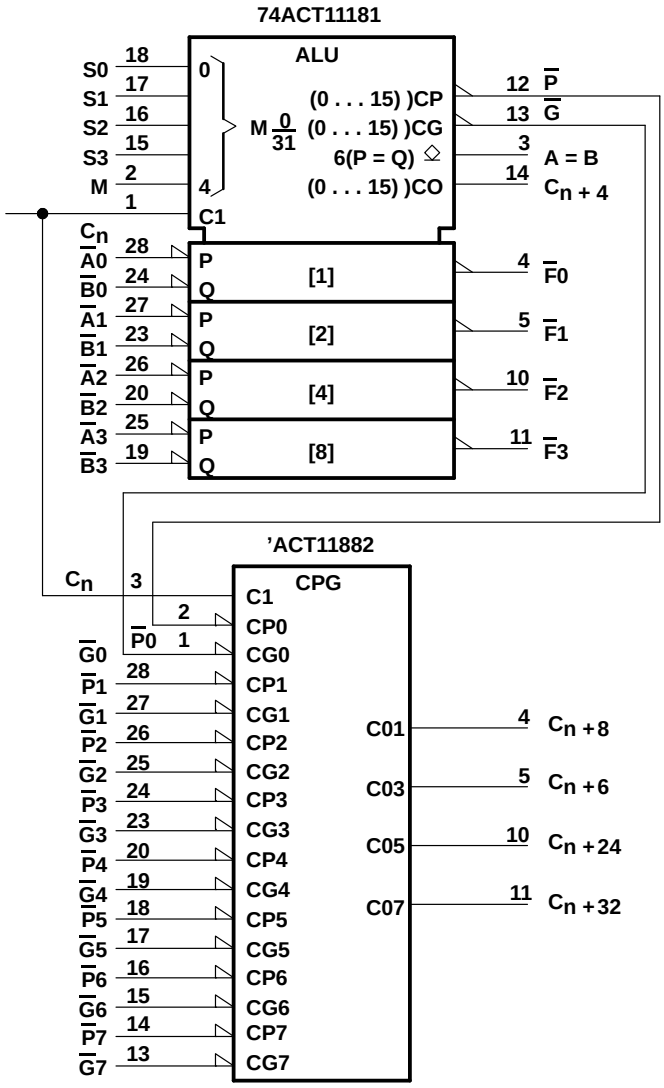


Figure 1
(use with Table 1)

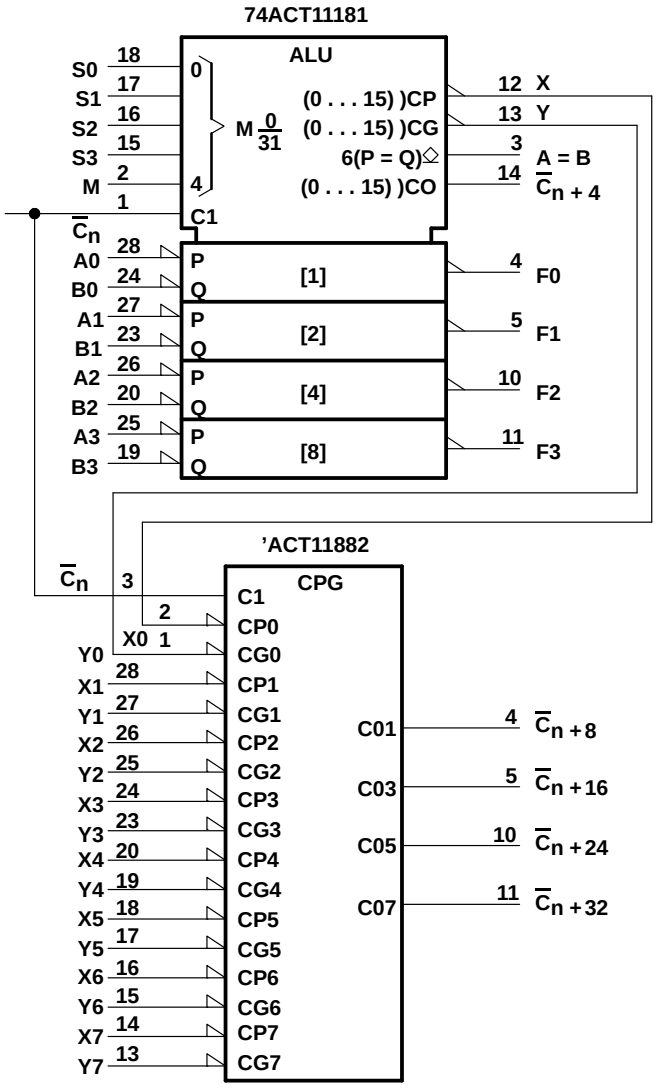


Figure 2
(use with Table 2)

Table 1

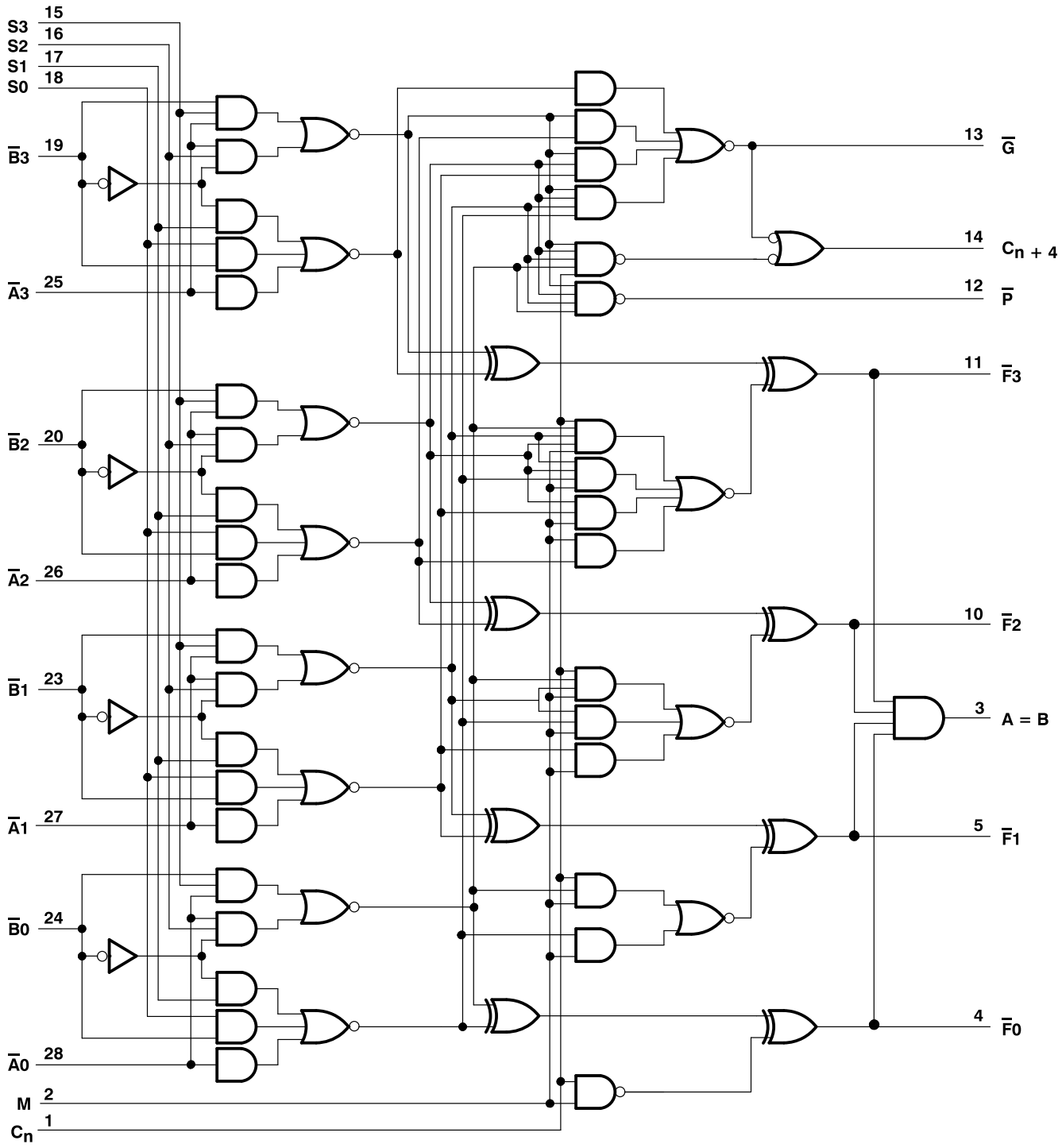
SELECTION				ACTIVE-LOW DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	All outputs except A = B		–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	Any output except A = B	I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 50 mA‡	5.5 V						
		I_{OH} = – 75 mA‡	5.5 V				3.85		
I_{OH}	A = B	V_{CC} = 5.5 V, V_O = V_{CC}	5.5 V			0.5		5	μA
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 50 mA‡	5.5 V						
		I_{OL} = 75 mA‡	5.5 V					1.65	
I_I		V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i		V_I = V_{CC} or GND	5 V		4.5				pF
C_o	A = B	V_O = V_{CC} or GND	5 V		11				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

addition mode; M = S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	C_n	C_{n+4}	1.5	10.7	17.5	1.5	18.6	ns
t_{PHL}			1.5	11.3	16.2	1.5	18.3	
t_{PLH}	Any $\overline{A}$	C_{n+4}	1.5	12.7	20.3	1.5	21.8	ns
t_{PHL}			1.5	14	19.7	1.5	22	
t_{PLH}	Any $\overline{B}$	C_{n+4}	1.5	13.5	21.6	1.5	23.2	ns
t_{PHL}			1.5	13.6	19.7	1.5	22	
t_{PLH}	C_n	Any $\overline{F}$	1.5	11.2	17.1	1.5	18.7	ns
t_{PHL}			1.5	9.9	15.9	1.5	17.4	
t_{PLH}	Any $\overline{A}$	$\overline{G}$	1.5	12.8	20.9	1.5	23.3	ns
t_{PHL}			1.5	12.7	17.8	1.5	20.9	
t_{PLH}	Any $\overline{B}$	$\overline{G}$	1.5	12.7	20.6	1.5	22.1	ns
t_{PHL}			1.5	14.3	19.2	1.5	21.3	
t_{PLH}	Any $\overline{A}$	$\overline{P}$	1.5	11.4	18.4	1.5	19.6	ns
t_{PHL}			1.5	9.6	16.6	1.5	17.4	
t_{PLH}	Any $\overline{B}$	$\overline{P}$	1.5	11.3	18.2	1.5	19.3	ns
t_{PHL}			1.5	10.6	15.6	1.5	16.6	
t_{PLH}	$\overline{A}i$	$\overline{F}i$	1.5	11.8	17.7	1.5	19.5	ns
t_{PHL}			1.5	11	17.7	1.5	18.7	
t_{PLH}	$\overline{B}i$	$\overline{F}i$	1.5	11.6	17.3	1.5	19.1	ns
t_{PHL}			1.5	12	19.4	1.5	20.6	
t_{PLH}	$\overline{A}i$	Any $\overline{F}$ except $\overline{F}i$	1.5	13	18.9	1.5	21	ns
t_{PHL}			1.5	12.4	18.8	1.5	20.2	
t_{PLH}	Any $\overline{B}$	Any $\overline{F}$ except $\overline{F}i$	1.5	13.1	18.7	1.5	21	ns
t_{PHL}			1.5	13.5	19.8	1.5	21.3	

mode switching; S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	M	Any $\overline{F}$	1.5	9.5	15	1.5	16.3	ns
t_{PHL}			1.5	10.6	16.4	1.5	17.5	
t_{PLH}	M	A = B	1.5	15.7	19.3	1.5	20.1	ns
t_{PHL}			1.5	14	18.7	1.5	21.8	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

subtraction mode; M = S0 = S3 = 0 V, S1 = S2 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	C_n	C_{n+4}	1.5	10.7	17.5	1.5	18.6	ns
t_{PHL}			1.5	11.3	16.2	1.5	18.3	
t_{PLH}	Any $\overline{A}$	C_{n+4}	1.5	12.7	20.3	1.5	21.8	ns
t_{PHL}			1.5	13.5	19.7	1.5	20.8	
t_{PLH}	Any $\overline{B}$	C_{n+4}	1.5	13.8	21.1	1.5	22.7	ns
t_{PHL}			1.5	14.8	20.7	1.5	23	
t_{PLH}	C_n	Any $\overline{F}$	1.5	11.2	17.1	1.5	18.7	ns
t_{PHL}			1.5	9.9	15.9	1.5	17.4	
t_{PLH}	Any $\overline{A}$	$\overline{G}$	1.5	12.8	20.8	1.5	22.2	ns
t_{PHL}			1.5	12.7	18.4	1.5	20.7	
t_{PLH}	Any $\overline{B}$	$\overline{G}$	1.5	13.2	20.8	1.5	21.6	ns
t_{PHL}			1.5	11.5	18.5	1.5	19.6	
t_{PLH}	Any $\overline{A}$	$\overline{P}$	1.5	9.6	14.6	1.5	15.5	ns
t_{PHL}			1.5	10.8	18.8	1.5	20	
t_{PLH}	Any $\overline{B}$	$\overline{P}$	1.5	10.4	15.1	1.5	16.3	ns
t_{PHL}			1.5	11.9	17.8	1.5	19.6	
t_{PLH}	$\overline{A}i$	$\overline{F}i$	1.5	11.2	17.2	1.5	19.9	ns
t_{PHL}			1.5	12.1	17.8	1.5	19.5	
t_{PLH}	$\overline{B}i$	$\overline{F}i$	1.5	12	18.6	1.5	20.7	ns
t_{PHL}			1.5	13.2	19	1.5	21.1	
t_{PLH}	Any $\overline{A}$	Any $\overline{F}$	1.5	12.6	18.9	1.5	20.3	ns
t_{PHL}			1.5	13.6	19.4	1.5	21.5	
t_{PLH}	Any $\overline{B}$	Any $\overline{F}$	1.5	13.1	18.7	1.5	20.4	ns
t_{PHL}			1.5	18	21.6	1.5	23.7	
t_{PLH}	Any $\overline{A}$	A = B	1.5	16	21.5	1.5	24.6	ns
t_{PHL}			1.5	18.5	22.7	1.5	23.9	
t_{PLH}	Any $\overline{B}$	A = B	1.5	18.5	22.7	1.5	23.9	ns
t_{PHL}			1.5	16.5	22	1.5	25.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

logic and arithmetic modes

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	Any $\overline{A}$	Any $\overline{F}$	M = 4.5 V (logic mode)	1.5	10	15.9	1.5	18.3	ns
t_{PHL}				1.5	11	17.4	1.5	19.6	
t_{PLH}	$\overline{Bi}$	$\overline{Fi}$	M = 4.5 V (logic mode)	1.5	12.2	18	1.5	19.6	ns
t_{PHL}				1.5	11.5	18.3	1.5	19.6	
t_{PLH}	Any S	Any $\overline{F}$	M = 0 V (arithmetic mode)	1.5	12.1	18.3	1.5	20.1	ns
t_{PHL}				1.5	10.6	15.8	1.5	17.4	
t_{PLH}	Any S	A = B	M = 0 V (arithmetic mode)	1.5	18.7	22.1	1.5	23.4	ns
t_{PHL}				1.5	17.2	22.2	1.5	25.4	
t_{PLH}	Any S	C_{n+4}	M = 4.5 V (logic mode)	1.5	13.9	21.8	1.5	23.6	ns
t_{PHL}				1.5	15.3	22.3	1.5	25.2	
t_{PLH}	Any S	$\overline{G}$	M = 0 V (arithmetic mode)	1.5	12.7	20.5	1.5	22.3	ns
t_{PHL}				1.5	13.5	19.7	1.5	22	
t_{PLH}	Any S	$\overline{P}$	M = 4.5 V (logic mode)	1.5	12.4	18.6	1.5	20.5	ns
t_{PHL}				1.5	11.7	17.7	1.5	18	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	119	pF

PARAMETER MEASUREMENT INFORMATION

ADDITION MODE TEST TABLE

FUNCTION INPUTS: M = S1 = S2 = 0 V, S0 = S2 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	Ai	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

MODE SWITCHING TEST TABLE

FUNCTION INPUTS: S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}2$, $\overline{A}2$, C_n	Any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}1$, $\overline{A}1$, C_n	A = B	In-Phase

PARAMETER MEASUREMENT INFORMATION

SUBTRACTION MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

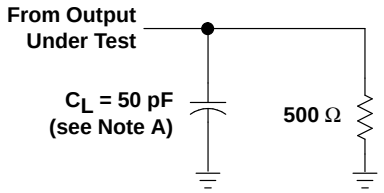
PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$ or any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$	In-Phase

LOGIC MODE TEST TABLE

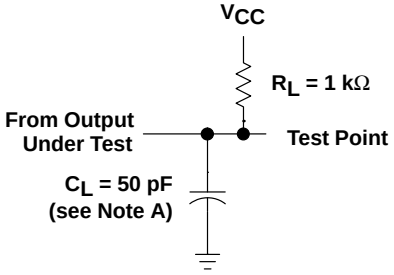
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

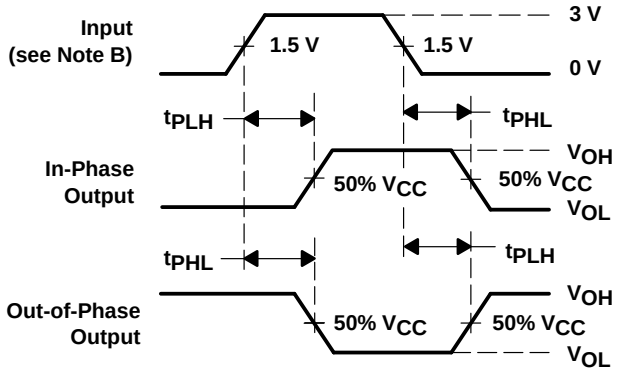
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT, TOTEM-POLE OUTPUTS



LOAD CIRCUIT, OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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