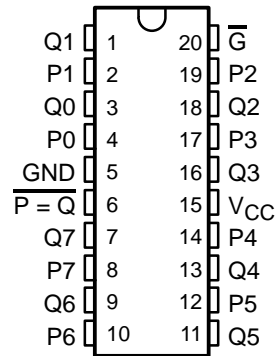


74AC11520 8-BIT IDENTITY COMPARATOR

SCAS025C – JULY 1987 – REVISED APRIL 1996

- Compares Two 8-Bit Words
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Equivalent of 20-k Ω Pullup Resistor on Q Inputs
- Package Options Include Plastic Small-Outline Packages (DW) and Standard Plastic 300-mil DIPs (N)

DW OR N PACKAGE
(TOP VIEW)



description

This identity comparator performs comparisons on two 8-bit binary or BCD words. Features include 20-k Ω pullup termination resistors on the Q inputs for analog or switch data and a $\overline{P=Q}$ totem-pole output.

The 74AC11520 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT $\overline{P=Q}$
DATA P, Q	ENABLE \overline{G}	
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

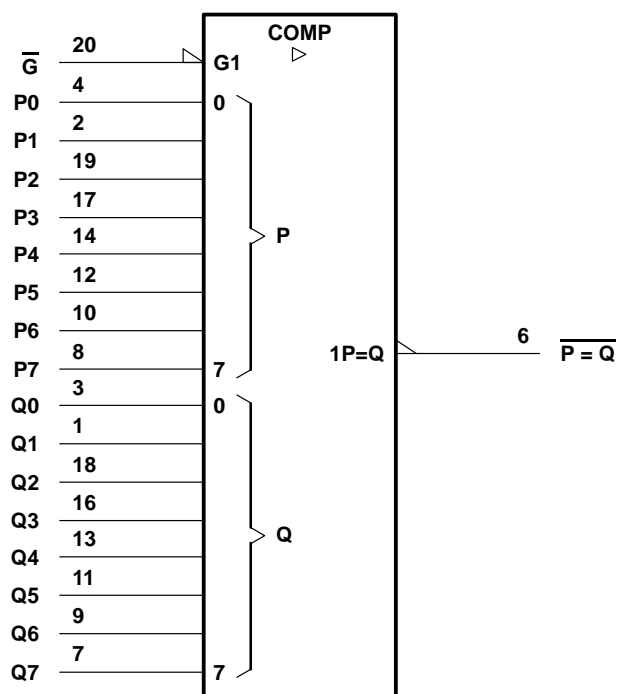
Copyright © 1996, Texas Instruments Incorporated

74AC11520

8-BIT IDENTITY COMPARATOR

SCAS025C – JULY 1987 – REVISED APRIL 1996

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

The diagram shows a CMOS inverter circuit. The input is connected to the gate of an NMOS transistor (bottom) and the gate of a PMOS transistor (top). The PMOS transistor's source is connected to VCC, and its drain is connected to the input of a second inverter. The NMOS transistor's source is connected to GND, and its drain is connected to the input of the first inverter. The output of the first inverter is connected to the input of the second inverter, forming a feedback loop. The output of the second inverter is connected to GND. The circuit is labeled with VCC at the top and GND at the bottom.

74AC11520

8-BIT IDENTITY COMPARATOR

SCAS025C – JULY 1987 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DW package	1.6 W
N package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 µA	3 V	2.9	2.9		2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I _{OH} = -75 mA [†]	5.5 V				3.85		
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I _{OL} = 75 mA [†]	5.5 V					1.65	
I _{IH}	V _I = V _{CC} , Q inputs only	5.5 V			10		10	µA
I _{IL}	V _I = GND, Q inputs only	5.5 V		-0.3	-0.6		-1	mA
I _I	V _I = V _{CC} or GND, P and \overline{G} inputs only	5.5 V			±0.1		±1	µA
I _{CC}	Q inputs at GND, Other inputs V _I = V _{CC} or GND	5.5 V		2.3	4.8		8	mA
	Q inputs open, Other inputs V _I = V _{CC} or GND	5.5 V			8		80	µA
C _i	V _I = V _{CC} or GND	5 V		3.5				pF

[†] Not more than one output or input should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	1.5	12	16.5	1.5	18.6	ns
t _{PHL}			1.5	10.4	14.4	1.5	16.3	
t _{PLH}	\overline{G}	$\overline{P} = \overline{Q}$	1.5	6.9	9	1.5	10	ns
t _{PHL}			1.5	6.3	8.6	1.5	9.5	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (INPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	1.5	8.1	11.1	1.5	12.6	ns
t _{PHL}			1.5	7.1	10.1	1.5	11.3	
t _{PLH}	\overline{G}	$\overline{P} = \overline{Q}$	1.5	4.9	6.6	1.5	7.4	ns
t _{PHL}			1.5	4.8	7.1	1.5	7.8	

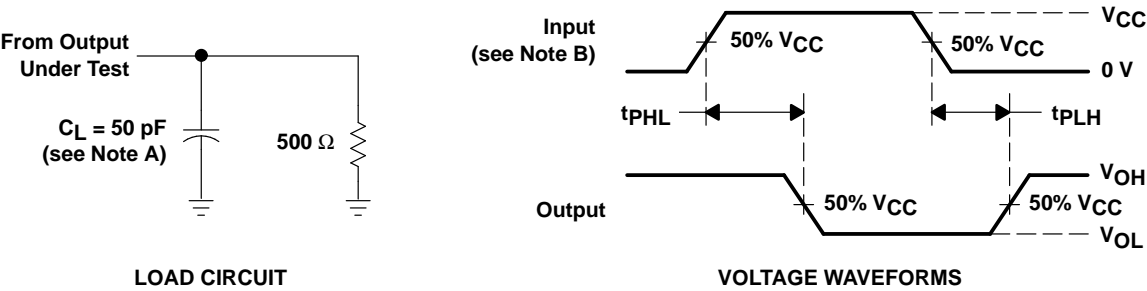
74AC11520
8-BIT IDENTITY COMPARATOR

SCAS025C – JULY 1987 – REVISED APRIL 1996

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	42	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

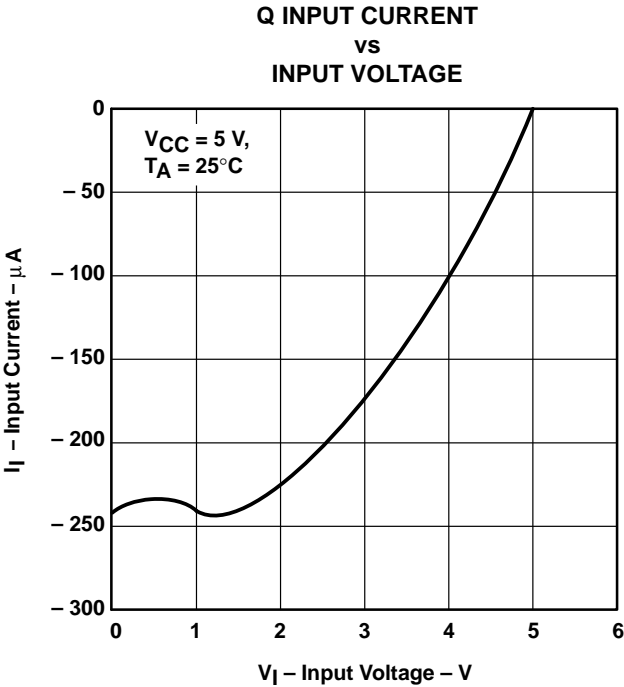


Figure 2

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.