Minimizing Output Skew Using Ganged Outputs

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Introduction

The purpose of this application report is to help designers use existing clock-driver products to drive large loads and maintain a minimum amount of skew between outputs of the device. The emphasis of this report will be on using parallel, or ganged, outputs to drive loads.

Skew Definitions

Output Skew – $t_{sk(o)}$

Output skew is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs. This parameter is useful when considering the distribution of a clock signal to multiple targets.

Pulse Skew – $t_{sk(p)}$

Pulse skew is defined as the difference between the propagation delay times t_{PLH} and t_{PHL} on the same pin at identical operating conditions. This parameter is useful when considering the output duty cycle characteristics of a device.

Process Skew – $t_{sk(pr)}$

Process skew is defined as the difference between propagation delay times on any two samples of an integrated circuit at identical operating conditions. This parameter addresses the difference in propagation delay times due to process variations.

Board Skew

Board skew is introduced into the clock system by unequal trace lengths and loads. It is independent of the skew generated by the clock driver. It is important to keep line lengths equal to minimize board skew.

When measuring propagation delays to determine the parameters $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$, the device(s) must be tested under identical operating conditions such as temperature, power supply voltage (V_{CC}), output loading, and input edge rates.

Ganged Outputs

As system frequencies increase, the need to minimize skews of clock drivers becomes critical to overall system performance. Existing non-PLL-based clock driver products deliver guaranteed output skews ($t_{sk(o)}$) in the 500-ps to 1-ns range. It is possible to use these low-skew clock drivers in a way that eliminates the output skew of the device. This can be achieved by using parallel, or ganged, outputs. Two or more outputs ganged (connected to a single transmission line) create a single clock source for all the target devices. Output skew of the clock driver is eliminated, and the drive capability is increased.

Performance Evaluation

To evaluate the impact of connecting all the outputs of a device to a single transmission line, a test board with traces of equal length to and from the inputs and outputs of the device was constructed. Using traces of equal length prevents board skew from being introduced into the system.

Various tests were performed on the CDC209 and CDC208 to evaluate their changes in performance when one output was used to drive a load versus four or eight ganged outputs. The dc-drive capability increases as more outputs are used to drive the load. Figures 1 and 2 show V_{OH}/I_{OH} and V_{OL}/I_{OL} curves displaying the difference between one, four, and eight outputs.

CDC209
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

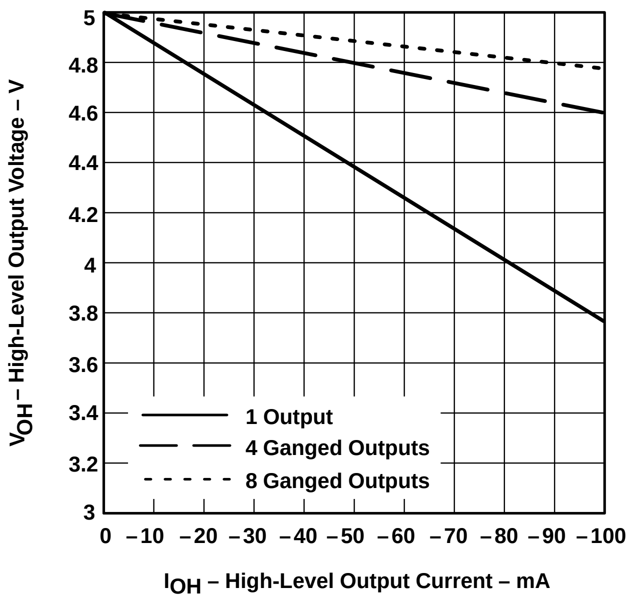


Figure 1

CDC209
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

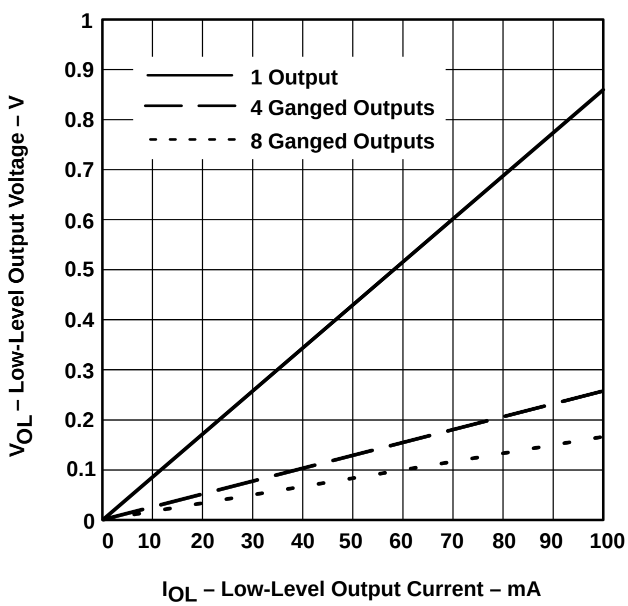


Figure 2

Figure 3 shows the difference in supply current versus operating frequency for four and eight ganged outputs.

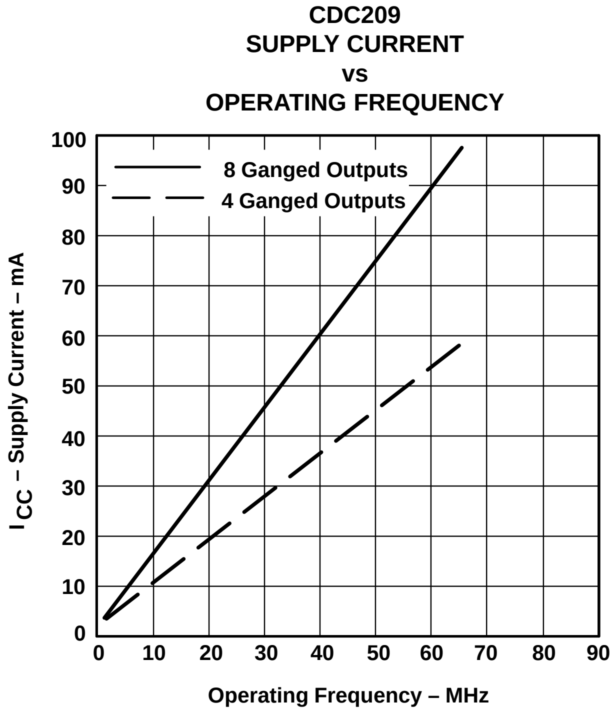


Figure 3

Figures 4 and 5 show the difference in t_{PLH} and t_{PHL} versus capacitive loading for one, four, and eight ganged outputs.

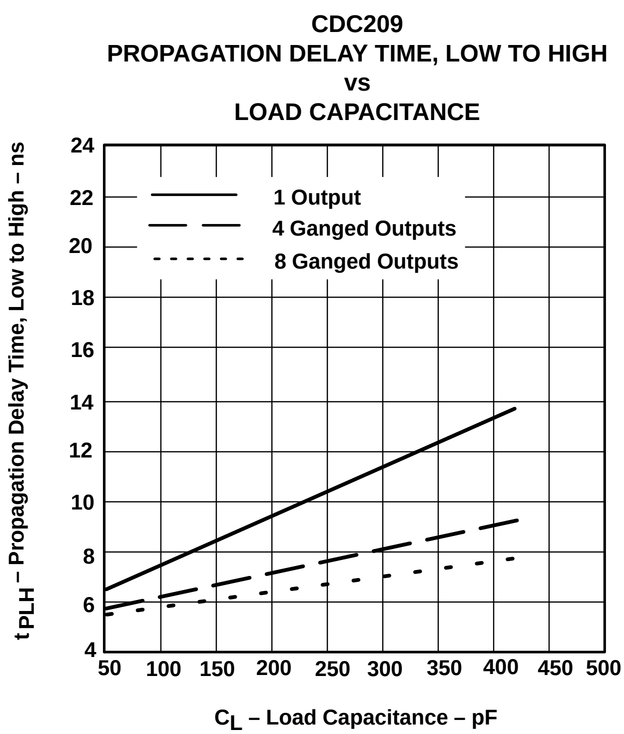


Figure 4

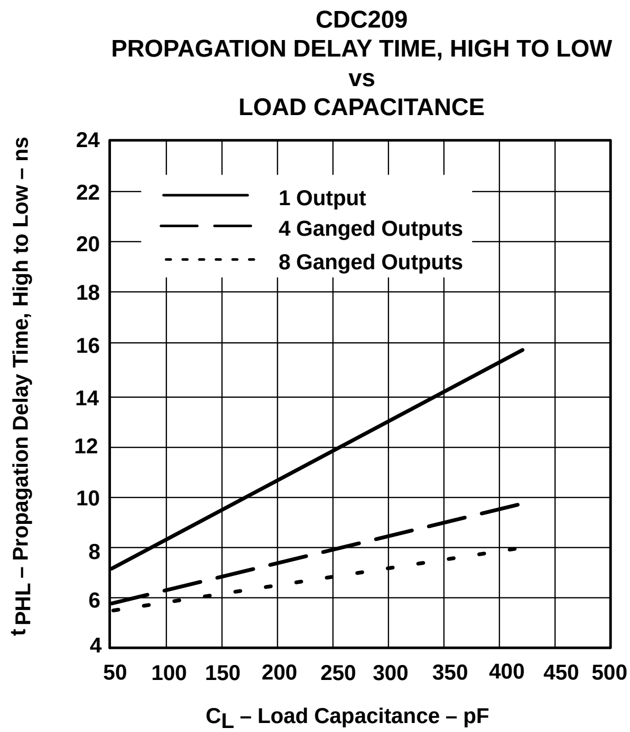


Figure 5

Figure 6 shows the difference in output waveforms of a CDC209 for one, four, and eight ganged outputs driving a 470-pF load in parallel with 500 Ω.

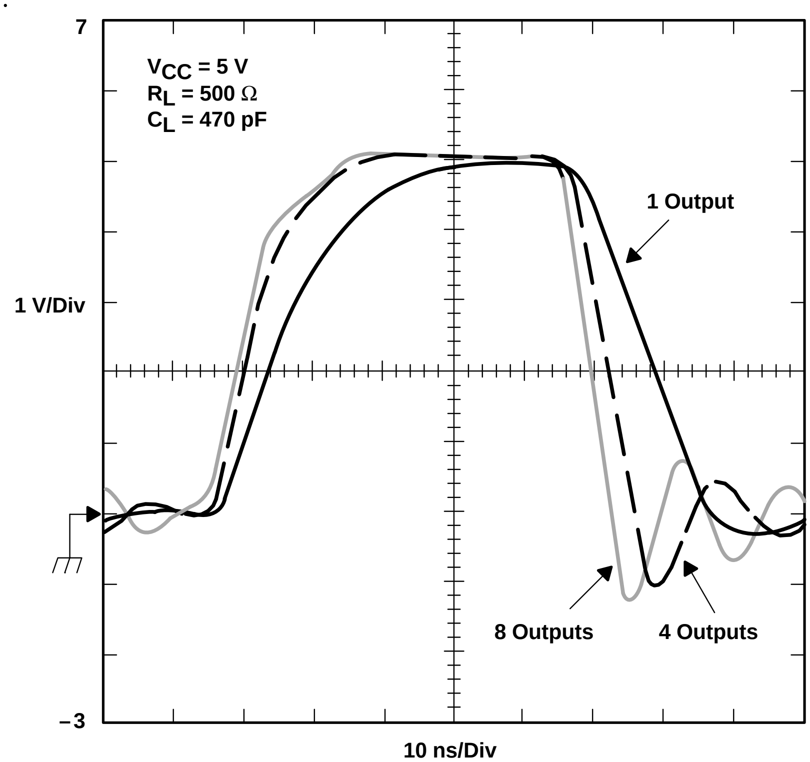
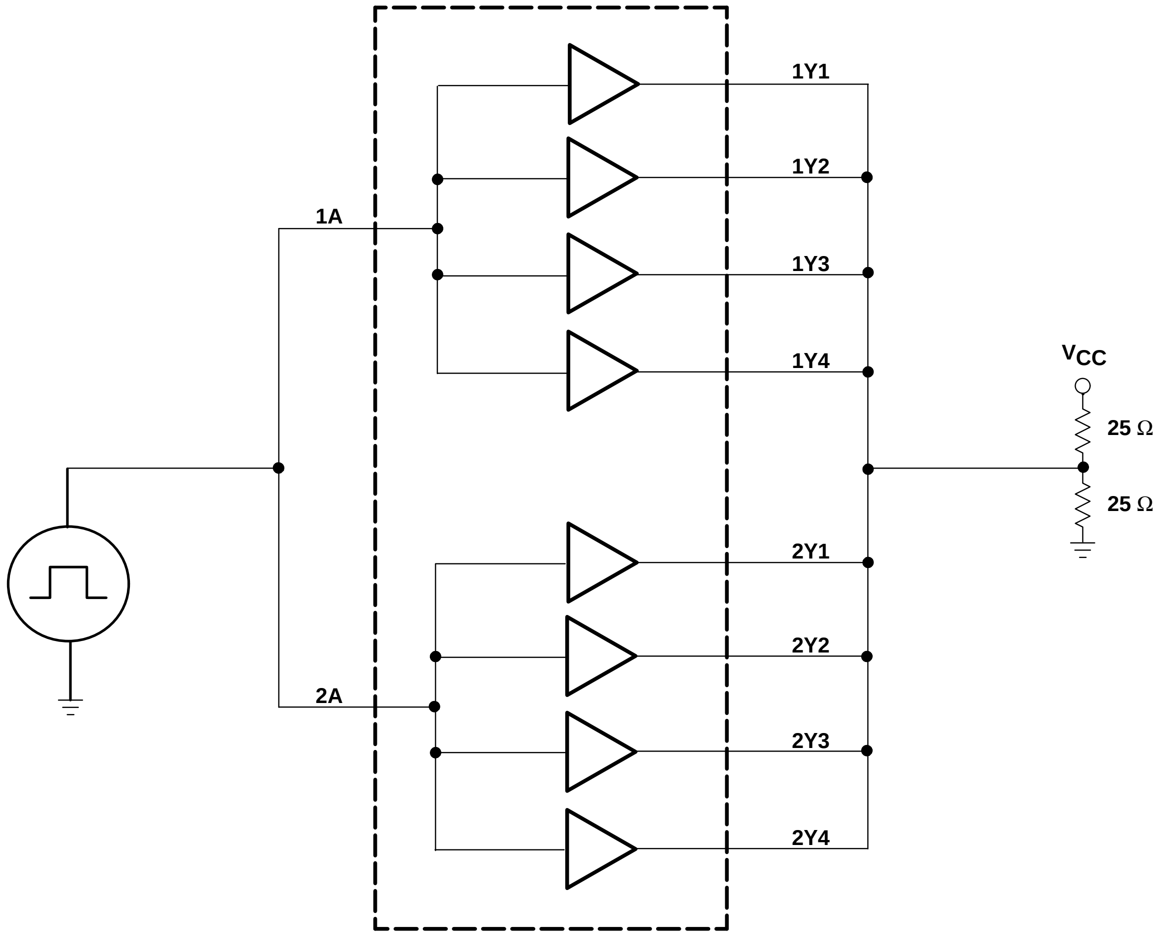


Figure 6. CDC209 Output Waveforms

Reliability

A life test of 1000 hours was also performed on 52 devices using the circuit shown in Figure 7. No failures were observed.



NOTES: A. Life test conditions: V_{CC} = 7 V, T_A = 150°C, input frequency = 10 MHz
B. It is very important to keep all of the input and output transmission lines equal length to prevent skew from being introduced.

Figure 7. Test Circuit

Applications

One application for ganged outputs is a backplane or bus on a motherboard. A backplane usually requires a single system clock capable of driving multiple plug-in boards. Ganged outputs are very effective at driving capacitive loads distributed along a single transmission line.

Great care must be taken when connecting more than one output to a single transmission line. The length and impedance of the transmission lines from each output to the point of intersection must be matched. The same attention must be given to the input traces if the outputs are driven from multiple inputs. If the lengths and impedances are not matched, a shelf may be visible in the output waveform.