Application and Design Considerations for the CDC5XX Platform of Phase-Lock Loop Clock Drivers

Grant E. Ley
Advanced System Logic – Semiconductor Group

SCAA028
April 1996

SCAA028
April 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Illustrations

List of Tables

Introduction

Today's high-speed system designs require stringent propagation and skew parameters. With system clock frequencies exceeding 50 MHz, the designer must consider clock skews to maintain desired system performance. Clock skew reduces the usable amount of time in each clock cycle and can force designers to ensure restrictive setup- and hold-time requirements for clocked components.

To meet the designer's need for high-performance clock system components, Texas Instruments (TI) has developed the CDC5XX platform of phase-lock loop (PLL) clock drivers. These clock drivers operate at 3.3-V V_{CC} and offer excellent performance with respect to skew and jitter. The CDC5XX platform of PLL products includes the CDC586, CDC2586, CDC582, CDC2582, CDC536, and CDC2536.

The CDC586 provides a TTL-compatible clock input and 12 LVTTL-compatible outputs, while the CDC582 provides a differential low-voltage pseudo-ECL (LVPECL) clock input and 12 TTL-compatible outputs. The CDC2586 and CDC2582 provide the same functions as the CDC586 and CDC582 respectively, but also include internal series-damping resistors to improve signal integrity without increasing component count for applications that require series termination. The CDC536 is a scaled version of the CDC586, providing TTL-compatible inputs and six LVTTL-compatible outputs. The CDC2536 is the series-damped version of the CDC536.

This application report details the functions and features of the CDC5XX platform of PLL clock drivers. Topics such as device configuration, board layout, and other design considerations are discussed to aid the clock distribution network designer.

Definitions

Output Skew

Output skew, $t_{sk(o)}$, is the difference between two concurrent propagation delay times that originate from a single input, or multiple inputs switching simultaneously and terminating at different outputs.

This parameter is useful when considering the distribution of a clock signal to multiple targets.

Process Skew

Process skew, $t_{sk}(pr)$, is the difference between identically specified propagation delay times on any two samples of an integrated circuit at identical operating conditions.

This parameter quantifies the skew-induced variations in the integrated circuit (IC) manufacturing process, but not by variations in supply voltage, ambient temperature, output loading, input frequency and edge rate, etc.

Limit Skew

Limit skew, $t_{sk(l)}$, is the difference between the greater of the maximum specified propagation delay times, t_{PLH} and t_{PHL}, and the lesser of the minimum specified propagation delay times, t_{PLH} and t_{PHL}.

Limit skew is not directly observable on a device; but, rather, it is a calculated value from the data sheet limits of t_{PLH} and t_{PHL}, This parameter quantifies the variation in propagation delay times over the entire range of supply voltages, ambient temperature, output loading, and all other specified operating conditions, such as input frequency, input duty cycle, and edge rates. All other device skew specifications, $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$, are subsets of the limit skew, and therefore are never greater than $t_{sk}(l)$.

Jitter

Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse.

Peak-to-Peak Jitter

Peak-to-peak jitter, sometimes referred to as period or long-term jitter, is the absolute maximum difference in the periods of any two cycles of a continuous clock pulse. Peak-to-peak jitter defines an upper bound on the cycle-to-cycle jitter.

RMS Jitter

RMS jitter is a statistical method of measuring device jitter performance. It is calculated as the standard deviation of a large sample set of period measurements. If a PLL exhibits a Gaussian distribution with respect to jitter, the peak-to-peak jitter can be calculated as six times the RMS jitter.

Features and Functional Description

Features

The CDC5XX platform of PLL clock drivers provides the designer with many key features and ease of use. All of the 3.3-V PLL CDCs share a common set of core features, such as:

- 3.3-V supply operation
- On-chip loop filter
- External feedback
- Distributed V_{CC} and GND pins to reduce switching noise
- 1×, 1/2×, or 2× configurable outputs
- Low-phase-error, output-skew, and jitter specifications

In addition, a variety of device-specific features provide the designer with choice and flexibility. Some of these features are:

- LVTTL or LVPECL inputs
- On-chip series-damping resistors
- Six or 12 outputs

The key features of the CDC5XX platform of PLL clock drivers are summarized in Table 1.

The core features provide many benefits to the designer. Low-phase-error, output-skew, and jitter specifications ensure reliable clock distribution, even when using multiple devices. The on-chip loop filter allows for easy implementation of the PLL and reduces overall component count necessary for traditional PLLs. The external feedback provides many options to the designer. While the feedback may be implemented directly from an output of the PLL, it can be selected from any point within the system to zero the propagation delay from the clock to that point. In addition, the external feedback, coupled with the two select inputs, provides for a variety of output configurations. Although the bank of outputs from which the feedback is derived is always at the same frequency as the input clock, the other outputs can be configured to provide either 1/2× or 2× frequency outputs. In addition, the design of these PLLs ensures an output duty cycle of 50% ± 5% regardless of input duty cycle, which can be critical for many of today's high-speed microprocessor systems.

Table 1. Device Features

DEVICE	FEATURES
CDC586 (CDC2586)	3.3-V supply operation On-chip loop filter External feedback Up to nine outputs configurable as 1/2X or 2X TTL-compatible inputs Twelve LVTTL-compatible outputs On-chip series-damping resistor option (CDC2586) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum jitter of 200 ps (peak to peak)
CDC582 (CDC2582)	3.3-V supply operation On-chip loop filter External feedback Up to nine outputs configurable as 1/2X or 2X LVPECL compatible clock inputs TTL-compatible control inputs Twelve LVTTL-compatible outputs On-chip series-damping resistors option (CDC2582) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum Jitter of 200 ps (peak-to-peak)
CDC536 (CDC2536)	3.3-V supply operation On-chip loop filter External feedback Three outputs configurable as 1/2X or 2X TTL-compatible inputs 12 LVTTL-compatible outputs On-chip series damping resistors option (CDC2536) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum jitter of 200 ps (peak-to-peak)

Functional Description

A functional block diagram of the CDC586 is shown in Figure 1. An integrated PLL synchronizes the feedback input with the input reference clock. The synchronized clock is distributed externally via four banks of three output buffers.

The voltage-controlled oscillator (VCO) operates at either two or four times the frequency of the reference input. This is determined by the output chosen for use as feedback and the configuration of the select inputs, i.e., SEL(0:1). Output banks 1Y(1:3), 2Y(1:3), and 3Y(1:3) can be configured to distribute either one-half or one-quarter the VCO operating frequency, while output bank 4Y(1:3) is fixed to operate at one-half the VCO operating frequency. The output that is used for feedback is forced to operate at the same frequency as the reference input. This also means that all other outputs in that bank are at the same frequency as the input reference clock, i.e., 1X. It is important that the VCO is operating within the specified stable frequency range (i.e., a VCO frequency of 100 to 200 MHz) to ensure device performance. This topic is discussed in greater detail in the next section.

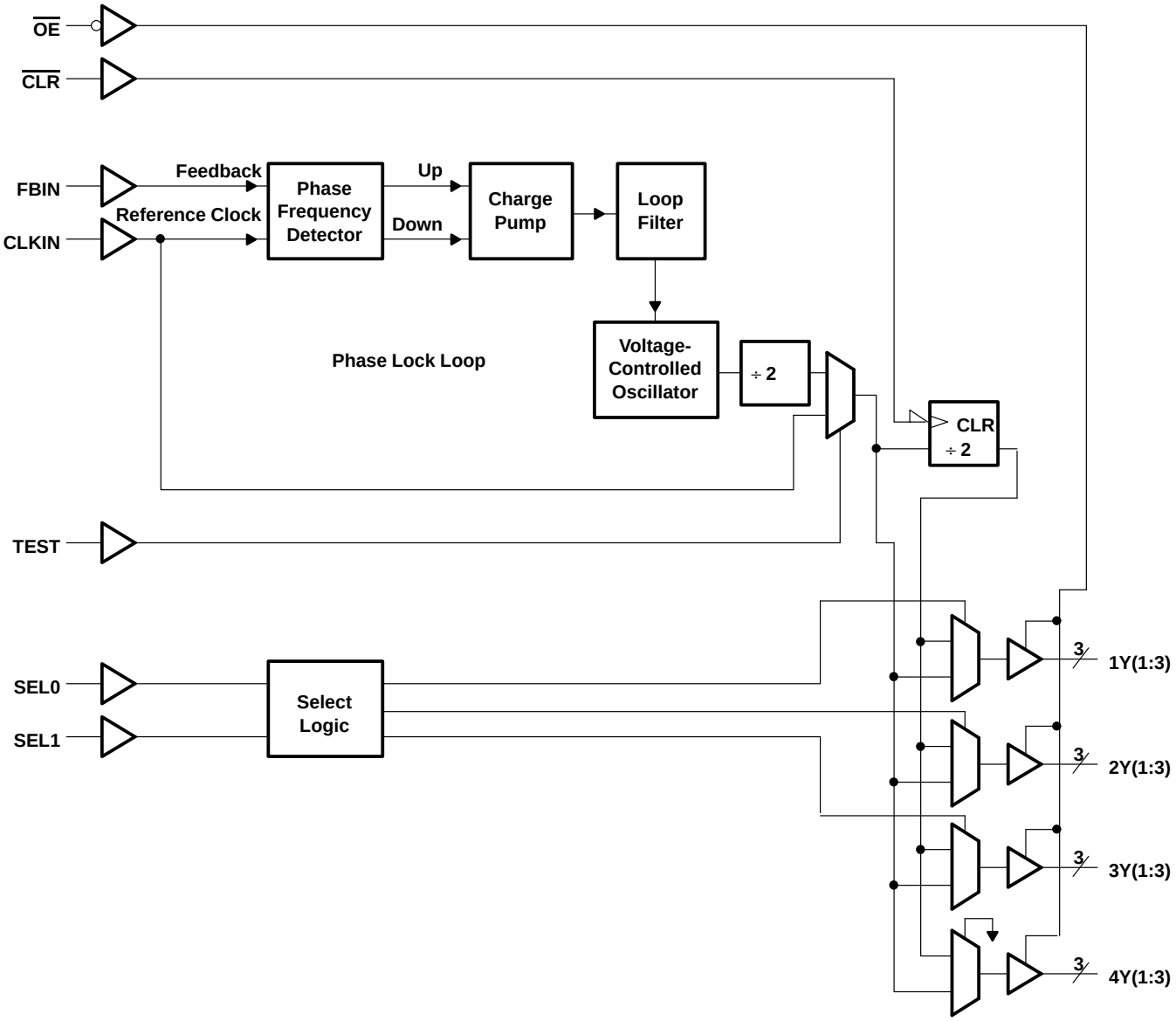


Figure 1. CDC586 Functional Block Diagram

Design Considerations

Configuring the CDC586, CDC2586, CDC582, and CDC2582

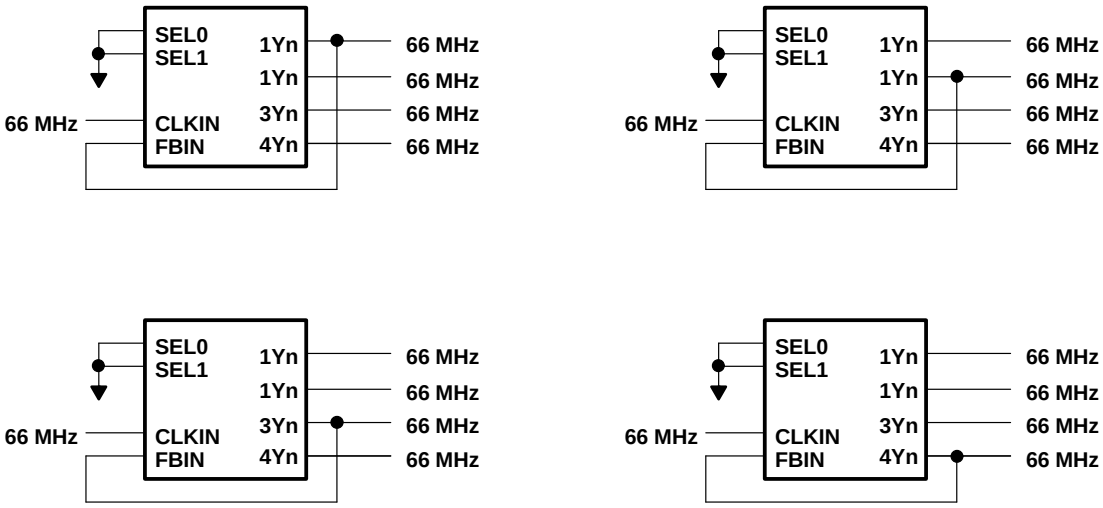
The CDC586 can be configured to provide several different output frequency relationships. All device outputs may be configured for 1× operation, and up to nine outputs may be configured for 1/2× or 2× operation. The output configuration is dependent upon the state of the SEL(0:1) inputs and the output used as the feedback.

Table 2 shows the possible output frequency relationships referenced to the VCO operating frequency. The output bank, which is used for feedback, switches at the same frequency as the input clock, which is one-half or one-fourth the frequency of the VCO per Table 2. When using a VCO/2 output for feedback, the outputs can be configured to switch at the same frequency or one-half the frequency of the clock input; when using a VCO/4 output for feedback, the outputs can be configured to switch at the same frequency or twice the frequency of the clock input. Examples of all possible output configurations are shown in Figures 2 through 4.

When using the CDC586, the designer must ensure that the VCO is operating within its recommended frequency range. Stable operation of the PLL is guaranteed within the specified operating frequencies. Degraded performance, such as higher jitter, can be observed when operating outside the specified operating frequencies. The CDC586 VCO is designed for optimal operation within the frequency range of 100 to 200 MHz. This implies that when operating with a feedback output configured for VCO/2, the input frequency range is 50 to 100 MHz; when operating with a feedback output configured for VCO/4 the input frequency range is 25 to 50 MHz.

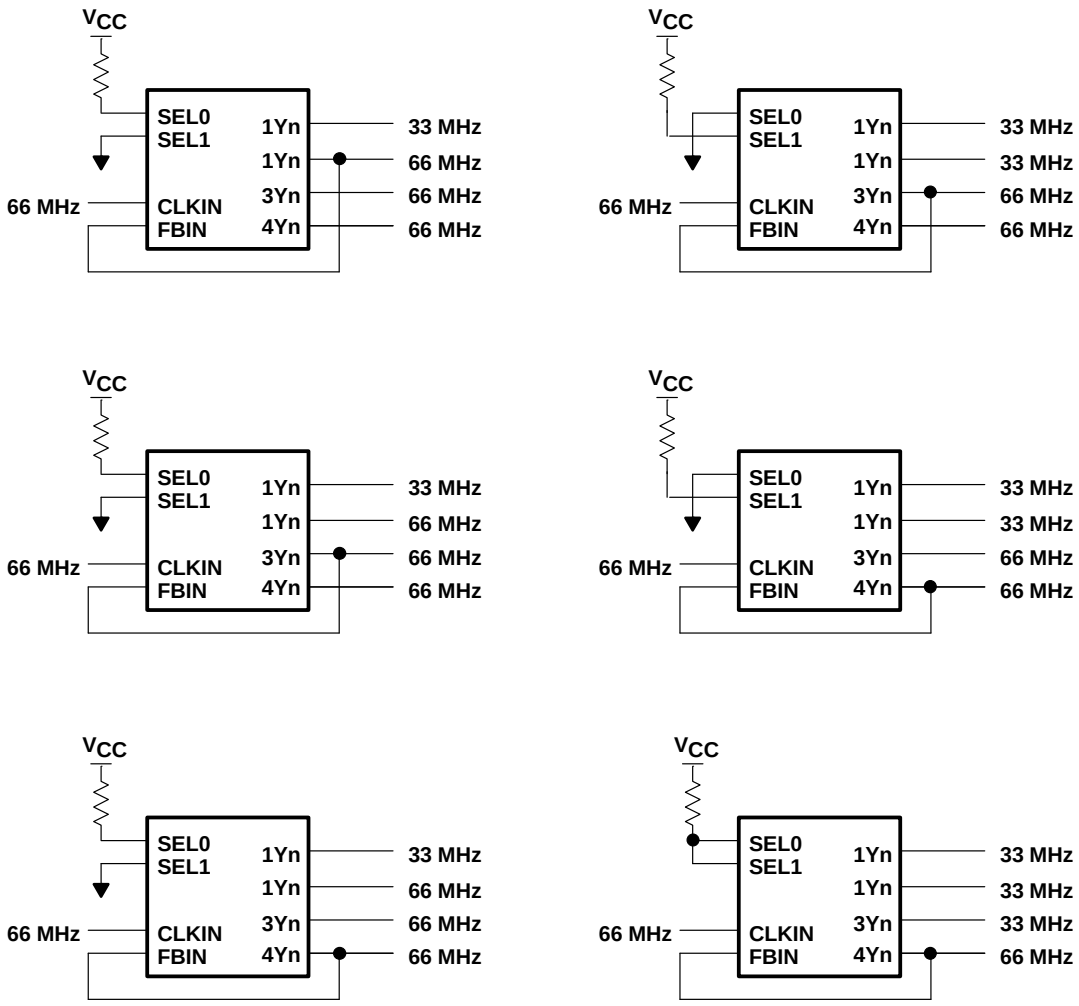
Table 2. Device Configuration

INPUTS			OUTPUTS			
$\overline{OE}$	SEL1	SEL0	1Yn	2Yn	3Yn	4Yn
H	X	X	Hi-Z	Hi-Z	Hi-z	Hi-Z
L	L	L	VCO/2	VCO/2	VCO/2	VCO/2
L	L	H	VCO/4	VCO/2	VCO/2	VCO/2
L	H	L	VCO/4	VCO/4	VCO/2	VCO/2
L	H	H	VCO/4	VCO/4	VCO/4	VCO/2



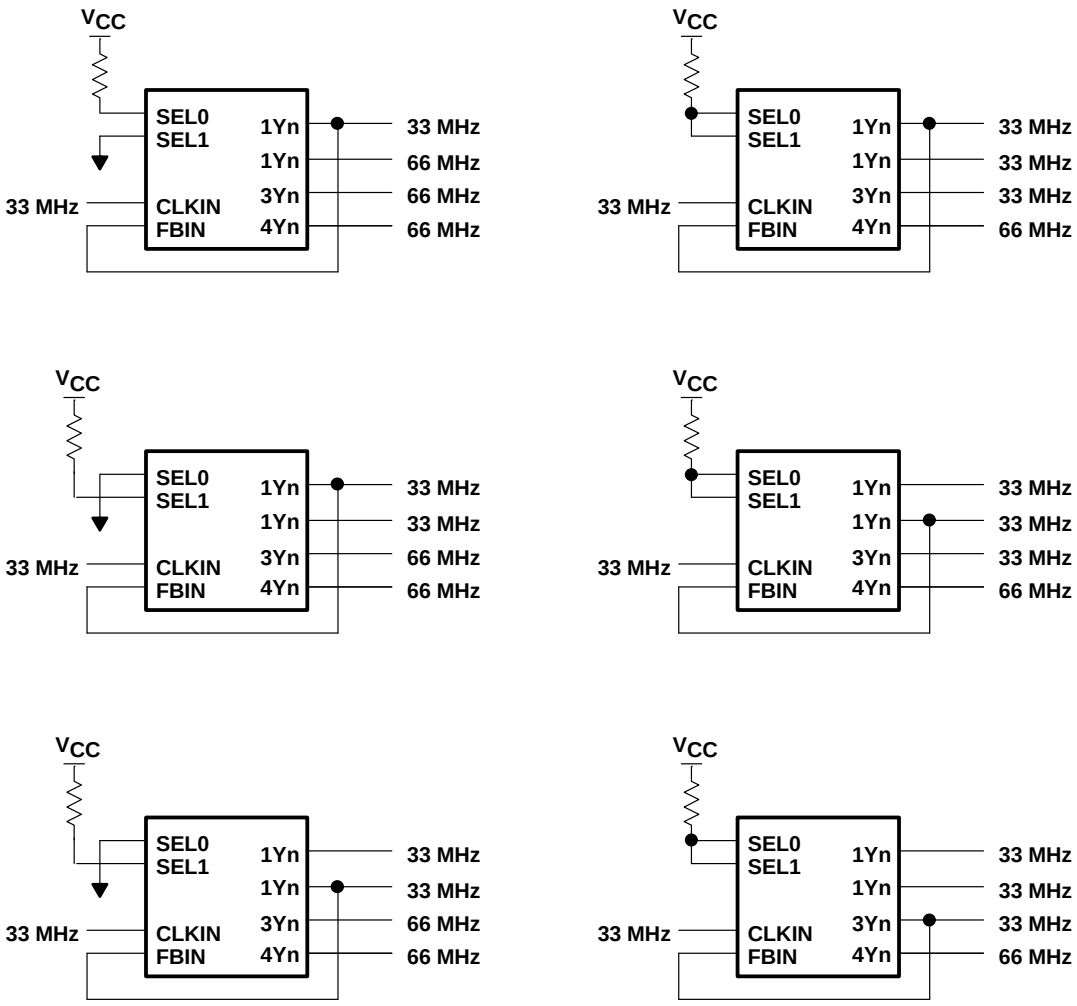
NOTE A: Minimum input frequency in 1× mode is 50 MHz. Maximum input frequency in 1× mode is100 MHz.

Figure 2. CDC586 1× Configuration



NOTE A: Minimum input frequency in 1/2× mode is 50 MHz. Maximum input frequency in 1/2× mode is100 MHz.

Figure 3. CDC586 1/2× Configuration



NOTE A: Minimum input frequency in 2× mode is 25 MHz. Maximum input frequency in 2× mode is 50 MHz.

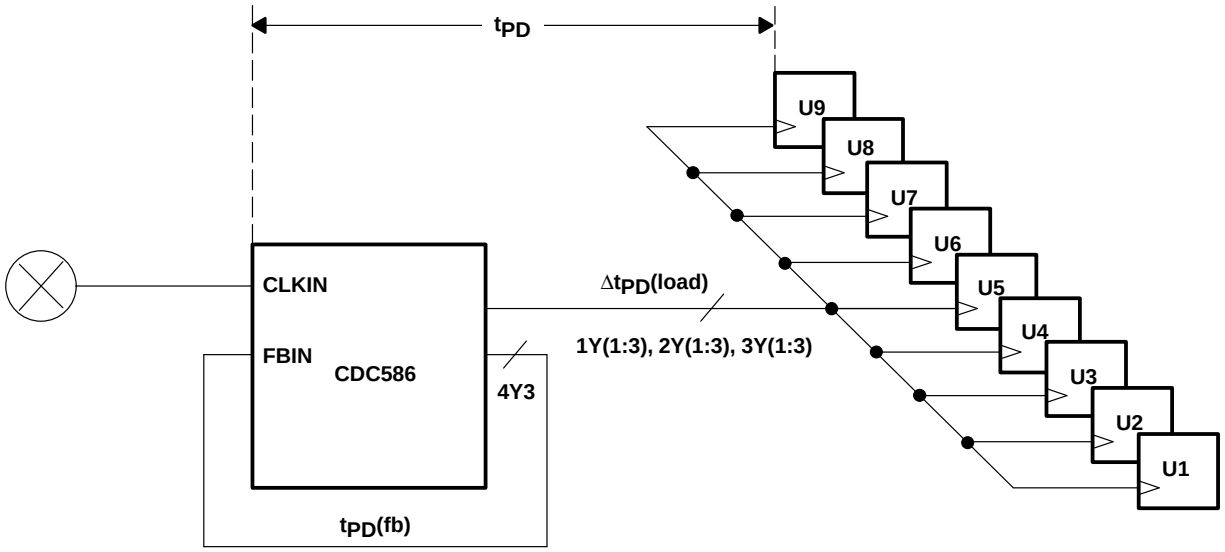
Figure 4. CDC586 2× Configuration

Zero-Propagation-Delay Operation

The external feedback allows the CDC586 to be used as a zero-delay fan-out buffer. The PLL synchronizes, in both phase and frequency, the feedback output with the input clock. This minimizes the apparent propagation delay through the device, and is specified as the static phase error. In addition, trace propagation delay from the PLL outputs to target devices can be eliminated by matching the feedback trace delay to the output to target trace delay. The effective propagation delay of a PLL with the CDC586 is shown in Figure 5.

The static phase error of the CDC586 is specified at ±500 ps across the recommended temperature and supply voltage operating conditions. Typical static phase offset for the CDC586 and CDC2586 from characterization is shown in Figure 6.

The skew between multiple devices with a common clock input is the difference between the maximum and minimum phase error of the devices. Therefore, regardless of device operating conditions, the absolute maximum skew (i.e., limit skew) across multiple devices is 1 ns, plus 200 ps jitter.



$$t_{(PD)} = [\Delta t_{PD}(fb) - \Delta t_{PD}(load)] + t_{PE}$$

Where:

t_{PE} is the static phase error of the PLL.

Figure 5. Zero-Propagation-Delay Application

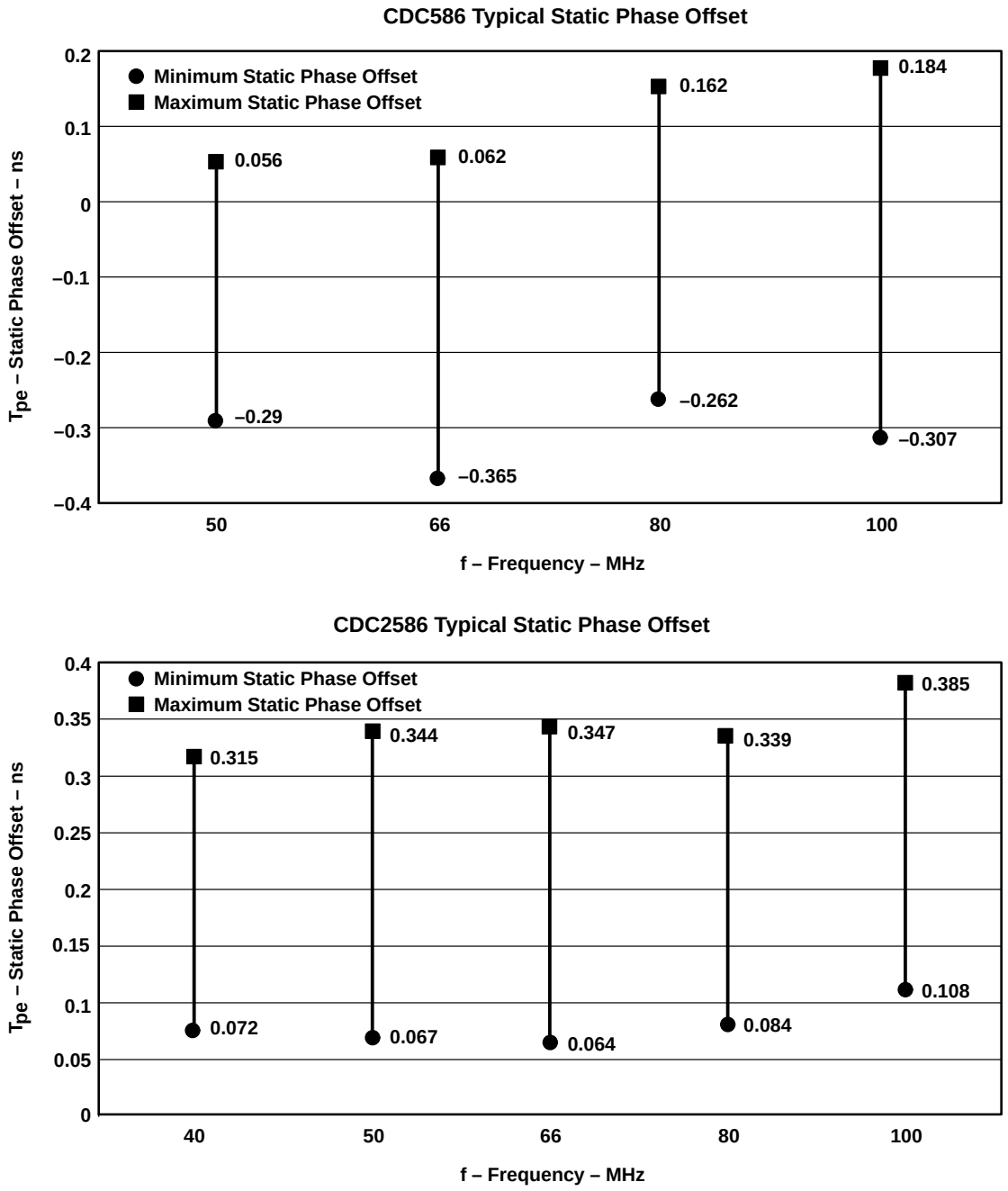


Figure 6. CDC586 and CDC2586 Typical Phase Error

Jitter

When designing clock distribution networks using PLL technology, jitter must be accounted for in the overall system timing budget. The CDC5XX platform of PLL clock drivers is designed to provide very low jitter for reliable clock distribution.

Jitter can be specified as cycle to cycle, peak to peak, or RMS jitter. Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse. Cycle-to-cycle jitter is shown in Figure 7. When specified in the picosecond range, this parameter cannot be accurately measured with today's measurement equipment; therefore, most devices are specified using peak-to-peak or RMS jitter.

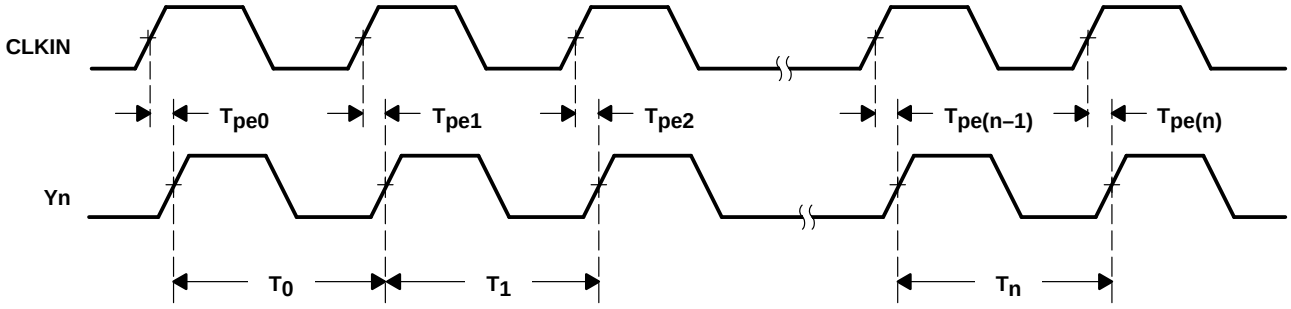
Peak-to-peak jitter, sometimes referred to as period or long-term jitter, is the absolute maximum difference in the periods of any two cycles of a continuous clock pulse. The peak-to-peak jitter defines an upper bound on the cycle-to-cycle jitter, however, due to the nature of the PLL, it is unlikely that the maximum variation in the output period occurs between consecutive cycles.

RMS jitter is a statistical method of measuring device jitter performance. It can be calculated as the standard deviation of a large sample set of period measurements. If a PLL exhibits a Gaussian distribution with respect to jitter, the peak-to-peak jitter is computed as six times the RMS jitter.

The RMS jitter can be determined by measuring the phase of the output with respect to a stable reference signal, typically the input reference clock generated from a very low jitter source, and calculating the standard deviation of the distribution. Jitter for the CDC586 platform of devices was characterized using this method. The test setup is shown in Figure 7.

When measuring jitter using this method, a very low jitter-pulse generator must be used so that its contribution to the measurement is negligible. The HP8133A provides an output signal with 1 to 1.5 ps RMS jitter, which is about 10 times lower than the measured jitter of the device under test (DUT), and can be ignored.

Figure 8 shows typical jitter performance of the CDC586. The data is presented as RMS jitter. As shown, better performance is achieved with a supply voltage greater than 3.3V. VCO operating frequency also has an effect on the jitter performance, with lower jitter typically corresponding to higher VCO operating frequencies.



$$\text{Static Phase Error} = t_{pe}$$

$$\text{Mean Static Phase Error} = t_{pe} = \frac{\sum_{i=0}^{n} (t_{pe1})}{n}$$

$$\text{Jitter (RMS)} = \sqrt{\frac{\sum_{i=0}^{n} (t_{pe1} - t_{pe})^2}{n-1}}$$

$$\text{Jitter (cycle-to-cycle)} = |t_{pe1} - t_{pe0}|$$

$$\text{Jitter (cycle-to-cycle)} = MAX(t_{pe1}:t_{pen}) - MIN(t_{pe1}:t_{pe})$$

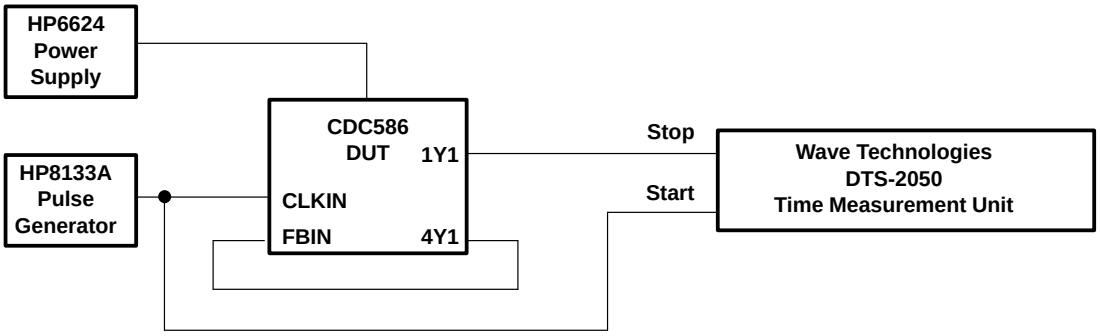


Figure 7. Jitter Measurement Methodology and Test Setup

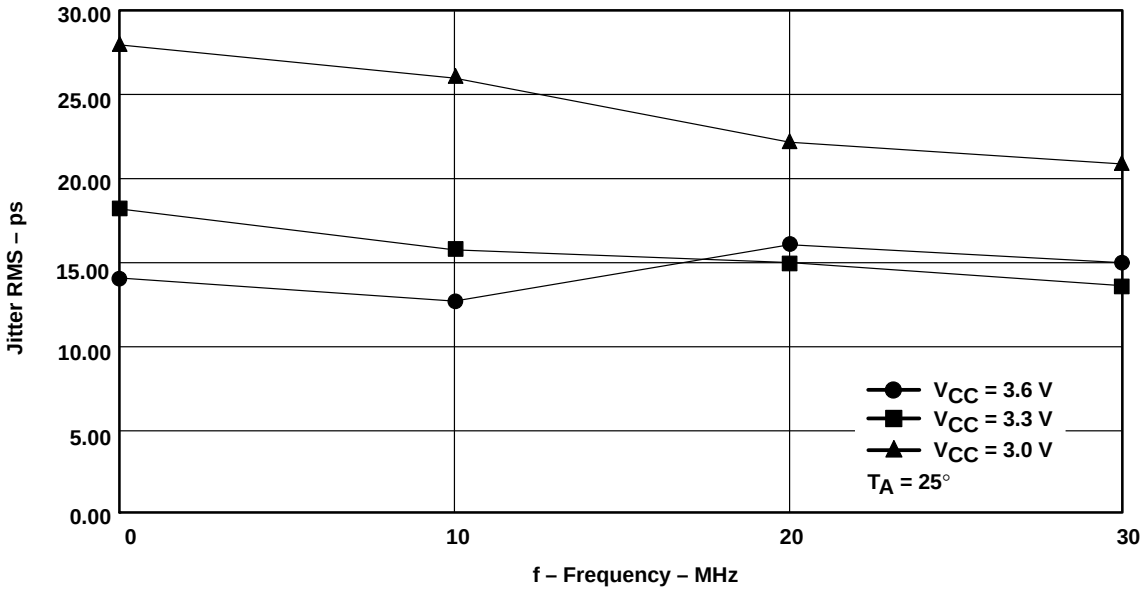


Figure 8. CDC586 Typical Jitter Performance

Driver Output Impedance

The CDC586, CDC582 and CDC536 were designed with high-drive, low impedance output drivers. Typical output impedance of the CDC5XX devices is 10 Ω. This provides sufficient driver strength to drive properly terminated 50 Ω parallel transmission lines.

For point to point clock distribution applications series termination is recommended. Series termination provides excellent signal integrity without the additional dc current consumption required for parallel termination. Several examples of series termination are shown in Figure 9.

Figure 10 shows the simulation results of a CDC586 output buffer driving a single series-terminated 50 Ω transmission line, a CDC586 output buffer driving two series-terminated 50 Ω transmission lines in parallel, and a CDC586 output buffer driving four series terminated 70-Ohm transmission lines in parallel. For the point-to-point example, the series resistor, Rs, can be determined by Zo = Ro + Rs, where Zo is the characteristic impedance of the transmission line and Ro is the output impedance of the driving buffer. For the case where multiple lines are driven, the series resistor can be determined by Z(eff) = Ro + Rs(eff), where Z(eff) is the parallel combination of the characteristic impedance of the transmission lines and Rs(eff) is the parallel combination of the series resistors, Rs.

The typical output impedance of the CDC25XX devices is 40 Ohms. In many point-to-point clock-distribution applications, the CDC25XX devices will provide sufficient damping of reflected waveforms to meet the desired signal integrity without the need for an external series resistor. However, the system designer should evaluate signal integrity through the use of simulation, such as SPICE. Texas Instruments provides input and output buffer HSPICE models for CDC devices, on customer request.

Typical V/I characteristics for both the CDC5XX and CDC25XX are shown in Figure 11.

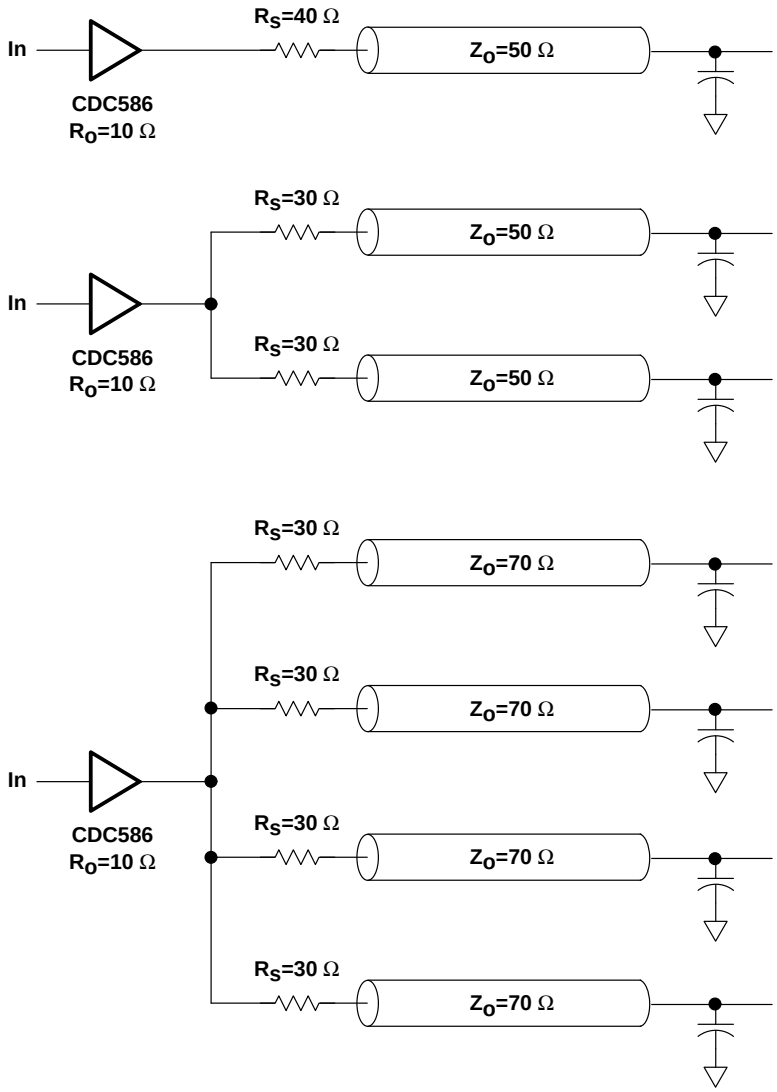
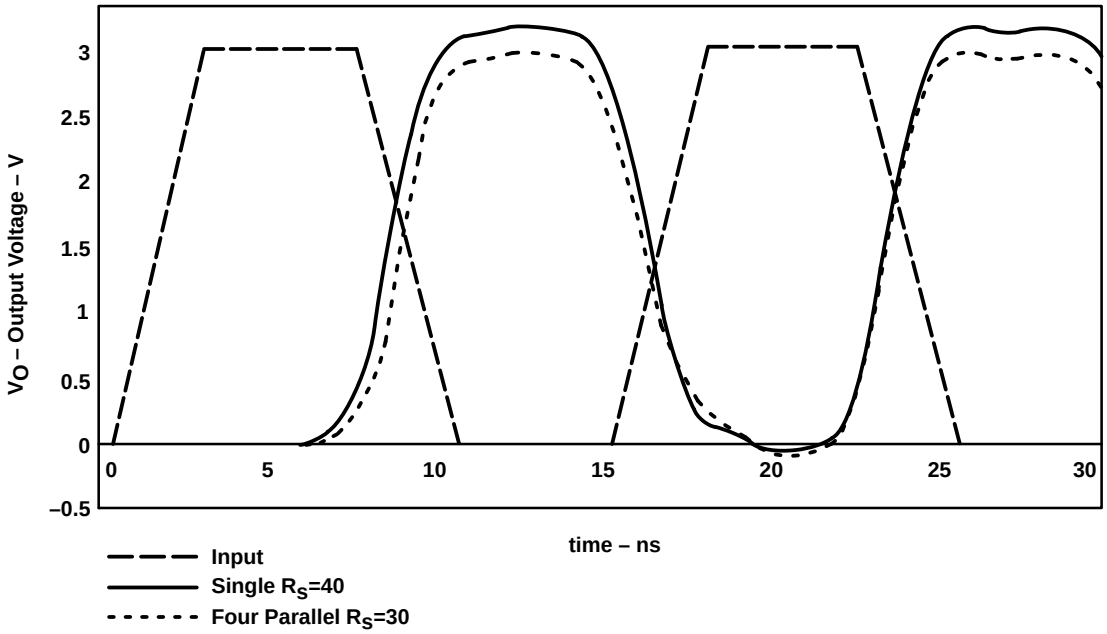


Figure 9. Series Termination Examples



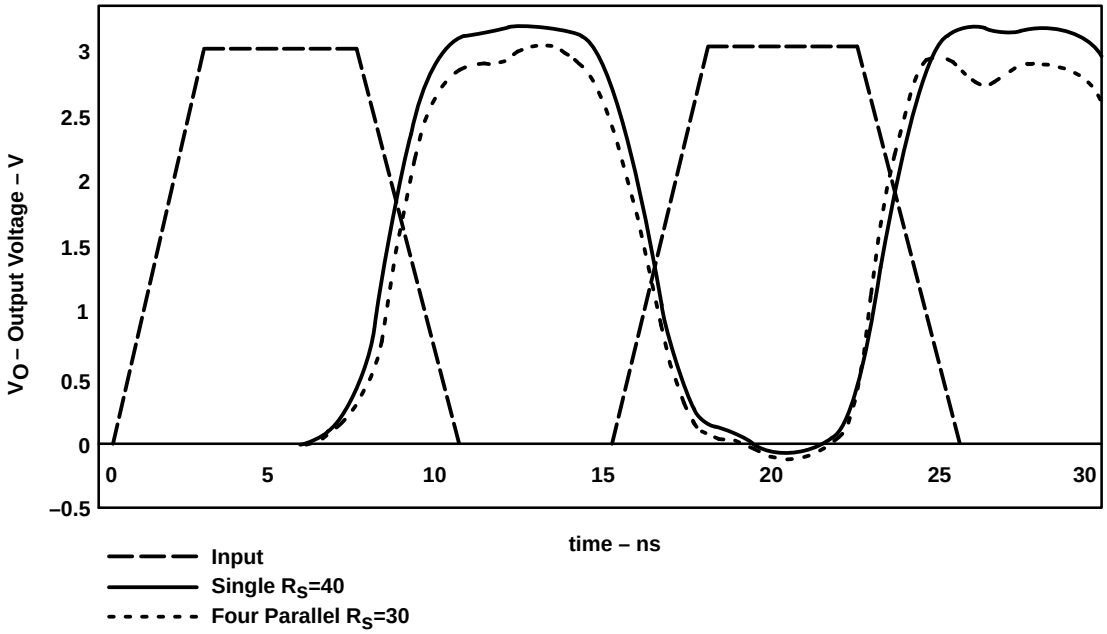


Figure 10. CDC586 Transmission Line Analysis

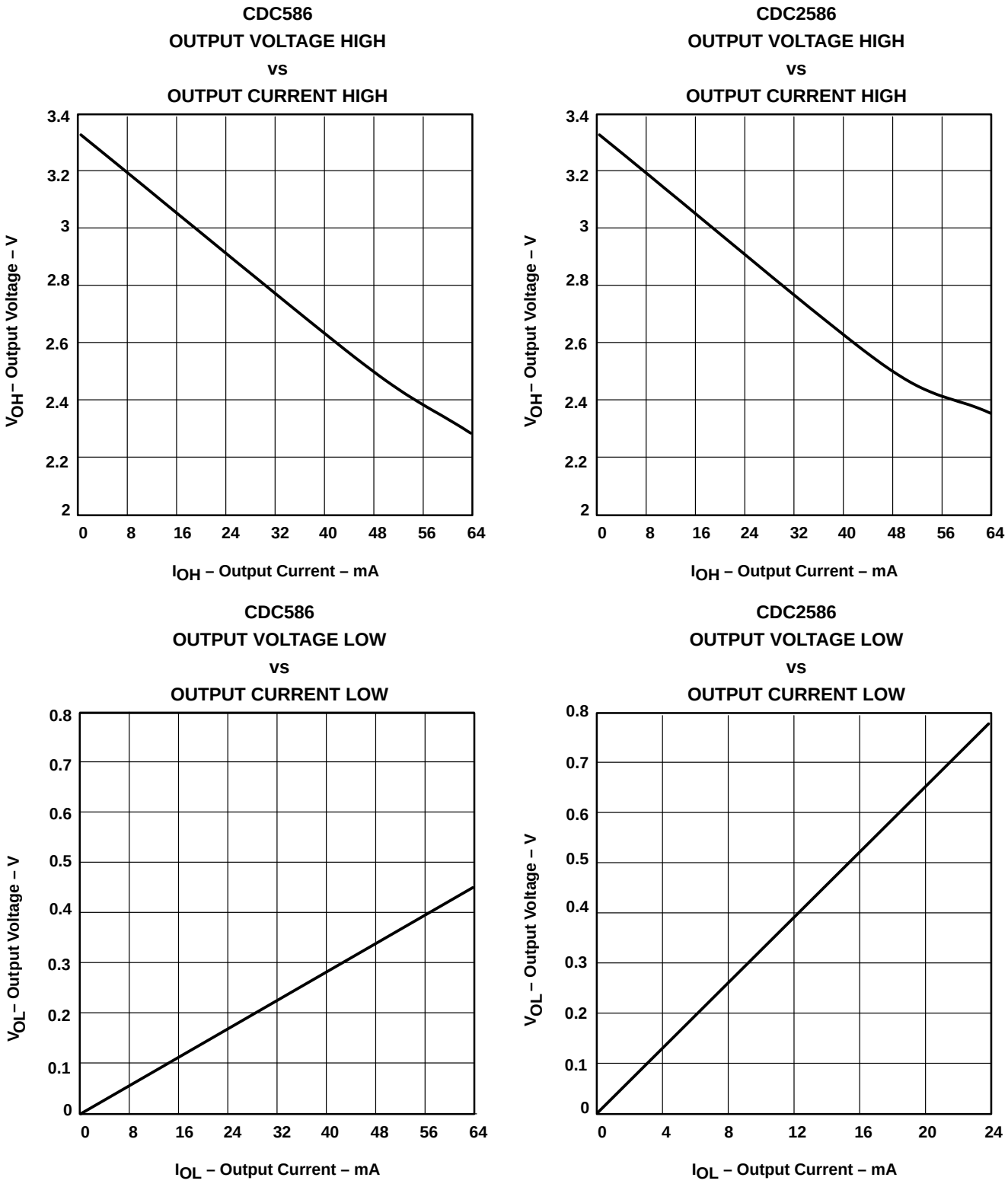


Figure 11. CDC586 and CDC2586 Typical V/I Curves

Power Supply and Decoupling Considerations

The CDC586 platform of clock drivers uses an integrated analog PLL to synchronize the outputs with the input reference clock. The performance of the analog portion of the circuit (i.e., the PLL) can be sensitive to noise on the supply voltage. Noise on the supply voltage can dramatically increase the jitter of the PLL. Since jitter must be accounted for in the overall system skew budget, this increase in jitter can cause system stability problems.

For best performance results, noise should be minimized on the analog power and ground pins of the CDC5XX and CDC25XX devices by using a filter. The CDC5XX platform of devices provides separate analog V_{CC} and GND pins, which allows the user to isolate the PLL from noisy voltage planes. For the CDC586/2586/582/2582, pins 43 and 46 are the analog V_{CC} pins for the PLL, while pins 47 and 49 are the analog grounds for the PLL. These devices are most susceptible to noise within the 10 KHz-to-1 MHz range; therefore, the filter should be designed to attenuate this frequency range. A low passfilter and local decoupling, as shown in Figure 12, can be used to isolate the PLL from noise sources.

The filter may be designed using a choke, a low-ohm resistor, or a ferrite bead. The choke should provide the best overall filter performance; however, a lower cost filter can be implemented using a ferrite bead or resistor. Ferrite beads that are primarily resistive are recommended for the best attenuation. If a single bead does not provide sufficient attenuation, two to three beads may be connected in series to improve filter performance. A low-ohm resistor, i.e., 10 Ω to 15 Ω , may be used instead of the ferrite to provide better low-frequency attenuation at a lower cost than using a choke. The analog circuits of the CDC586 typically consume about 1 mA of current, with a worst-case consumption of 5 mA. The dc voltage drop across the analog filter should be considered when evaluating filter options. For a ferrite bead, the dc voltage drop is nominally zero, and for a 15-Ω resistor, the maximum dc voltage drop would be 75 mV.

The 0.1 μF and 0.001 μF capacitors provide local decoupling of the analog supply. In addition, the digital supply pins should also be decoupled using 0.001-to 0.1-μF capacitors. For decoupling, low-inductance ceramic chip capacitors are recommended. For best results, all components, (both decoupling capacitors and filter components) should be placed as close as possible to supply pins of the device.

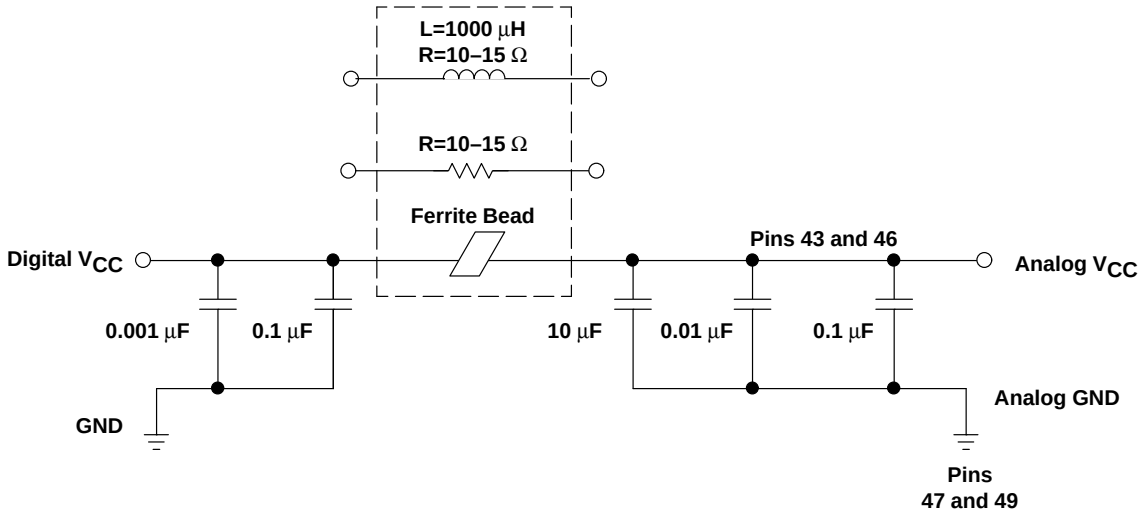


Figure 12. Analog Power Filter

References

Letter B JC–10–90–119A, Terms, Symbols, and Definitions for Skew Parameters.

Blood, William R., Jr., MECL System Design Handbook, 1983, Motorola Inc.