64-Byte FIFOs
SN74ALS2232A and SN74ALS2233A

First-In, First-Out Technology

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TEXAS INSTRUMENTS

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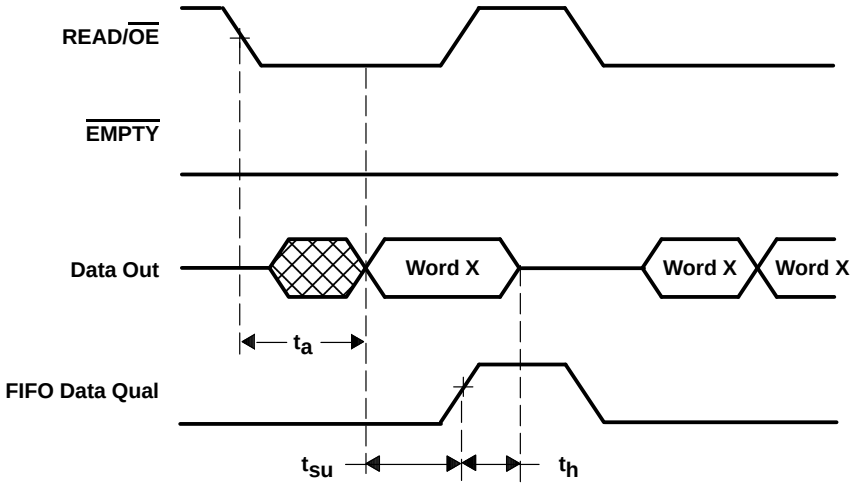
Introduction

First-in, first-out (FIFO) memories are irreplaceable bus logic when interfacing two asynchronous systems. The Texas Instruments SN74ALS2232A 64 × 18 and SN74ALS2233A 64 × 9 FIFOs are ideal solutions for many high-speed buffering needs. These bipolar devices, produced in IMPACT-X technology, come in a 28-pin PLCC and a 24-pin DIP for the ′ALS2232A and 28-pin PLCC and DIP for the ′ALS2233A.

Data is stored in a dual-port SRAM that supports transfer rates up to 40 MHz and maximum access times of 27 ns. Reads are accomplished independent of writes with separate internal addressing.

Clocks

The read enables of many FIFOs also control the active/high-impedance state of the data outputs. FIFOs using this logic must have a read-enable pulse long enough to include an access and hold time before it disables the outputs, which makes high-frequency clock design difficult (see Figures 1 and 2).



t_a = access time maximum
t_{su} = setup time minimum
t_h = hold time minimum

Figure 1. FIFO Read Control With READ/$\overline{OE}$ Logic

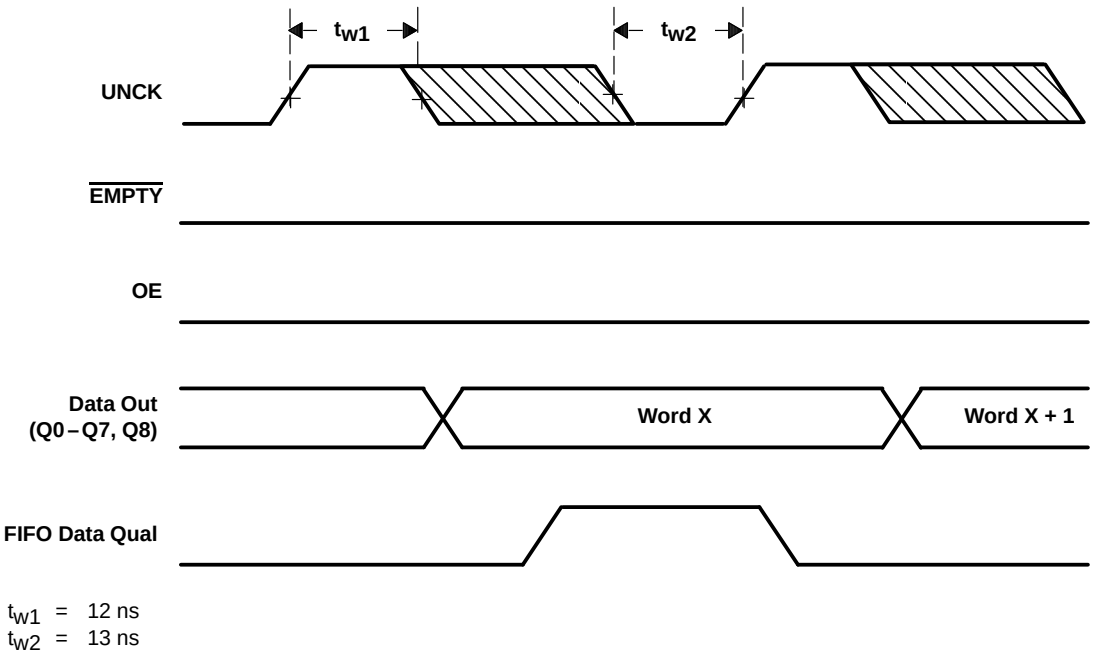


Figure 2. ′ALS2232A and ′ALS2233A UNCK Control

Texas Instruments has allowed clock generation to be simple for its FIFOs. Load-clock (LDCK) and unload-clock (UNCK) inputs are edge triggered, which makes the device more suited for use as a buffer in a data-transmission path. Fewer constraints are placed on a design with edge-triggered clocks since duty cycles are permitted to vary greatly (see Figure 2). A separate output-enable (OE) input is provided for applications requiring 3-state buses.

The LDCK and UNCK independently control all data transfers into and out of memory and can be synchronous or asynchronous. The first word loaded into an empty FIFO propagates directly to the data outputs. Any UNCK pulses that occur during an empty condition are ignored, while any LDCK pulses that occur during a full condition are ignored.

Flags

The ′ALS2232A has two flags to indicate boundary conditions of the memory: $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$. In addition to these, the ′ALS2233A has the almost-full/almost-empty (AF/AE) and half-full (HF) flags. AF/AE is high when memory contains less than nine words or more than 55 words. To distinguish between an almost-full and an almost-empty state, HF is high when memory contains more than 31 words. The extra flags are provided for applications wherein full and empty conditions should be avoided.

Noise Control

Ground bounce is a result of current surges produced by output switching. Bond wire, lead, and board inductance cause internal ground levels to fluctuate from the current surge (rise above, then dip below 0 V). Extreme ground noise that causes input levels to cross the transition threshold may be detected as clock pulses by high-speed devices. Worst-case conditions for ground bounce are high V_{CC} and outputs switching simultaneously from high to low.

The ′ALS2232A and ′ALS2233A have package-centered V_{CC} and GND pins to combat ground bounce. The shortened bond wire and lead distance reduce package inductance from conventional corner-pin configurations.

Figure 3 shows a large voltage transient that might be measured on the ground pad of any device referenced to a 0-V plane. An input at a steady high or steady low level is likely to cross the transition threshold as a result.

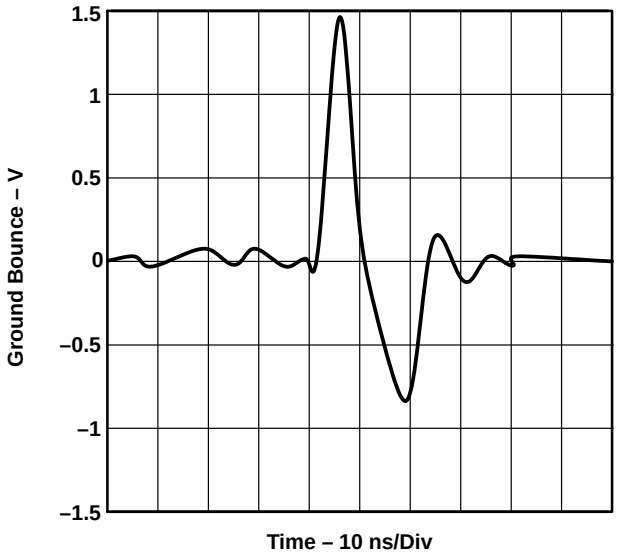


Figure 3. Noise From a GND Pad to a 0-V Plane

Figure 4 is the equivalent circuit of the clock inputs for the ′ALS2232A and ′ALS2233A. This modified RS flip-flop is more likely to pass a very quick high pulse (0 to 5 ns) caused by noise when it is in the steady low state than it is to pass a very quick low pulse when in the steady high state. The clock input one-shot structure is immune to a very quick (0 to 5 ns) low pulse when in the steady high state. For improved noise protection, LDCK and UNCK signals may be generated as inactive high with a low pulse generated for clocking.

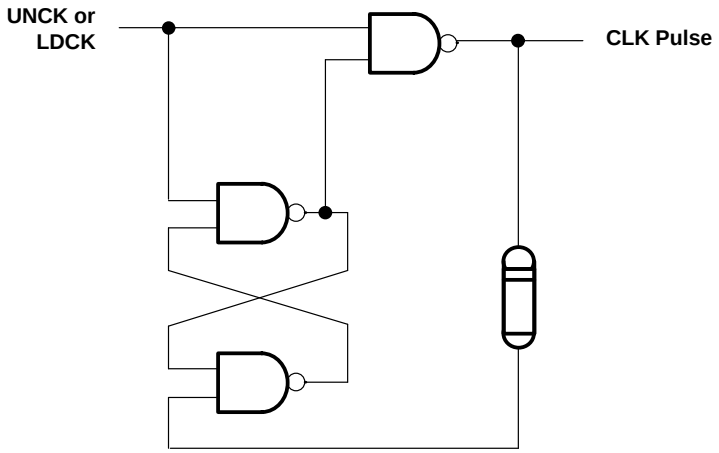


Figure 4. ′ALS2232A and ′ALS2233A Clock Input Circuit

Applications

Using the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ Flags

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ flags are provided to indicate that the FIFO is at one of its boundaries. An example of how to qualify these flags as enables for the device clocks is shown in Figure 5. Without the flip-flop qualification, a flag can cause the asynchronous generation of a clock. The two-stage synchronization alternative shown reduces the chances of a metastable output from one-stage synchronization.

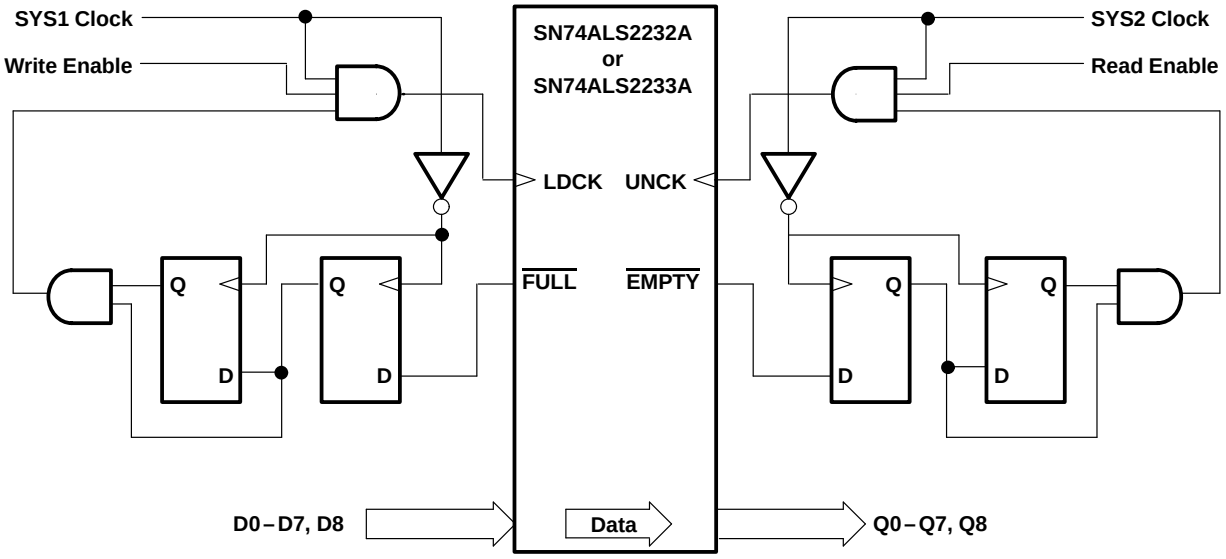


Figure 5. Clock Generation With Two-Stage Synchronization of $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$

Width Expansion

Several ′ALS2232A devices can be used in width expansion to handle datapaths with several bytes. The ′ALS2232A can likewise be expanded and also pass parity for each byte. No special control logic is needed to implement this application (see Figure 6).

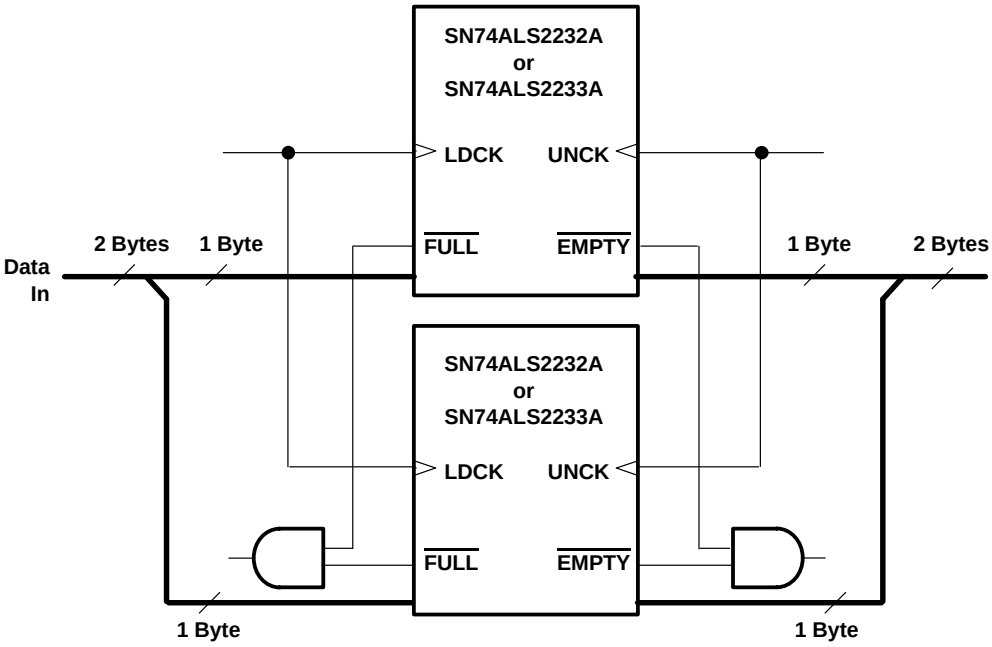


Figure 6. Width Expansion

Bus Conversion

Systems frequently require that data be converted from 1-byte buses to multiple-byte buses operating asynchronously. Figure 7 shows an 18-bit bus folded into a 9-bit bus using the ′ALS2233A. The control logic can be implemented with a TIBPAL20R4.

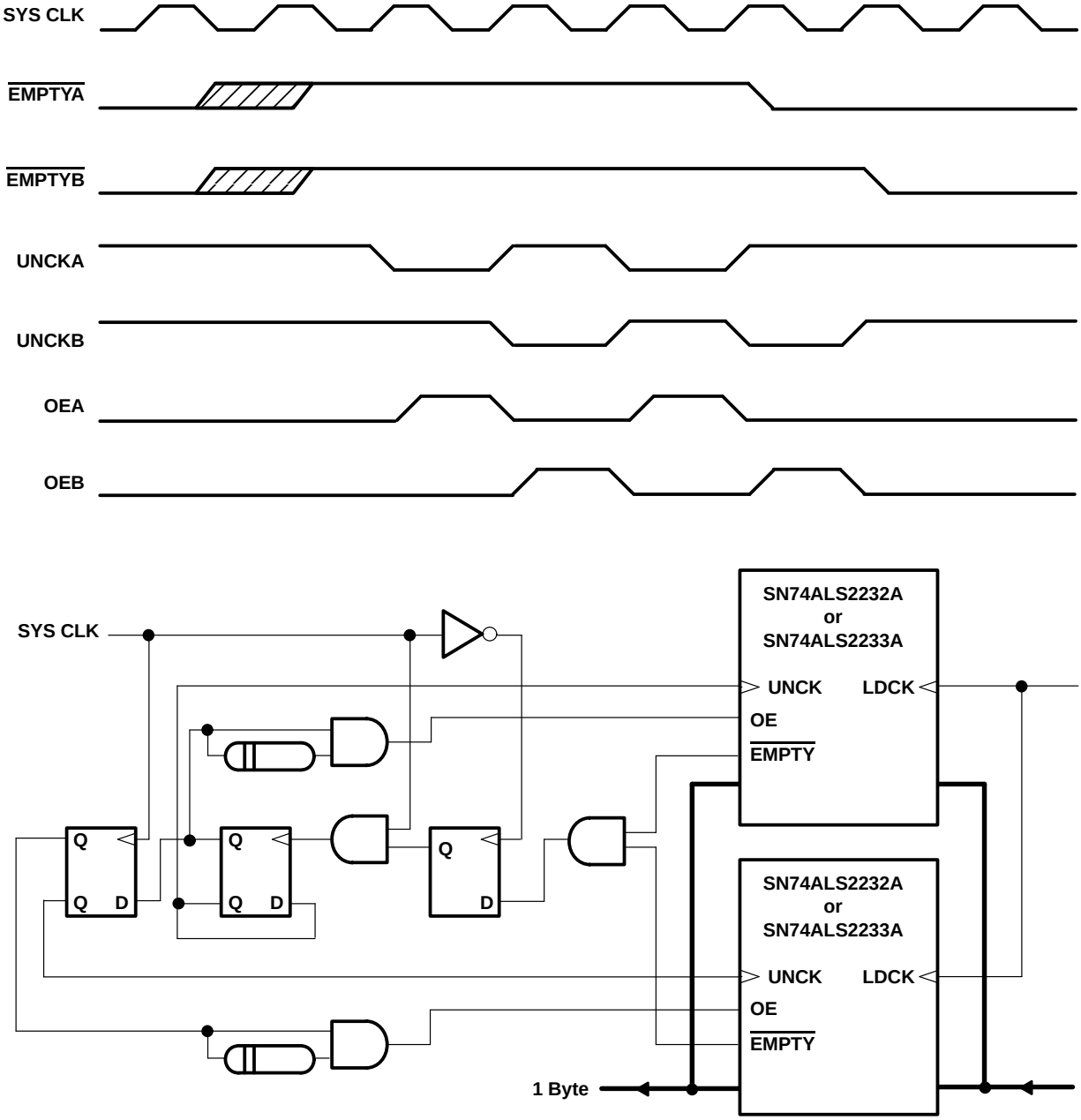


Figure 7. Bus-Folding Logic

Table 1. Terminal Functions

FUNCTION	TERMINAL NAME	DEFINITION
Control inputs	LDCK	Load clock; rising-edge clock. Writes data into the FIFO; updates the flags.
	UNCK	Unload clock; rising-edge clock. Reads data out of FIFO; updates the flags.
	OE	Output enable. Controls the active/high-impedance state of the data outputs. A high level on OE selects the active state; low selects high impedance.
	$\overline{\text{RESET}}$	Reset. Low level resets the read and write pointers to the first location and sets the flag status to empty. The FIFO must be reset after power up.
Status-flag outputs	$\overline{\text{EMPTY}}$	Empty flag. t_{PLH} transitions are controlled by LDCK. t_{PHL} transitions are controlled by UNCK or $\overline{\text{RESET}}$. FIFO read pointers are unaffected by UNCK when $\overline{\text{EMPTY}}$ is low.
	$\overline{\text{FULL}}$	Full flag. t_{PHL} transitions are controlled by LDCK. t_{PLH} transitions are controlled by UNCK or $\overline{\text{RESET}}$. FIFO memory and write pointers are unaffected by LDCK when $\overline{\text{FULL}}$ is low.
	AF/AE	Almost-full/almost-empty flag: high level when FIFO is eight locations from a full or empty condition (FIFO contains less than nine words or more than 55 words)
	HF	Half-full flag. t_{PLH} transitions are controlled by LDCK. t_{PHL} transitions are controlled by UNCK or $\overline{\text{RESET}}$. HF is at a high level when the FIFO contains more than 31 words.
Data	D0–D7 (SN74ALS2232A) D0–D8 (SN74ALS2233A)	Data inputs: data latched by LDCK into memory
	Q0–Q7 (SN74ALS2232A) Q0–Q8 (SN74ALS2233A)	Data outputs: data read from FIFO