Advanced Bus-Matching/ Byte-Swapping Features for Internetworking FIFO Applications

Tom Jackson
Advanced System Logic – Semiconductor Group

SCAA014A
March 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Illustrations

Introduction

Bus matching and byte swapping are features that Texas Instruments (TI) has added to their internetworking family of application-specific, first-in first-out memories (FIFOs). The first two FIFOs available are the SN74ABT3614 and SN74ABT3613. The bus-matching feature allows the user to dynamically select the desired bandwidth, either long-word format (36 bits), word format (18 bits), or byte format (9 bits) for mixed-bus systems. Byte swapping allows the user to reconfigure protocols for different microprocessor-based systems, such as big-endian format (i.e., RISC-based microprocessors such as the MC68000, IBM370) where the most significant bit (MSB) is 0 or little-endian format (i.e., CISC-based microprocessors such as iPAX, x86, DEC VAX) where the least significant bit (LSB) is 0 (see Figure 1). The bus-matching and byte-swapping features can be used independently or in conjunction with one another, which allows the user a wide range of possible solutions.

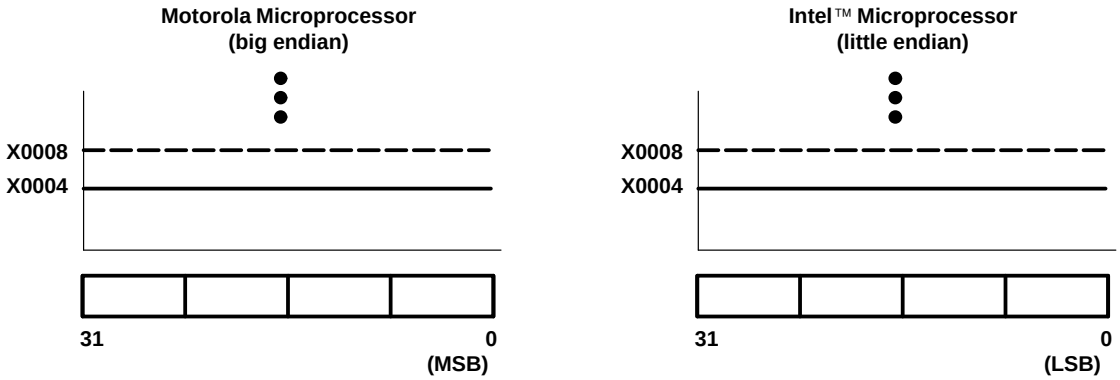


Figure 1. Big-Endian and Little-Endian Formats

Intel is a trademark of Intel Corp.

Conventional Bus-Matching Data Reads

With the evolution of 32-bit microprocessors and digital signal processors (DSPs), designers must add large complex discrete circuits to provide data continuity between mixed data-bus systems. A typical solution requires four 9-bit FIFOs and considerable board space (see Figure 2).

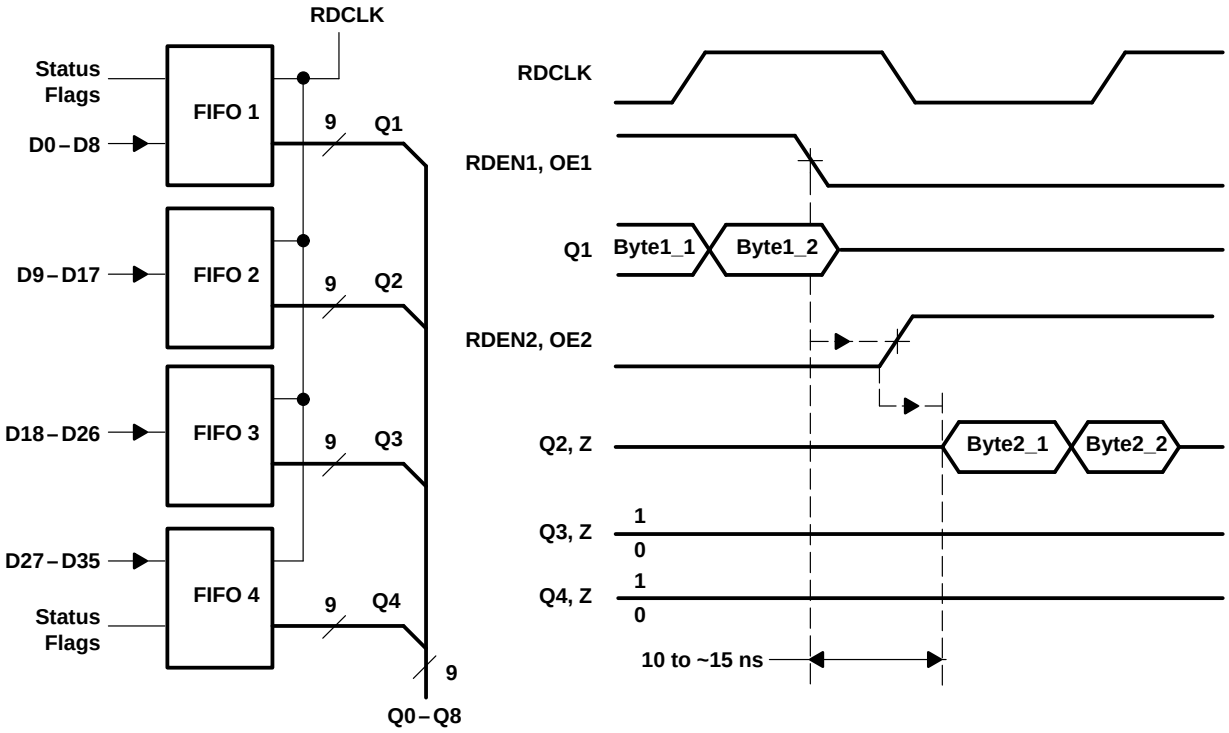


Figure 2. Data-Read Cycle for 36-Bit to 9-Bit Bus Matching

To provide bus matching from a 36-bit bus to a 9-bit bus, access time and flag synchronization are critical issues due to the combination of separate components. Figure 2 shows the required circuitry and associated timing diagram for a conventional bus-matching operation. The first byte of the long word is written into FIFO1 on D0–D8. On the rising edge of the read clock with read enable-1 (RDEN1) and output enable-1 (OE1) held high, the first byte of FIFO1 (byte 1_1) is read out. During that first read cycle, the remaining three FIFOs must be disabled. Before reading the second byte from FIFO2 (byte 2_1), the read enables and output enables of FIFO1 are asserted low, putting the FIFO outputs into 3-state, which prevents any bus-arbitration problems. FIFO1 must be disabled before FIFO2 is enabled.

In addition to the associated propagation delays of enabling and disabling the FIFOs, the typical access time of a single FIFO can range from 10 to 20 ns. To ensure proper device synchronization, the FIFO access time must be increased to allow for the propagation delays of the control signals. The increased propagation time for data reads can cause a bottleneck for data that is waiting to be written into the other FIFOs. This delay dramatically impacts system performance and data throughput. If the timing parameters are violated, the result is bus contention and lost data. To complete the long-word read, the cycle is repeated three more times. For subsequent long-word data reads, the process begins with the second byte of FIFO1 (byte 1_2). This data *ping-ponging* is prolonged and requires excessive access times and data setup and hold times to perform a single long-word read cycle. These factors contribute to reducing the effective maximum operating frequency of the system.

TI's Bus-Matching Data Reads

TI has designed the internetworking FIFOs to provide the user a single-chip solution for dynamic bus matching, in addition to fast data access times (t_a = 10 ns). The bus-matching feature offers a flow-through architecture that maintains port-to-port transparency and eliminates the need for any bus-arbitration control logic. Bus matching is performed with the FIFO on the port B bus and can be configured in long-word format (36 bits), word format (18 bits), or byte format (9 bits) for data reads from FIFO1 or written to FIFO2, in the case of the SN74ABT3614 bidirectional FIFO. Port-B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths. The bus-matching feature is implemented using the big-endian ($\overline{BE}$) format and the port-B bus size-select (SIZ0, SIZ1) terminals (see Table 1).

Table 1. Bus Size-Select Terminals

PACKAGE	TERMINAL NUMBER		
	$\overline{BE}$	SIZ1	SIZ0
120-pin TQFP (PCB)	47	50	51
132-pin PQFP (PQ)	132	129	128

The sizing function is performed on the output of port B after a long word has been written into the FIFO on port A (see Figure 3). If an output register is not used (e.g., 9- or 18-bit data reads), no line terminations such as pullup resistors are required due to the bipolar output structures of TI's advanced BiCMOS technology.

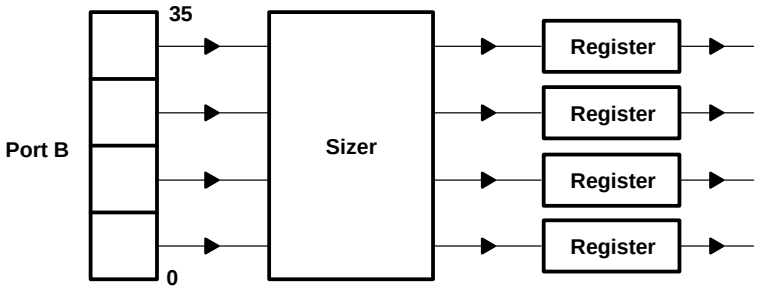


Figure 3. Bus Sizer

By varying the assertion levels of the three control terminals, five different bus-format configurations can be selected (see Table 2).

Table 2. Bus Configurations

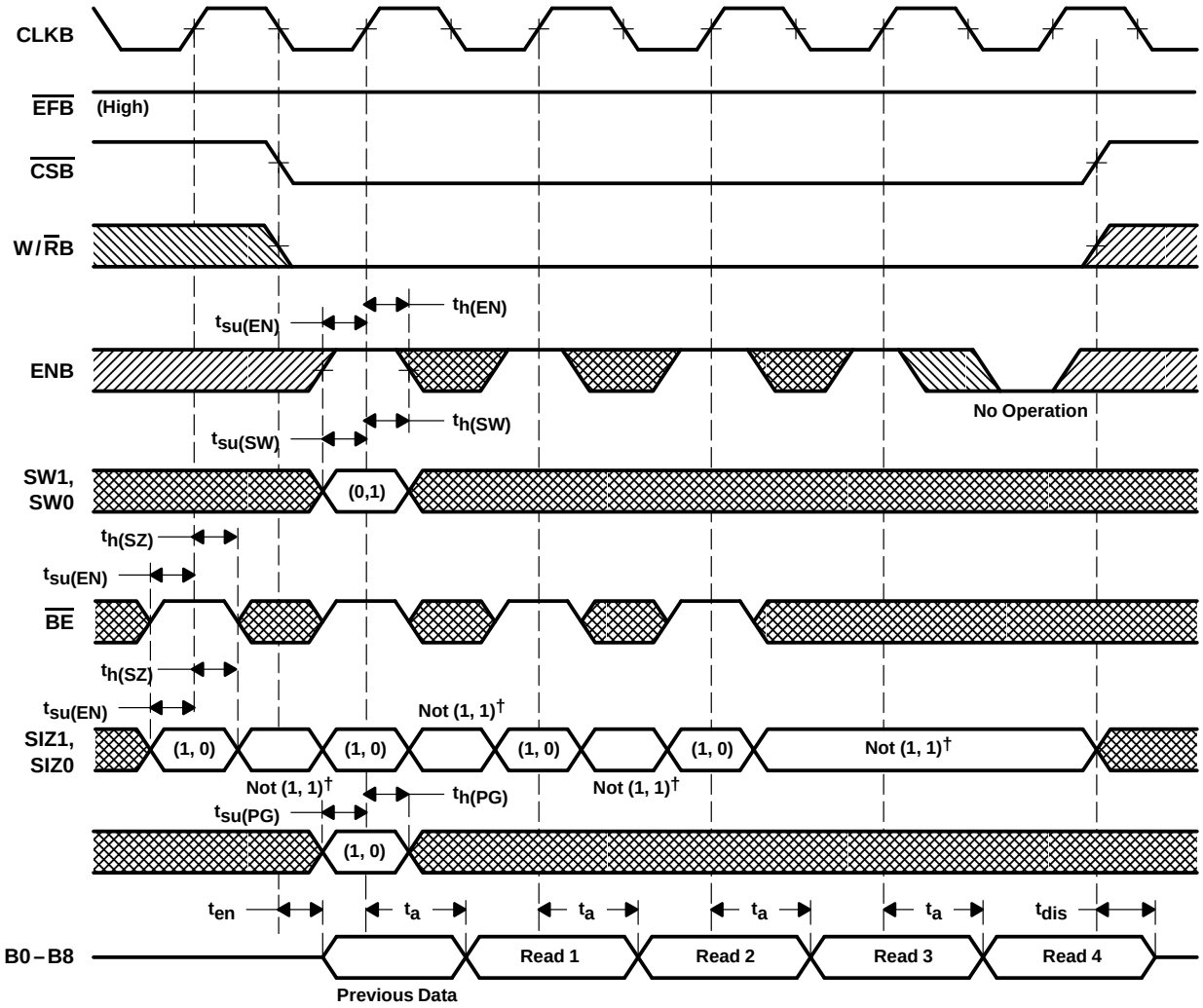
$\overline{BE}$	SIZ0	SIZ1	BUS CONFIGURATION
X	L	L	Long-word size
L	L	H	Word size – big endian
H	L	H	Word size – little endian
L	H	L	Byte size – big endian
H	H	L	Byte size – little endian

The byte-order arrangement of data that is read from or written to the FIFO can be changed synchronous to the clock. The bytes are rearranged within the long word, but the bit order within the bytes remains constant. The byte-swapping feature is implemented by asserting port-B byte-swap select (SW0, SW1) terminals (see Table 3).

Table 3. Byte-Swap Select Terminals

PACKAGE	TERMINAL NUMBER	
	SW1	SW0
120-pin TQFP (PCB)	48	49
132-pin PQFP (PQ)	131	130

The example as shown in Figure 4 takes the conventional 36-bit to 9-bit bus-matching example as shown in Figure 2 one step further by incorporating the byte-swapping feature. A timing diagram of a little-endian, byte-size, byte-swap data read from port B using the SN74ABT3613 unidirectional FIFO is shown in Figure 4. With a 36-bit-long word written into memory from port A, data read can be performed. On the rising edge of CLKB with the port-B chip select ($\overline{CSB}$) asserted low, the size and swap functions can be selected. The little-endian format is chosen by asserting $\overline{BE}$ high. Byte size is selected by asserting SIZ1 high and SIZ0 low. On the second clock cycle, the byte swap is performed by asserting SW1 low and SW0 high for one clock cycle.



† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0 – B35.

Figure 4. Port-B Data-Read Cycle for 36-Bit to 9-Bit Bus Matching

During the second clock cycle, the first byte appears on the output bus B0–B8. After four successive read cycles are completed, the entire long word is parsed out onto the bus in four 9-bit data packets (see Figure 5). In byte-size or word-size data reads, the unused bytes hold the last FIFO output values. After the four bytes are read, the configuration can be dynamically changed.

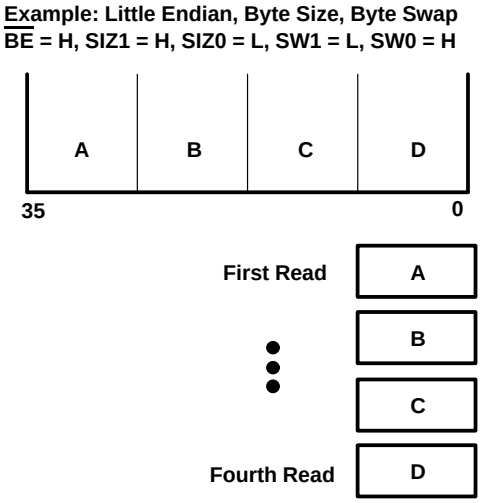


Figure 5. Little-Endian Data-Output Structure

If the example shown in Figure 4 is configured for big-endian format, the data is output on bus B27–B35 (see Figure 6 and Figure 7). No line termination is required for the unused data outputs. This is a dramatic improvement, not only in design ease, but in performance over the conventional data *ping-ponging* technique shown in Figure 2.

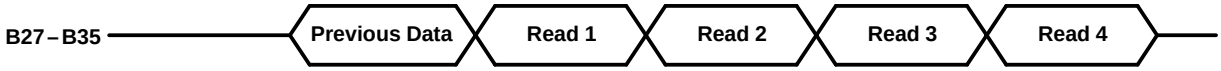


Figure 6. Big-Endian Data Output

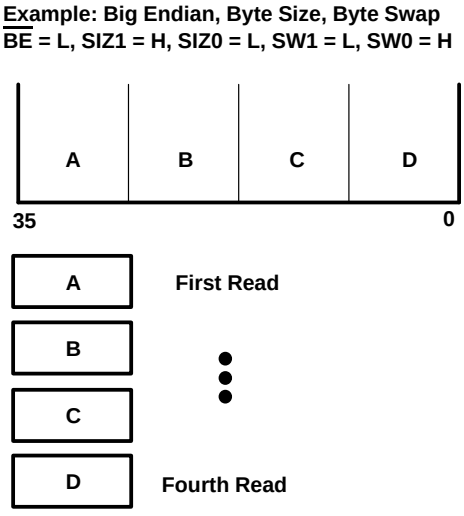


Figure 7. Big-Endian Data-Output Structure

Conventional Bus-Matching Data Writes

Conventional bus-matching data writes experience the same timing restrictions as data reads. The example in Figure 8 shows the circuitry required for 9-bit to 36-bit data writes. Just as in the example in Figure 2, four 9-bit FIFOs are required in addition to an extra control-logic block to synchronize all the write enables.

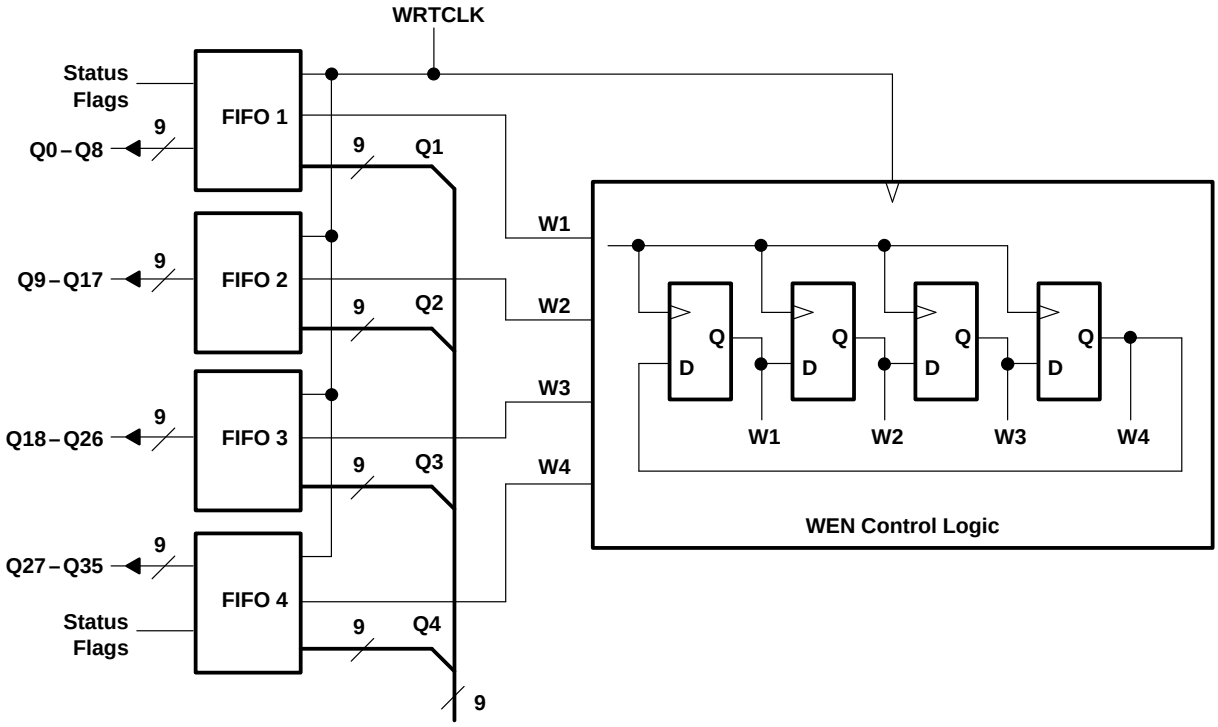
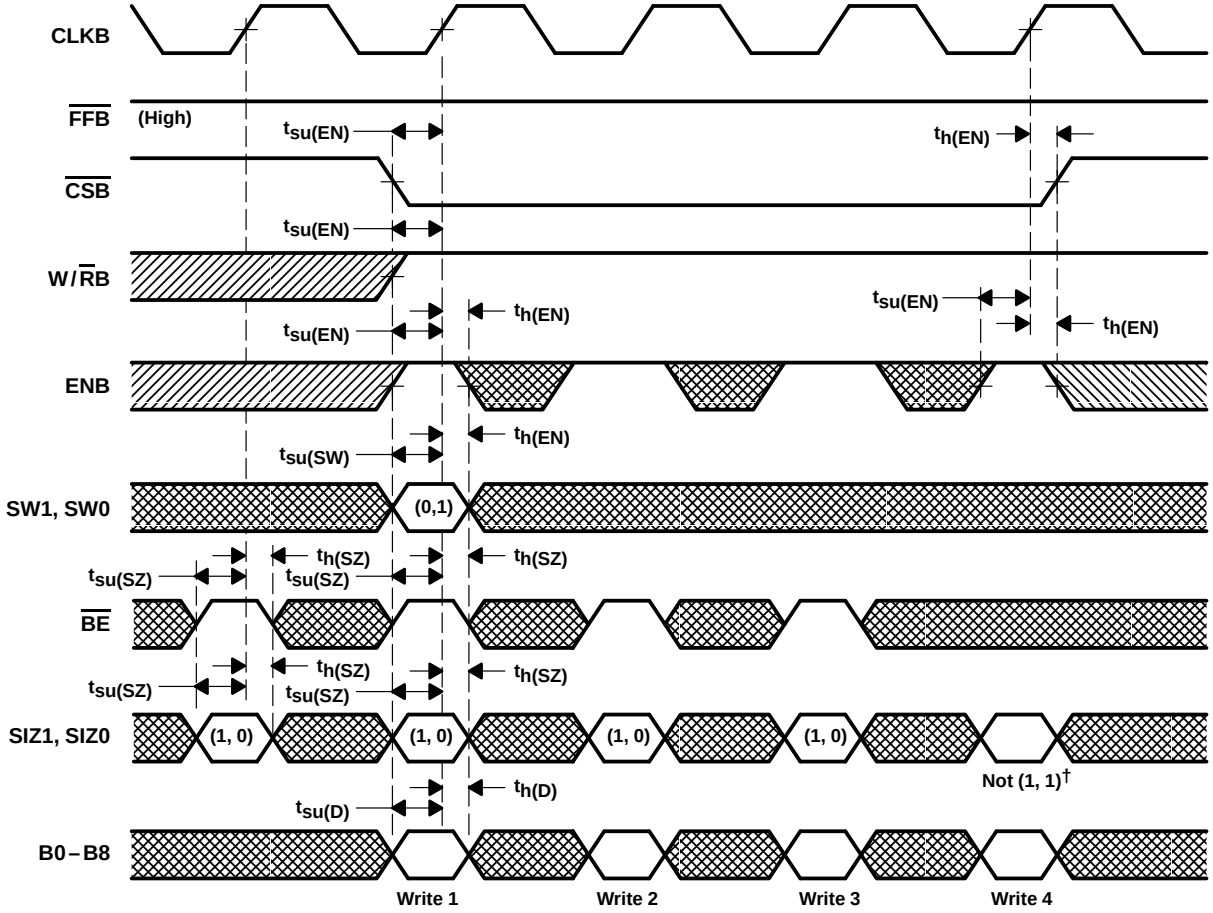


Figure 8. Data-Write Cycle for 9-Bit to 36-Bit Bus Matching

The write-control logic controls each data write in a round-robin style. The control logic consists of a bank of flip-flops that generate the appropriate write-enable signal. After four successful data writes, a long word can be read from the FIFO bank. However, the FIFO bank must have its full- and empty-status flags monitored to ensure data integrity. The empty status is monitored from FIFO4, the last FIFO in the chain. Upon an empty signal, additional data reads are immediately disabled. The full status is monitored from FIFO1, the first FIFO in the chain. When a full status is indicated, further data writes are disabled. To ensure maximum performance, the status flags require fast propagation delays for proper data synchronization. Otherwise, data overwrites can occur, corrupting the FIFO data, or additional wait states must be introduced into the system. Due to the synchronization issues, additional bus control or interrupts become extremely difficult by using the half-full, almost-full or almost-empty flags. This also limits FIFO operations. The data setup and hold times also must be increased to ensure there are no bus contentions during a write operation.

TI's Bus-Matching Data Writes

The timing diagram for performing a little-endian, byte-size, byte-swap data write to port B of FIFO2 using the SN74ABT3614 is shown in Figure 9. By implementing TI's SN74ABT3614 bidirectional FIFO in a design, bus matching can be performed in either direction without the need for additional glue logic or loss of system performance.



† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

Figure 9. Port-B Data-Write Cycle for 9-Bit to 36-Bit Bus Matching

On the rising edge of CLKB with the port B selected ($\overline{CSB}$), the size and swap functions can be selected. The little-endian format is chosen by asserting $\overline{BE}$ high. Byte swap is selected by asserting SIZ0 high and SIZ1 low. These assertion levels are maintained for the entire write cycle. On the second clock cycle, the byte swap is performed by asserting SW1 low and SW0 high for one clock cycle. The data is then written into B0–B8, since the little-endian format has been selected.

If Figure 9 is configured for big-endian format, the data is written into B27–B35 (see Figure 10). No line termination in the form of pullup resistors is required for the unused data inputs.

Figure 10. Big-Endian Format of Byte Write

TI's Byte-Swapping Feature

TI has designed the internetworking FIFOs to provide designers maximum flexibility and ease of use. In addition to the bus-matching feature, a byte-swapping option has been added. The byte-swapping feature allows communication between systems with mixed bus protocols such as those using by RISC and CISC microprocessors. The previous examples of TI's bus matching (Figure 2 through Figure 10) have included the byte-swapping function to demonstrate the true power and flexibility these features provide when implemented together.

Byte swapping is performed on port B of the FIFO (see Figure 11) after the bus-matching function has been executed. Either feature can be implemented separately depending on the system requirements.

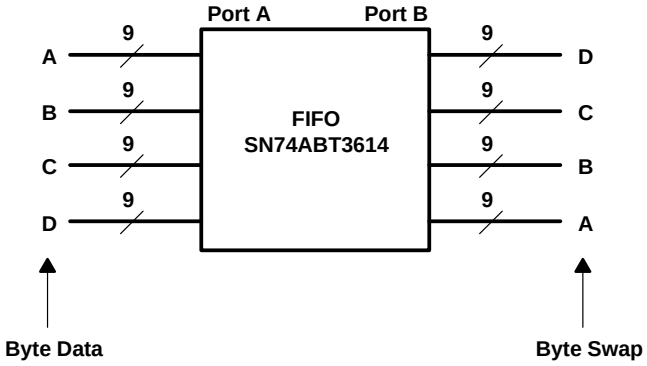


Figure 11. Byte Swapping

As with the bus-matching function, there are several variations of byte swapping, depending upon the assertion levels of the port-B byte-swap select terminals (see Table 4).

Table 4. Byte-Swapping Option

SW0	SW1	BUS CONFIGURATION
L	L	No swap
L	H	Byte swap
H	L	Word swap
H	H	Byte-word swap

Bus matching and byte swapping are performed in the following sequence for all data reads; the 36-bit word is first read, the swap is performed, followed by the bus-size function. The converse is true for data writes.

Conclusion

The ability to dynamically select the desired bus configuration and format is a very useful feature for today's designs. Many systems, such as network switches and routers, implement high-speed backplanes that are typically 32 to 36 bits to ensure maximum bandwidth for data; however, there are many 8-bit and 16-bit controllers and buses in existence. TI's bus-matching feature ensures a flow-through, high-speed architecture that permits multiple logical permutations. There is no longer the need for rerouting bytes on buses and manually controlling bus arbitration through a large and costly discrete solution. The SN74ABT3613 FIFO provides a unidirectional datapath with bus matching and byte swapping on port B. The SN74ABT3614 provides a full bidirectional datapath and supports bus matching and byte swapping in either direction. Both of these FIFOs feature TI advanced-clocked architecture in a space-saving single-chip solution that offers a maximum clock speed of 67 MHz with 10-ns access time.