FIFO Memories: Solution to Reduce FIFO Metastability

First-In, First-Out Technology

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As system operating frequencies continue to increase in excess of 33 MHz, designers must begin to address the issues of overall system reliability due to increased chance of a metastable event occurring. A metastable event is defined as the time period when the output of a logic device is neither at a logic high nor at a logic low but rather in an indeterminate level. The chance of a metastable occurrence is exponentially increased if single-stage synchronization is employed, as in the case of the ′722xx synchronous-style devices versus the two-stage synchronization that is implemented by Texas Instruments (TI) (see Figure 1). The following information assists designers in understanding and improving upon the metastable characteristics of ′722xx synchronous-style devices and their reliability.

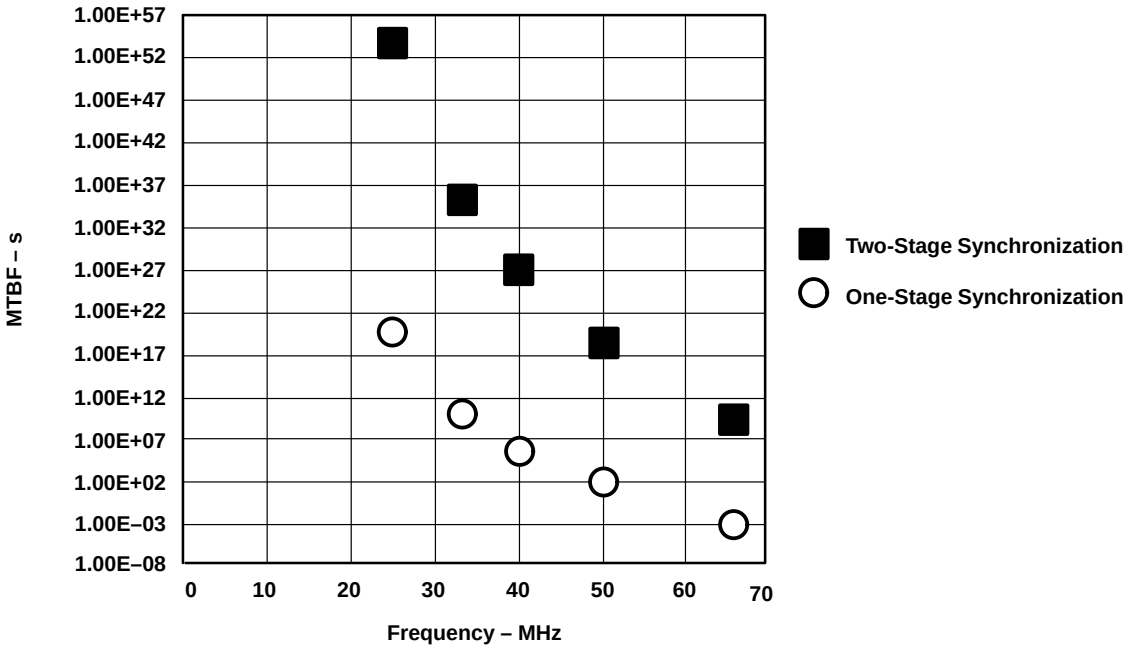


Figure 1. MTBF for Metastability as a Function of Frequency

Metastability may occur when using a FIFO to synchronize two digital signals operating at different frequencies. This type of application is a familiar one to many design engineers. Triggering a metastable event is common in single-stage (single flip-flop) synchronized FIFOs that are used to synchronize different clock signals (see Figure 2). With this method, the asynchronous input might change states too close to the clock transition, violating the flip-flop's setup and hold times. This causes an increase in resolve time (t_r) which then results in an overall increase in propagation delay (t_{pd}). Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with the increased resolve time. The expected time until the output of a single flip-flop with asynchronous data has a metastable event is described by the mean time between failure (MTBF) equation (see equation 1). The first term of the equation is the probability that the asynchronous data will trigger a metastable event. The second term is the data rate. The third and final term is the probability of the metastable event recovering given the resolve time. A linear increase in resolve time exponentially increases the MTBF of a metastable event.

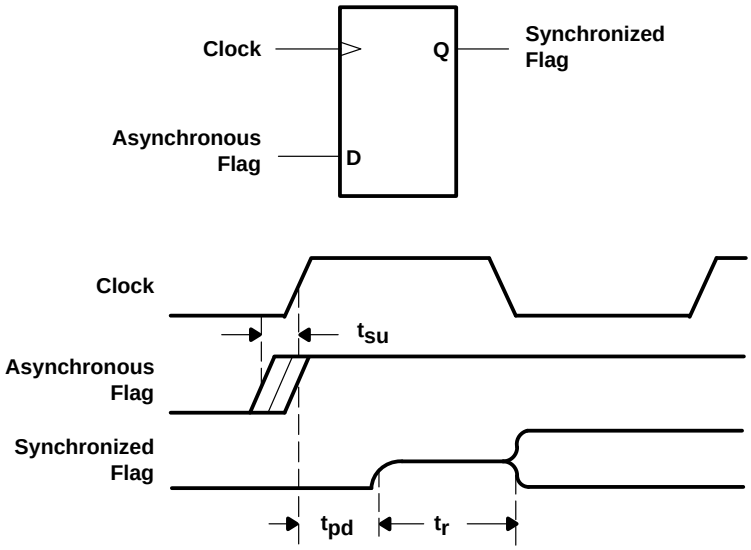


Figure 2. Single-Stage Synchronizer

$$MTBF_1 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times \exp\left(\frac{t_r}{\tau}\right) \quad \textbf{(1)}$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
τ = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency (for OR-flag analysis, it is the frequency at which data is written to empty memory; for IR-flag analysis, it is the frequency at which data is read from full memory).

TI has increased the metastable MTBF by several orders of magnitude over single-stage synchronization with its advanced FIFO family by employing two-stage synchronization (see Figure 3). The output of the first flip-flop is clocked into the second flip-flop on the next clock cycle. For the output of the second stage to become metastable, the first stage must have a metastable event that lasts long enough to encroach upon the setup time of the second stage. The addition of the second flip-flop to the single-stage synchronizer allows the flip-flops more time to resolve any metastable output. This is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. MTBF for a two-stage synchronizer is given in equation 2. All terms, except for the third one, are the same as in equation 1. The third term represents the additional propagation delay through the added flip-flop.

$$MTBF_2 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times \exp\left[\frac{\frac{1}{f_c} - t_{pd}}{\tau}\right] \times \exp\left(\frac{t_r}{\tau}\right) \quad \textbf{(2)}$$

t_{pd} = propagation delay through the first flip-flop
$MTBF_2$ = $MTBF_1$

Where:

t_r = $t_r + (1/f_c - t_{pd})$

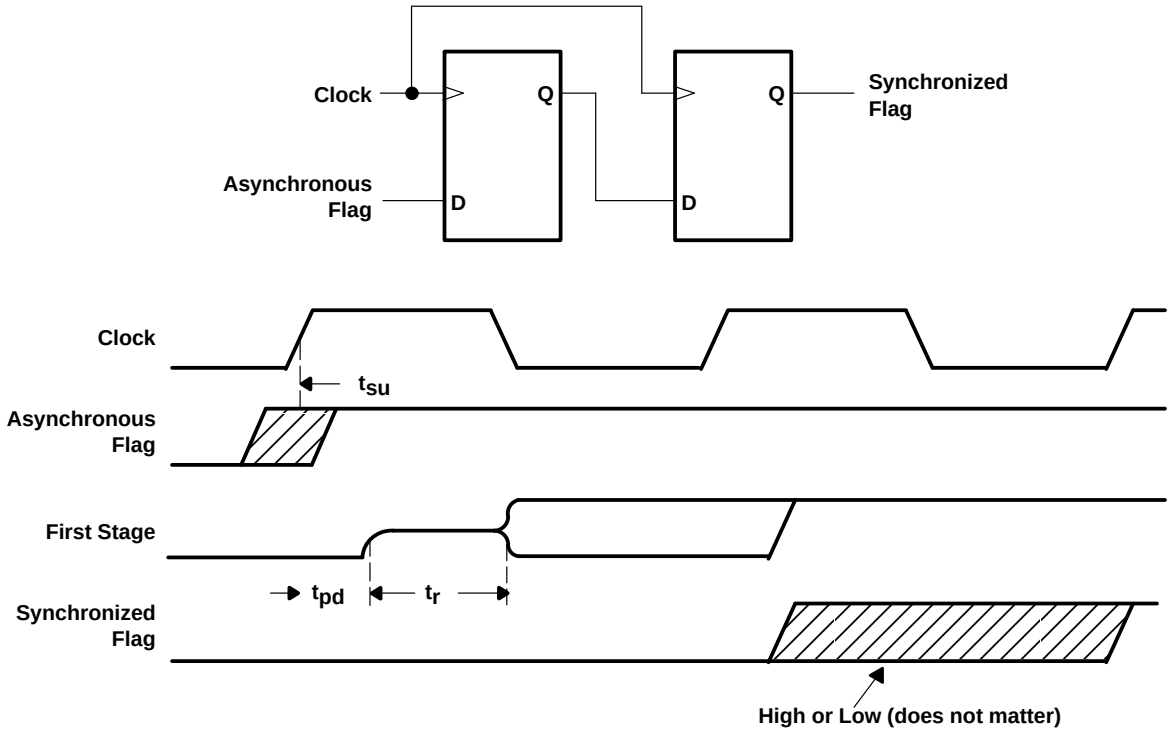


Figure 3. Two-Stage Synchronizer

The functional block diagram in Figure 4 illustrates the connections necessary to add the second-stage synchronization to the ′72211 synchronous FIFO. A quick and inexpensive schematic to resolve metastability of a synchronous FIFO is shown in Figure 5. In this case, the FIFO is the ′72211LJ and, by implementing a single TI SN74F74 D-type positive-edge-triggered flip-flop and a TI SN74F08 two-input positive AND gate, the metastability characteristics of this circuit can be dramatically improved. The TI SN74F74 acts as the second stage for this circuit, increasing the resolve time as described in the previous paragraphs. The TI SN74F08 is implemented to act as the control-empty and control-full flags to the receiving device. These control lines of the first-stage and second-stage synchronized flags are then ANDed together to create the control flags (control empty and control full). The control lines are essentially read enables that ensure the synchronization of the device. As is shown in the logic diagram and truth table, synchronization is complete only when the empty flags ($\overline{EF}$) of both the second stage (truth table input A) and the device (truth table input B) are high. The empty flag is used for read control and the full flag ($\overline{FF}$) is used for write control. If either flag from the synchronizer or the device is held low or becomes metastable, a read is not permitted (truth table output Y) until the write flag is synchronized.

As can be seen in today's digital systems, synchronous and asynchronous operations can and will produce random errors due to metastability in single-stage FIFO designs like those of the ′722xx synchronous FIFO family. The described method of implementing a second stage for flag synchronization is extremely useful for clock speeds that are either approaching or exceeding 33 MHz. Metastability can be virtually eliminated in the ′722xx synchronous FIFO family by the simple addition of a second flip-flop. The second-stage synchronizer greatly reduces metastability, thereby increasing the MTBF and allowing designers to use faster microprocessors and higher data-transfer rates for greater overall system performance and reliability.

To reduce metastability and improve system reliability, TI offers a complete line of high-performance FIFO memory devices. TI's FIFOs have dual-stage synchronization designed onto each chip. This eliminates the need for any external discrete solution and reduces critical board space by fully utilizing TI's family of fine-pitch surface-mount packaging.

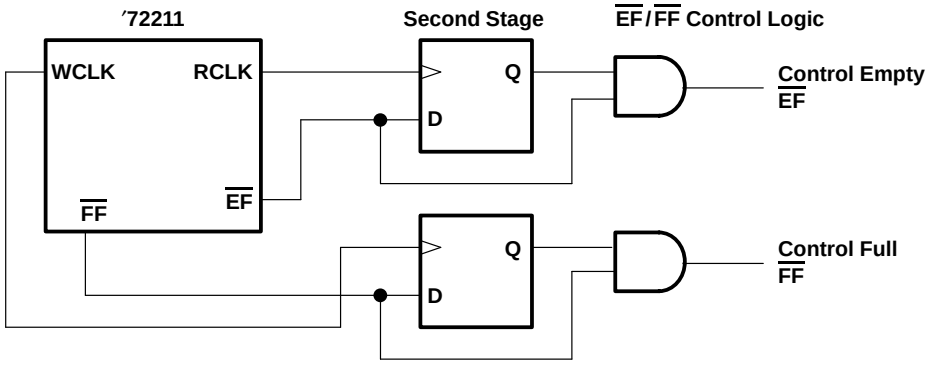
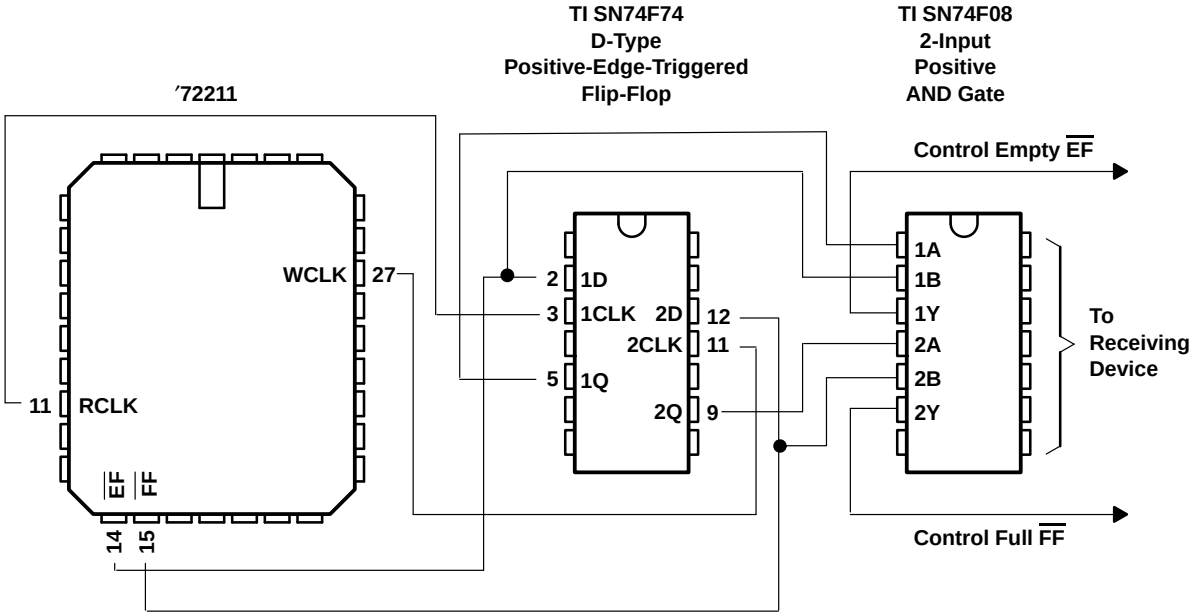


Figure 4. Connecting the Second-Stage Synchronizer to the ′72211 Synchronous FIFO



INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Figure 5. Resolving Metastability of a Synchronous FIFO