1K × 9 × 2 Asynchronous FIFOs SN74ACT2235 and SN74ACT2236

First-In, First-Out Technology

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TEXAS INSTRUMENTS

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Introduction

Texas Instruments (TI) designed the SN74ACT2235 to meet a variety of synchronous or asynchronous bidirectional applications. Two 1K x 9 first-in, first-out (FIFO) memories are arranged in parallel to buffer data in opposite directions. Data ports also may exchange real-time data. Three-state control (GAB, GBA) and real-time/stored data select (SAB, SBA) match the popular ′652 transceiver logic. Produced in TI's EPIC™ CMOS process, the inputs accept TTL-voltage levels. An option to the SN74ACT2235 is the SN74ACT2236, which has ′646 transceiver control (DIR, $\overline{G}$). The functional block diagram for the SN74ACT2235 is shown in Figure 1.

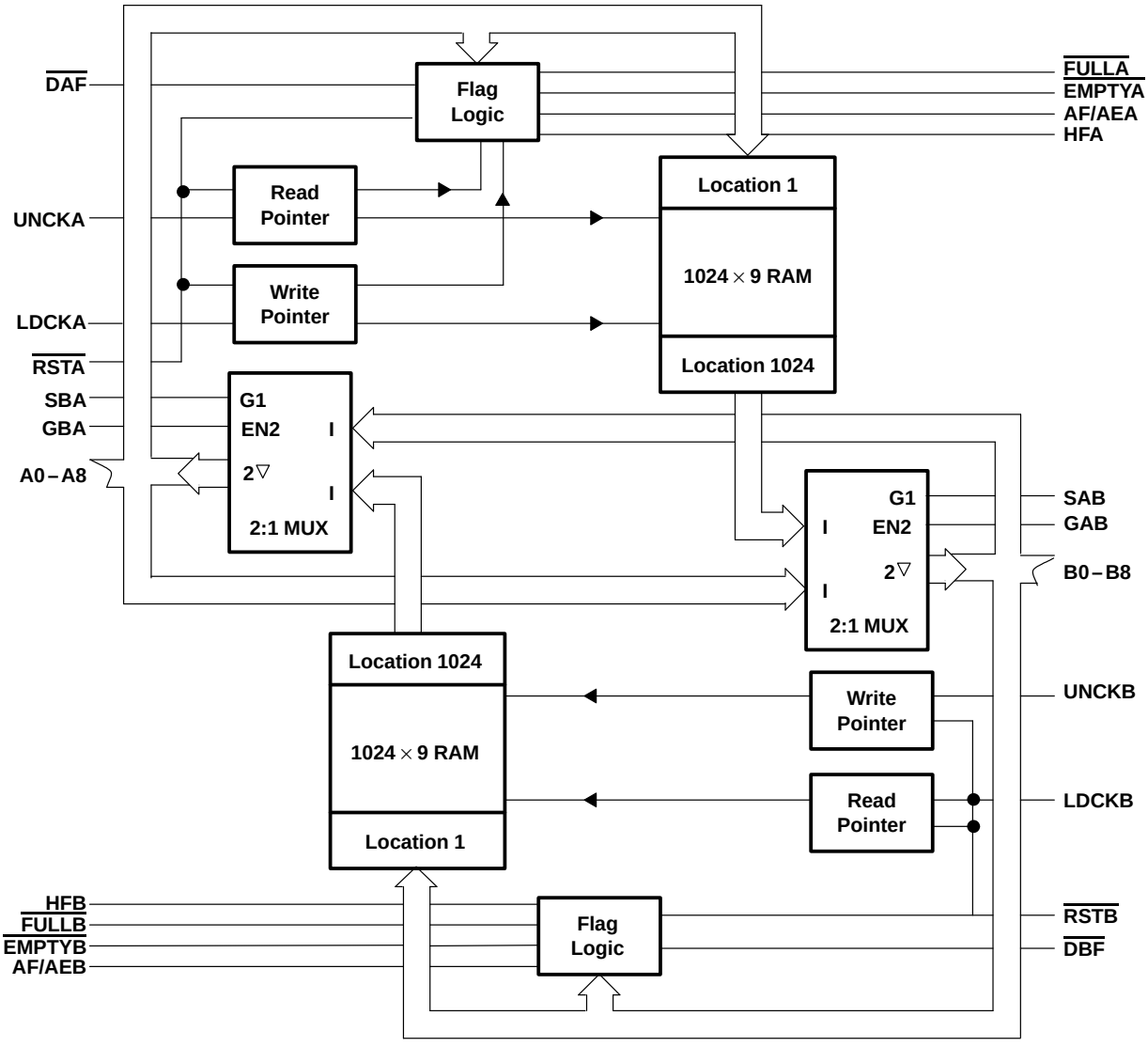

Figure 1. SN74ACT2235 Block Diagram

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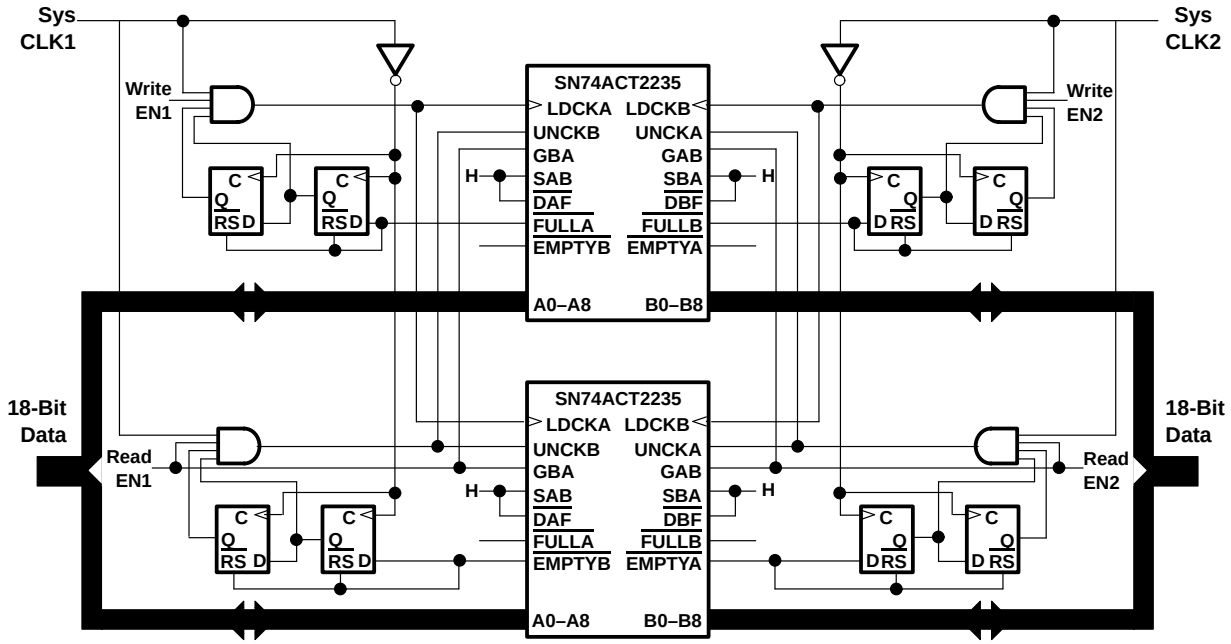
FIFO Control

The SN74ACT2235 consists of two FIFO memories, FIFOA and FIFOB. Both FIFOs can be accessed from either port A or port B. Four control signal lines (GAB, GBA, SAB, and SBA) control the eight possible data flow paths through the device (these datapaths are illustrated in the device data sheet). Each FIFO has a load clock (LDCK) that writes data into memory and an unload clock (UNCK) that reads the data in the same order it was written. Both clocks are positive-edge-triggered and may operate asynchronously to one another. The first word loaded into an empty FIFO propagates directly to the outputs and the $\overline{\text{EMPTY}}$ flag switches high. $\overline{\text{EMPTY}}$ represents the valid state of data on the outputs (data is valid when $\overline{\text{EMPTY}}$ is high and invalid when $\overline{\text{EMPTY}}$ is low). $\overline{\text{EMPTY}}$ may be used to enable an UNCK pulse when it is synchronized with the bus that reads the data. $\overline{\text{FULL}}$ can qualify a LDCK pulse in the same way.

Figure 2 is an example of an SN74ACT2235 interfacing two asynchronous systems. Each system provides a read enable, write enable, and free-running clock. Synchronization of a flag to the system clock is needed to use it as device-clock control. Although the flag's high-to-low transition is synchronous to the clock it enables, the low-to-high transition is asynchronous. The output of the latch qualifying this transition has the possibility of going metastable when bistable (setup and hold) conditions are not met. An output is metastable if it lingers between the specified V_{OH} and V_{OL} levels. Two-stage synchronization of the flags reduces the probability of a metastable-induced failure.



NOTE: Two devices are used for 18-bit width expansion.

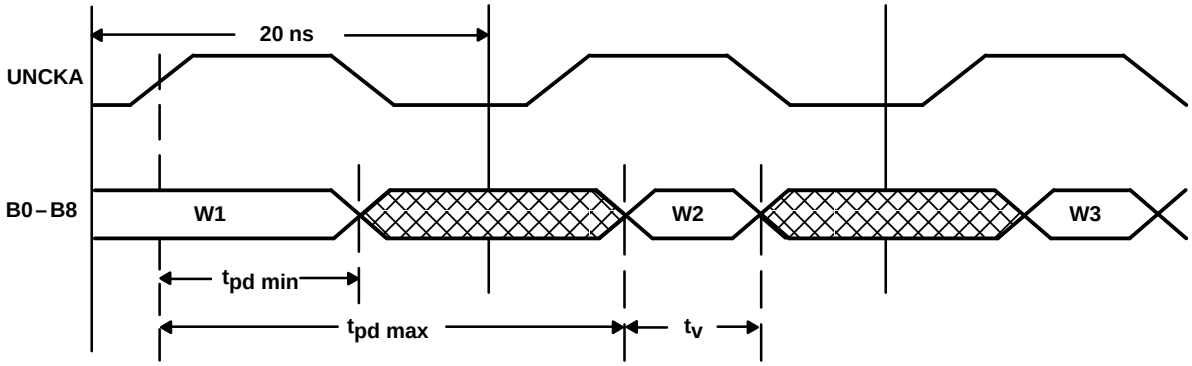
Figure 2. Controlling the SN74ACT2235 Using a Clock, Write Enable, and Read Enable per System

High-Frequency Applications

A unique feature of the SN74ACT2235 is that the UNCK cycle time may be less than the device access time. The SN74ACT2235-20 has a maximum LDCK and UNCK frequency of 50 MHz (20-ns cycle time) and a 25-ns maximum access time (t_{pd} UNCKA or UNCKB to B bus or A bus). In a series of FIFO reads, the next access may be initiated before the present one is complete. The largest concern associated with this technique is the length of time data is assured as valid. Minimum access time from the rising edge of UNCK also may be viewed as minimum data hold time. Timing for this relationship is shown in Figure 3. Valid data time from the SN74ACT2235 over the commercial temperature range and ±10% V_{CC} is given by equation 1:

$$t_v = t_c + t_{pd}\text{min} - t_{pd}\text{max} \quad \textbf{(1)}$$

Data from an SN74ACT2235 operating at a 50-MHz clock frequency is valid for at least 7 ns. This allows a 4-ns setup and 1-ns hold time with a 2-ns tolerance to the next device in the datapath.



For SN74ACT2235-20: $t_{pd\ min}$ = 12 ns, $t_{pd\ max}$ = 25 ns, t_v = 7 ns

Figure 3. Read Operation When Cycle Time Is Less Than Access Time

Programmable Flags

Data is often transmitted in packets, where each packet is a specific number of bytes and must be delivered in an unbroken stream. A FIFO transmitting packeted data needs a flag that shows the number of bytes stored. This keeps from breaking the transmission of a packet due to an empty or full condition. The SN74ACT2235 has a programmable almost-full/almost-empty (AF/AE) flag for this application. The AF/AEA offset value (X) and the AF/AEB offset value (Y) are programmed separately. AF/AEA is high when FIFOA contains X or fewer words or (1024 – X) or more words. It is low when FIFOA contains between (X + 1) and (1023 – X) words. AF/AEB functions in the same manner with its programmed value Y. The programmed or default value of 256 is chosen during a reset of each FIFO.

Flag-programming logic is illustrated in Figure 4. Programming the AF/AE flag value for each FIFO is done with the define-flag ($\overline{DAF}$, $\overline{DBF}$) inputs and resets ($\overline{RSTA}$, $\overline{RSTB}$). Define-flag inputs are negative-edge-triggered clocks that store input data to a register. If $\overline{DAF}$ or $\overline{DBF}$ is low when the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$ occurs, the registered value is used for the FIFO AF/AE flag. The flag uses the default value of 256 if $\overline{DAF}$ or $\overline{DBF}$ is high during the rising edge of $\overline{RSTA}$ or $\overline{RSTB}$.

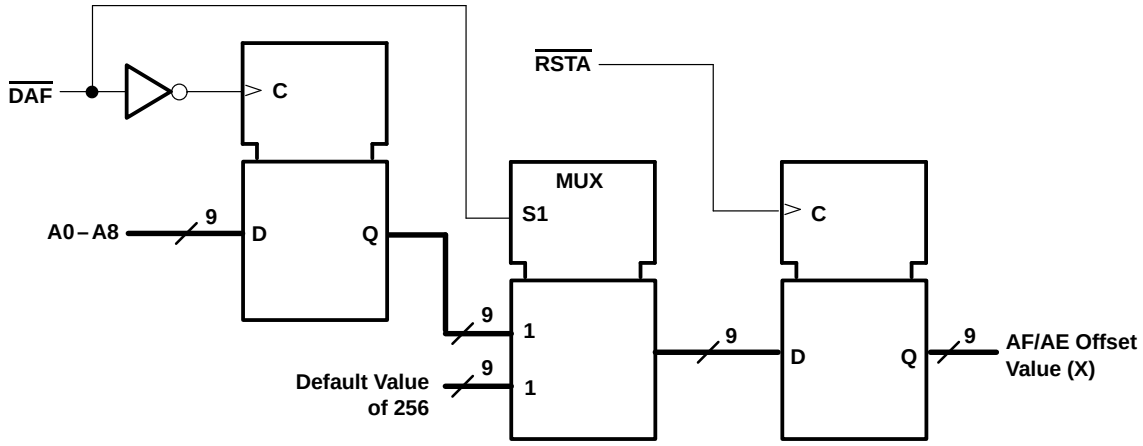


Figure 4. AF/AEA Flag-Programming Logic for FIFOA

Programming both flag offset values from either port is possible using real-time select. Figure 5 is a timing example of programming AF/AEB from port A. To program the AF/AEB offset value (Y) from port A, the binary value for Y is on A0–A8, SAB is low, and GAB is high. With this configuration, the port-A data appears on the inputs of FIFOB and a falling edge of $\overline{DBF}$ stores the Y value.

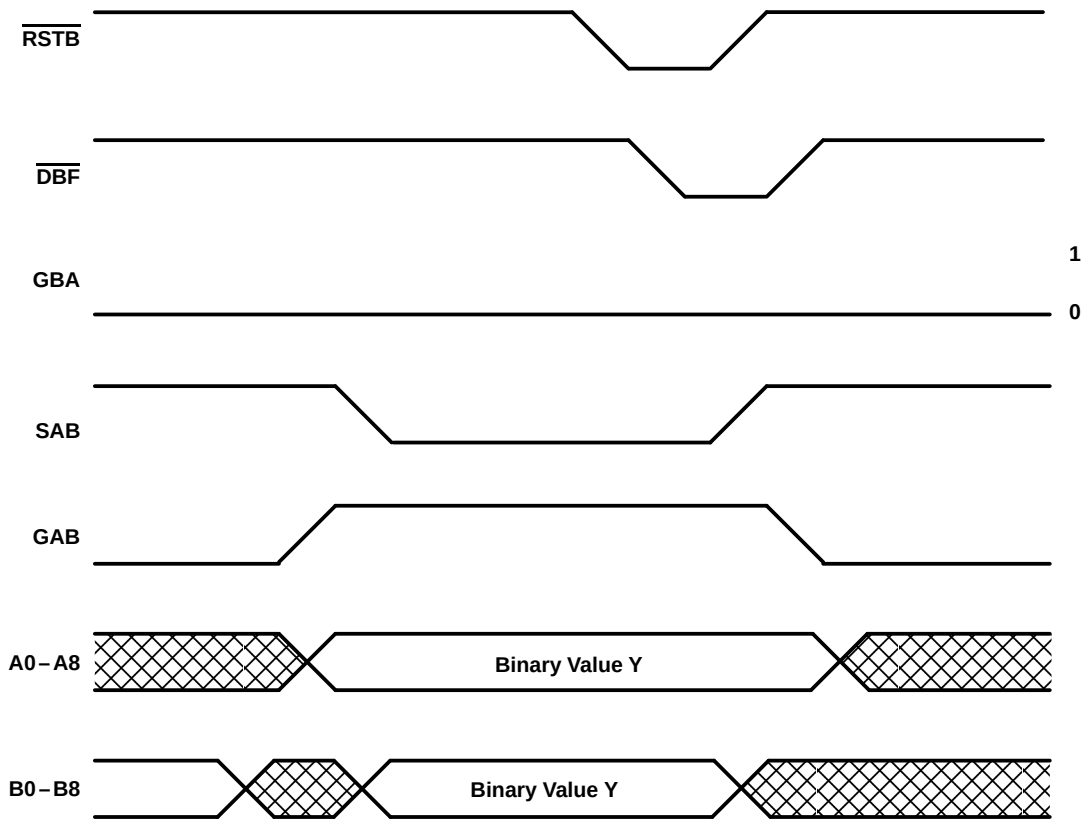


Figure 5. Programming AF/AEB Flag of FIFOB From Port A

Output Drive

Charging and discharging the load of a bus with acceptable speed requires high device-output drive. The I/O ports of the SN74ACT2235 provide 16-mA I_{OL} and 8-mA I_{OH} for this task.

Most memory devices have low drive capability and require buffers to interface a bus. They do not use larger transistors that support high current because the rate of change of current with respect to time (di/dt) increases. When several transistors switch simultaneously, the rate of change of current through ground and V_{CC} lines multiplies. Voltage transients on the power lines are given by equation 2:

$$V = -L(di/dt) \quad (2)$$

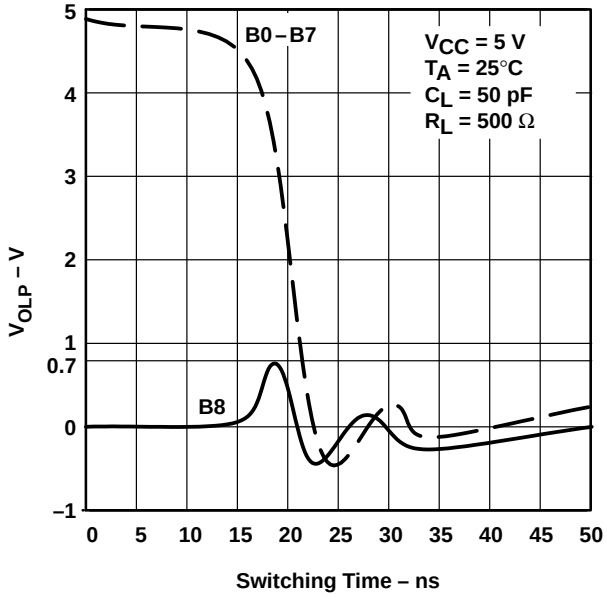
Where:

L = inductance of the bond wire and package lead

The SN74ACT2235 provides a two-fold solution to allow high-output current capability with low noise. One solution is to reduce inductance of ground and V_{CC} lines. The SN74ACT2235 has four GND and two V_{CC} pins in parallel. The resulting ground inductance is about 1/4 that of a single connection and divides V_{CC} inductance in half.

Reducing di/dt per output transistor is another way to minimize voltage transients. TI's patented output-edge-control (OEC™) design divides a large transistor into smaller segments that turn on in series and turn off simultaneously. OEC™ lowers di/dt, maintains a quick voltage transition through threshold, and avoids the high power consumed when gradually turned off .[1]

The result of a V_{OLP} test on the SN74ACT2235 is shown in Figure 6. V_{OLP} is a measurement of ground-voltage noise when all outputs of a bus are switched from high to low. Eight of nine outputs of a bus are switched, and the peak-voltage rise of the steady-state low output is measured. Maximum ground-voltage rise is only 700 mV. The output fall time is less than 3 ns with a 50-pF load.



NOTE: Eight bus outputs switching, one remains low

Figure 6. SN74ACT2235 V_{OLP} Measurement

Conclusion

The SN74ACT2235 and SN74ACT2236 provide several advantages for high-speed asynchronous bus interface. Simple control logic offers great design flexibility. Programmable flags may be used for data flow optimization. High-output drive for bus leading is balanced with noise reduction through package and circuit design.

[1] Advanced CMOS Logic Designer's Handbook, pages 3–1 through 3–12.