

Simultaneous-Switching Noise Analysis for Texas Instruments FIFO Products

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Abstract

Analysis of circuit-noise immunity during simultaneous switching of multiple outputs is crucial in the high-speed advanced logic families including ACT and ABT FIFO products. Consequently, reduction of simultaneous-switching noise is of the utmost concern to the FIFO design team at Texas Instruments (TI). TI offers reliable FIFO products that meet the fast-speed requirement of today's technology. In this application report, a thorough explanation of noise-reduction techniques for TI's FIFO devices is provided. This report assists component and system design engineers in their evaluations of simultaneous-switching noise for TI's ACT and ABT FIFO products.

Introduction

One concern in advanced integrated circuit (IC) design is the challenge of minimizing simultaneous-switching noise while increasing switching speed of the device. This application report presents the achievements TI has made in providing very high-speed FIFO products with minimum simultaneous-switching noise.

This report provides an introduction to advanced CMOS simultaneous-switching noise and the approaches taken by the FIFO design group to effectively reduce the noise. Test procedures for measuring noise during simultaneous switching of multiple outputs are also presented. Test results provide the data necessary to ensure proper operation of the FIFO during simultaneous switching of multiple outputs.

In high-speed, high-density CMOS VLSI devices, many output drivers may switch simultaneously. During the transition, the excessive current drawn from the power supply can produce a significant amount of power/ground noise called simultaneous-switching noise (SS noise). The noise may be generated in the package V_{DD}/V_{SS} planes and also in the internal (on-chip) V_{DD}/V_{SS} buses. Figure 1 shows the power/ground noise coupling through a dc-on driver to external circuitry.

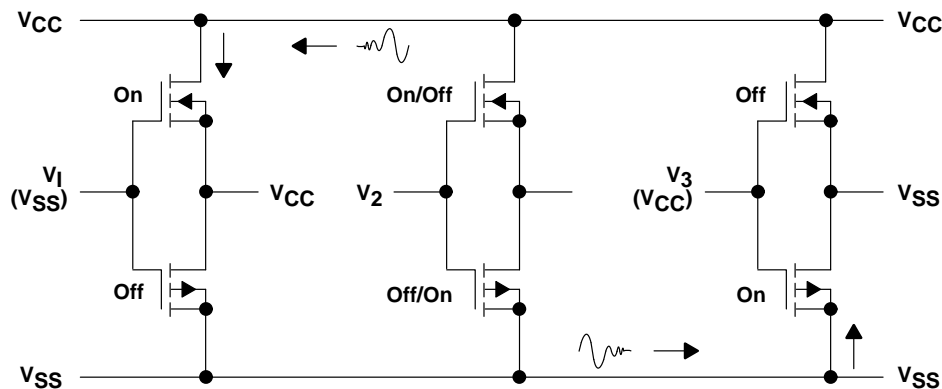


Figure 1. Power/Ground Noise Coupling Through a dc-on Driver to External Circuitry¹

A simultaneous-switching scenario where several drivers switch at the same time is shown in Figure 2. The electrical path from the ground/power IC pads to the package terminals is inductive as shown in Figure 2. The IC pads are connected through bonding wires to the package pads that are connected through a multilayer package to the package terminals, which, in turn, are connected to ground/power planes on the printed circuit board (PCB). All of these different elements in the packaging of the IC behave as inductances with negligible resistive components.²

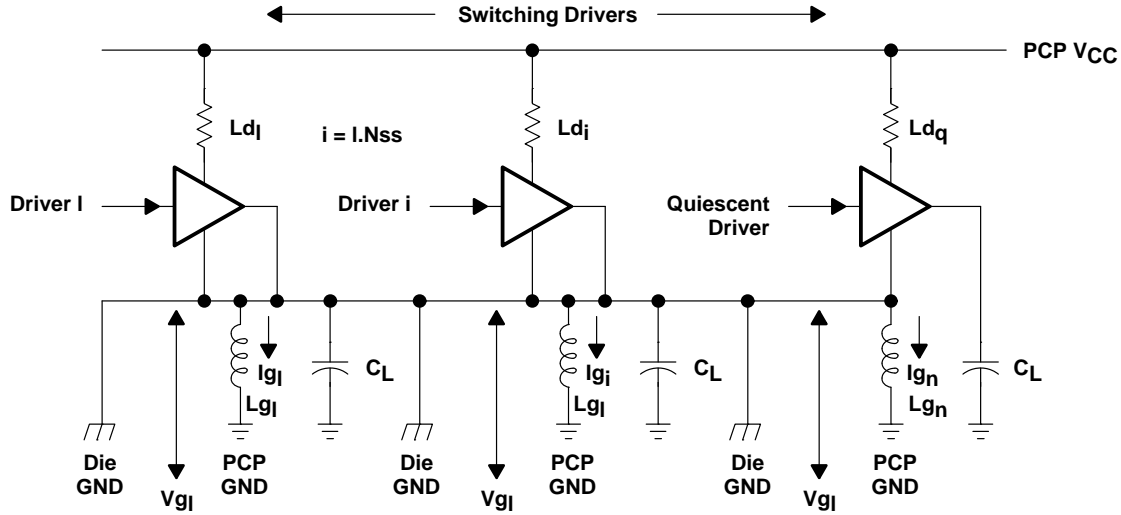


Figure 2. Simultaneous Switching²

The physics of the device package plays a fundamental role in the voltage-noise spike. The major effect on a high-speed device is the induced voltage on the GND and V_{CC} terminals caused by the transient currents from switching capacitive loads.³ If only one output is switched, the ground noise is calculated by equation 1 where L_g is the inductance of the ground terminal due to the bond wire, lead, and via, and di/dt is the time rate of change in transient current driving the capacitive load. Equation 2 illustrates transient current where dV_o/dt is the change of output voltage in time.

$$V_{GND} = -L_g \times di/dt \quad (1)$$

$$i(t) = C_L \times dV_o/dt \quad (2)$$

The induced ground bounce appears on the quiescent output as shown in Figure 3.

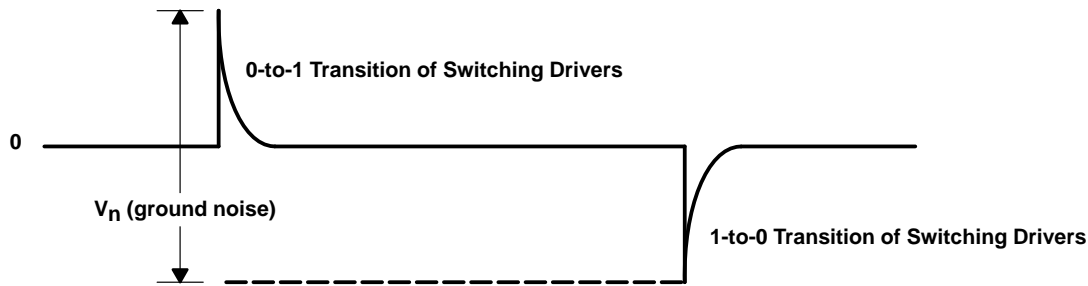


Figure 3. Example of Ground-Bounce Waveform²

When the number of simultaneously switching outputs increases, ground noise increases. For large ICs, the relationship between ground-bounce amplitude and the number of switching drivers is no longer linear.^{1, 2, 4}

Unless these power/ground noise fluctuations are controlled, simultaneous-switching noise can degrade or even limit system performance. Uncontrolled noise spikes can lead to loss of stored data, severe speed degradation, output glitches, and reduction in system-noise immunity.³ From a functional perspective, ground bounce reduces noise margins of the gate and may cause false switching of quiet gates. Noise margins for the low state are usually smaller than noise margins for the high state; therefore, noise of the ground bus in the IC concerns designers the most.^{2, 5}

Several techniques have been proposed for reducing simultaneous-switching noise. At the package level, one approach is to reduce the inductance by improved packaging techniques, such as decreasing the various inductive contributions to ground bounce.² Surface-mount packages, such as PQFPs, are a better package option than through-hole packages, such as DIP or PGA, because the former have shortened pins or a lower-profile package. Another approach is to decrease the inductance of the ground pins by placing as many ground/power pins in the package as possible.^{1, 2} At the design level, some designers have proposed output edge control (OEC™) as a solution to reduce noise.⁴

At the circuit level, simultaneous-switching noise can be reduced by skewing the output drivers and/or by damping out power and ground noise with additional damping resistors at the source end of both p- and n-channel transistors of output drivers,³ and/or by adding bypass capacitors that reduce the current noise associated with output buffers driving off-chip loads.⁴ This application report concentrates only on TI's approaches to reduce the simultaneous-switching noise in high-performance advanced FIFO products.

TI Solution for Simultaneous-Switching Noise

TI's solutions to minimize noise caused by simultaneous switching of outputs include reducing package inductance by using multiple ground pins, controlling the output edge, and separating the ground pins. Measurements used by TI in evaluating the chip's performance are included in the following discussion.

Reducing Package Inductance

To reduce voltage spikes, the value of lead inductance (L_g) in equation 1 should be lowered. Lead inductance is dependent upon lead lengths as well as the location of GND/ V_{CC} pins in the package. Decreasing the overall size of the FIFO package lowers the package inductance. The inductance value per pin for most of the package types used for FIFO products is shown in Table 1. TI's current technology has provided high-performance 9-, 18-, and 36-bit FIFO products with less inductance per pin, giving TI a performance edge in the FIFO market. More information on TI package types is provided in Appendix B.

Table 1. Inductance Value per Pin for Most Package Types Used for FIFO Products

PITCH	PACKAGE TYPE	FIFO TYPE	INDUCTANCE PER PIN (nH)
Standard-Pitch Option	24-pin DIP	4-, 5-, 8-, and 9-bit FIFO	3–15
	28-pin DIP	9-bit (IDT) FIFO	2–15
	44-pin PLCC	9-bit FIFO	6–8
	28-pin SOIC	1-bit FIFO	3–8
Fine-Pitch Option	120-pin TQFP	36-bit FIFO	4–5
	80-pin TQFP	18-bit FIFO	5
	64-pin TQFP	9-bit FIFO	3–4

Multiple GND and V_{CC} Pins

By adding more GND and V_{CC} pins on a chip, TI offers advanced FIFO products with lower noise compared to other products with only one GND and one V_{CC} corner pin. The previous section discussed simultaneous-switching noise being directly proportional to the inductance of the ground/power leads. Multiple ground/power pins improve the noise immunity of the chip by reducing the total ground/power lead inductance because the total inductance is a parallel combination of the lead inductances of the ground/power pins. For example, SN74ACT7814 FIFO memory in Figure 4 has four GND pins distributed among the outputs. The total ground-lead inductance of this chip is approximately one-fourth of that of a similar chip with only one GND pin. Assuming L_1 , L_2 , L_3 , and L_4 are the lead inductances of the four ground pins on the chip, and assuming these inductances are equal, the combination of the parallel inductances is 1/4 of the inductance when only one GND pin is on the chip (see equation 3).

$$L_T = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4}} = \frac{L_1}{4} \quad (3)$$

OEC is a trademark of Texas Instruments Incorporated.

Multiple ground/power pins are used on all TI FIFO products. Table 2 shows the number of data output pins per ground pin for different FIFO products.

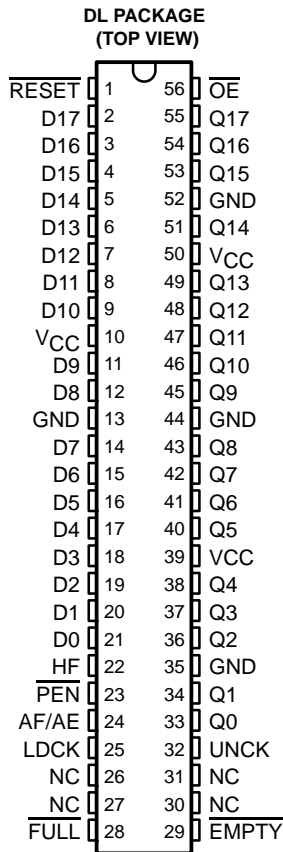


Figure 4. SN74ACT7814 FIFO With Multiple GND Pins

Table 2. Number of Data Output Pins per Ground Pin for Different FIFO Products

FIFO	FIFO PRODUCT	SIZE	PACKAGE TYPE	GND PINS	DATA OUTPUTS PER GND PIN
9 Bits	SN74ACT2335	102492	44-pin PLCC (FN)	4	4.5
			64-pin TQFP (PM)	12	1.5
	SN74ACT2236	102492	44-pin PLCC (FN)	4	4.5
			64-pin TQFP (PM)	12	0.75
18 Bits	SN74ACT7803	51218	(DL)	4	4.5
			68-pin PLCC (FN)	10	1.8
	SN74ACT7811	102418	80-pin TQFP (PN)	14	1.3
			80-pin QFP (PH)	14	2.6
32 Bits	SN74ABT7819	512182	80-pin TQFP (PN)	14	2.6
			120-pinTQFP (PCB)	14	4.6
			132-pin PQFP (PQ)	15	4.3

36 Bits	SN74ABT3614	64362	120-pin TQFP (PCB)	10	7.2
			132-pin PQFP (PQ)	18	4.0
	SN74ACT3632	512362	120-pin TQFP (PCB)	14	5.1
			132-pin PQFP (PQ)	14	5.1
	SN74ACT3641	102436	120-pin TQFP (PQ)	15	2.4
			132-pin PQFP (PCB)	15	2.4

Output Edge Control (OEC™) Method

OEC™ is another method for controlling simultaneous-switching noise. This is a circuit method that reduces the di/dt portion of equation 1. The output transistor is split into many small subtransistors with sequential turnon of each subtransistor. By splitting the total current into a series of smaller currents distributed over time, the effective di/dt is reduced. The delay in turnon of the successive subtransistors reduces the maximum peak di/dt for the entire output transistor.

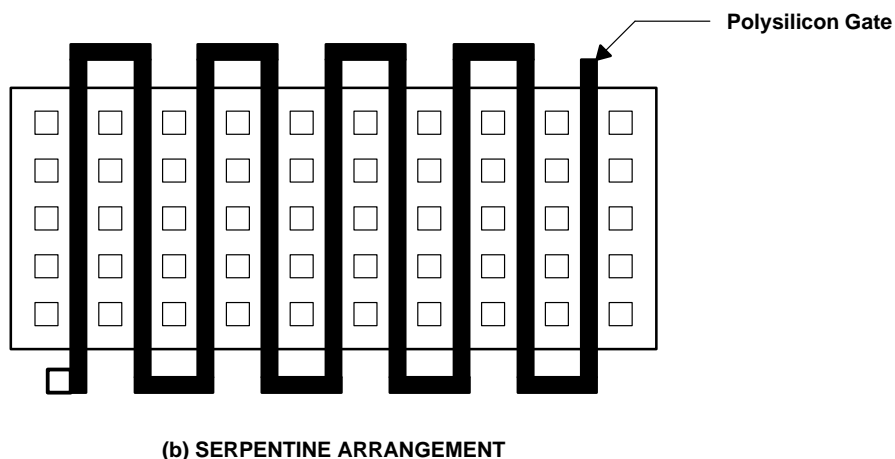
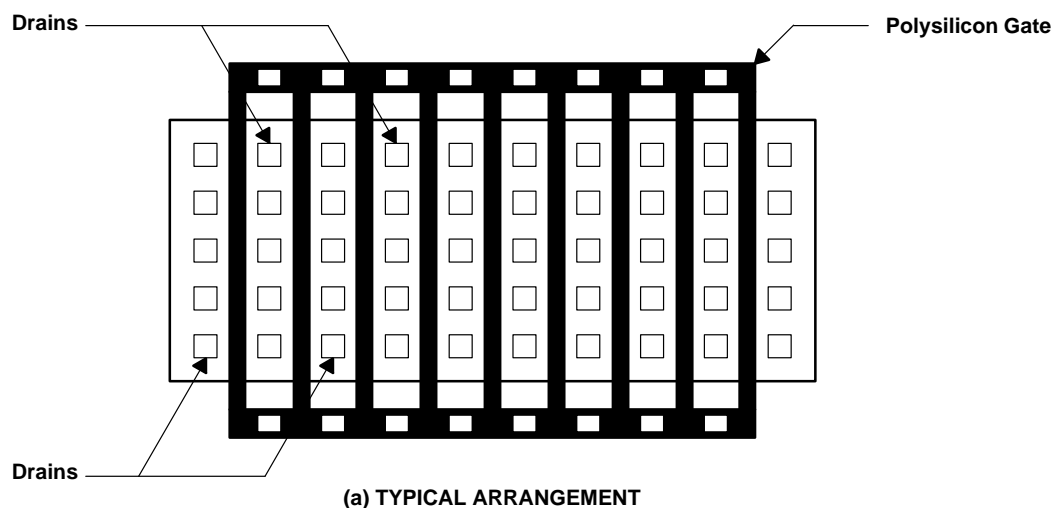


Figure 5. CMOS-Transistor-Gate Layout

At the output, the structure of the polysilicon gate is modified to grade the turnon by removing portions of the polysilicon gate to form a serpentine arrangement and by driving the gate from one end (see Figure 5). The resistance of the polysilicon and the capacitance of each gate segment form a distributed RC network that slows the turnon of each succeeding segment. Figure 6 shows the equivalent-circuit schematic for the distributed output transistor.⁴

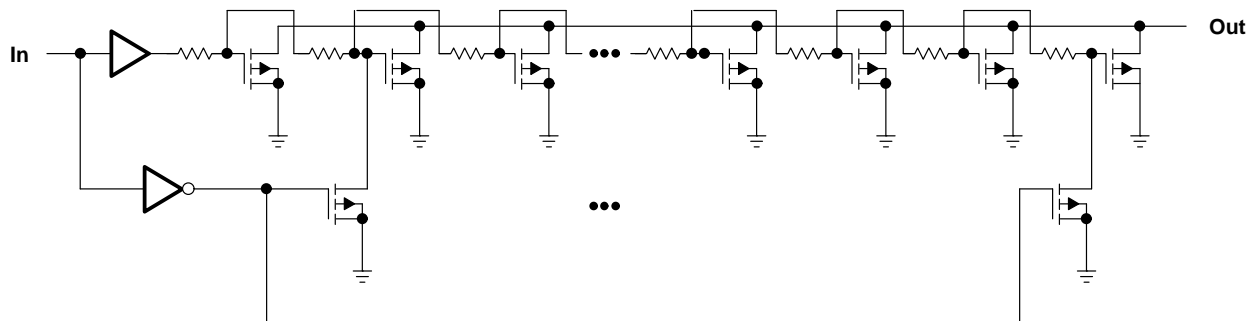


Figure 6. TI's Patented OEC Circuitry

The OEC circuitry implemented in output structures reduces simultaneous-switching noise by reducing the edge rate. The distributed output transistor with pull-down transistors evenly added gives a fast-turnoff feature to the circuit and minimizes the through current as well. The undesirable slow turnoff is resolved by evenly adding pull-down transistors to the distributed output transistor. Turnoff transistors minimize through current by rapidly turning off all the segments of the output-transistor circuit; therefore, the OEC method not only provides an effective means for controlling di/dt noise in high-speed CMOS FIFO products, but adds a fast-turnoff feature to the output circuit.

Dirty and Clean Grounds in 36-Bit FIFO Families

To reduce effects of simultaneous-switching noise on 36-bit FIFOs, TI divides the ground pins into dirty and clean ground terminals. A dirty ground is used only for device outputs and a clean ground is used for inputs and other internal circuit connections. A dirty ground is isolated from a clean ground on the chip, but users can connect them to the same external ground. Isolating the two grounds benefits the FIFO chips because output-switching noise does not affect the rest of the chip, thereby reducing the possibility of false clocks and intermittent data errors.

Simultaneous-Switching Tests Performed to Ensure Reliability of FIFO Products

SPICE Simulation

Simultaneous-switching SPICE simulations were performed for the SN74ACT3632 device during the design process for 36-bit FIFO products. Simulation results for SN74ACT3632 indicate that V_{CC} droop and ground bounce when 18 bits are switching simultaneously are only 4.39 and 0.67 V, respectively. When 36 bits are switching simultaneously, V_{CC} droop and ground bounce only change to 4 and 0.9 V, respectively. The results of this SPICE simulation illustrate the reliability of TI's high-performance FIFO products against ground noise⁶ (see Table 3).

Table 3. SPICE Simulations for the SN74ACT3632 Device When 18 or 36 Outputs Switch Simultaneously

SN74ACT3632 SWITCHING SIMULTANEOUSLY	V_{CC} DROOP (V)	GROUND BOUNCE (V)
18 bits	4.39	0.67
36 bits	4.0	0.9

Ground/Power-Noise Measurements (V_{OLP} and V_{OHV})

Noise measurements evaluate the performance of FIFO products while simultaneously switching the outputs. A typical simultaneous-switching test is performed to determine the magnitude of the disturbance on the output that is not being switched, as well as stored data integrity for devices with multiple outputs. The voltage induced on a quiescent output during simultaneous switching is referred to as V_{OLP} and V_{OHV} . For V_{OLP} (V_{OHV}) measurements, the output under test is held low (high) while the rest of the outputs are switching from high to low (low to high). V_{OLP} , the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs, is measured with respect to a ground reference near the output under test. V_{OHV} is the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. Table 4 summarizes the V_{OLP} and V_{OHV} results for 36-bit FIFO products. Data was taken on an automatic test machine (HP 82000) at room temperature (25°C).

Table 4. Sample V_{OLP} and V_{OHV} Test Results for 36-Bit FIFO Products

DEVICE	V_{OLP} (V)	V_{OHV} (V)	V_{CC} (V)
SN74ABT3614	0.75	0.2	5.5
SN74ACT3632	1.0	1.4	5.0

The results of V_{OLP} and V_{OHV} measurements performed on TI's 36-bit FIFO products indicate the reliability and noise immunity of TI's high-performance FIFO products. Sample waveforms for SN74ACT3638, SN74ACT3611, and SN74ACT3613 are presented in Appendix A.

Special Test Performed on 36-Bit FIFOs (V_{IH} and V_{IL} Testing)

V_{IH} and V_{IL} values for 36-bit FIFO families are tested while outputs are simultaneously switching. For example, the SN74ACT3632 continues to function properly with V_{IH} and V_{IL} values shown in Table 5. These results show that separating the output ground from the ground used for the rest of the chip results in excellent input-noise margins for the 36- and 32-bit-wide FIFOs.

Table 5. Test Required for the 36-Bit SN74ACT3632

V_{CC}	4.5 V	5.5 V
V_{IH}	1.8 V	1.9 V
V_{IL}	1.3 V	1.3 V

Summary

Fast switching speeds in today's technology require solutions to problems such as simultaneous-switching noise. The fast switching of drivers can cause uncontrolled noise spikes on the chip's ground bus, which lead to false clocks or incorrect data and control signals on the device. As more outputs of an IC switch simultaneously, noise effects increase and limit the usefulness of the device.

Better packaging options, multiple ground/power pins, output edge control, and separating the ground pins as clean and dirty ground pins reduce the simultaneous-switching noise. Finally, results obtained from simultaneous-switching tests are provided to illustrate the noise immunity of TI's high-performance FIFO devices.

References

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3. *Texas Instruments Advanced CMOS Logic Designer's Handbook*, 1988.
4. Craig Spurlin and Dale Stein, "EPIC Advance CMOS Logic Output Edge Control," *Texas Instruments Technical Journal*, March-April 1989,.
5. H. Hashemi, U. Ghoshal, K. Ziai, and P. Sandborn, "Analytical and Simultaneous Study of Switching Noise in CMOS Circuits," Proceedings of the Technical Conference, September 1990, pp. 762-773.
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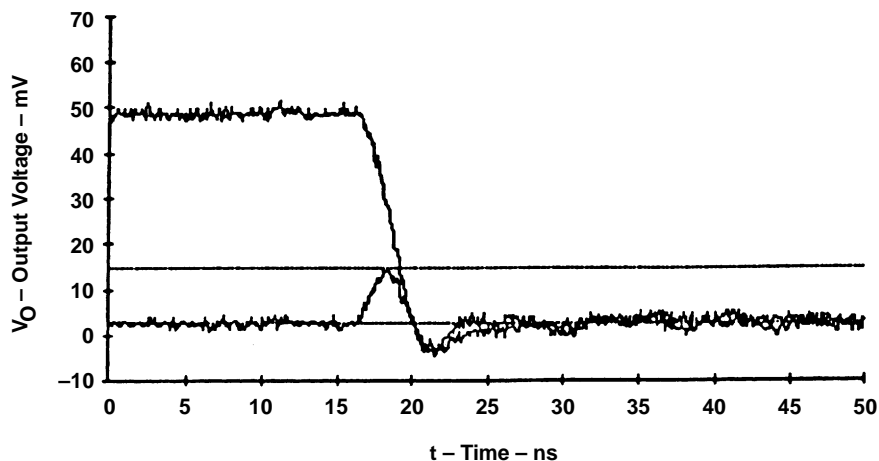
Acknowledgements

The V_{OLP} and V_{OHV} graphs in Appendix A are provided with the assistance of Al Sawyer.

Packaging information in Appendix B is provided by TI packaging engineers and organized by Tom Jackson.

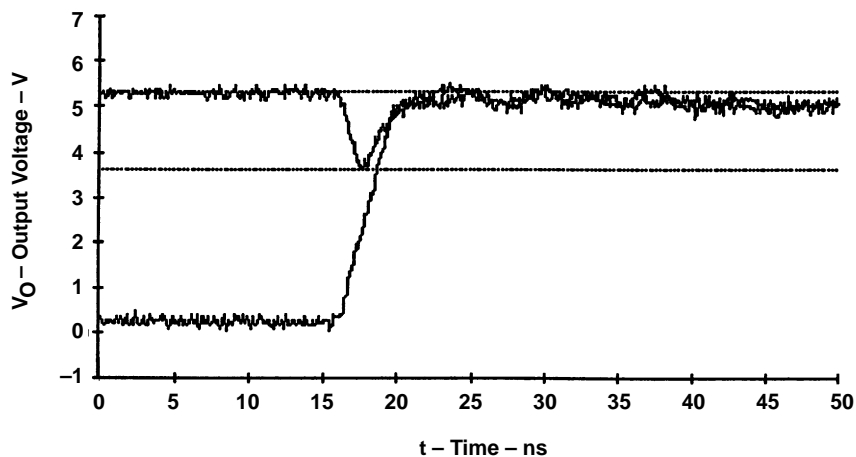
Appendix A

Appendix A shows V_{OLP} and V_{OHV} measurements during simultaneous switching. Measurements are made with respect to ground at 25°C with an HP8200 automatic test machine. V_1 is the quiescent voltage on the output being tested prior to switching other outputs. V_2 is the peak voltage on the output being tested while switching other outputs. V_D is the difference in V_1 and V_2 .



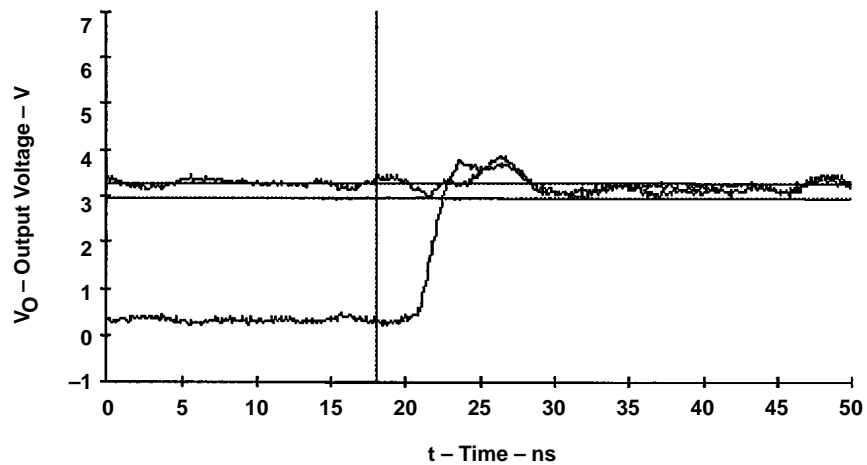
$$V_1 = 25 \text{ mV}, V_2 = 14.7 \text{ mV}, V_D = 12.2 \text{ mV}$$

Figure A-1. SN74ACT3638 V_{OLP} , $V_{CC} = 5.5 \text{ V}$



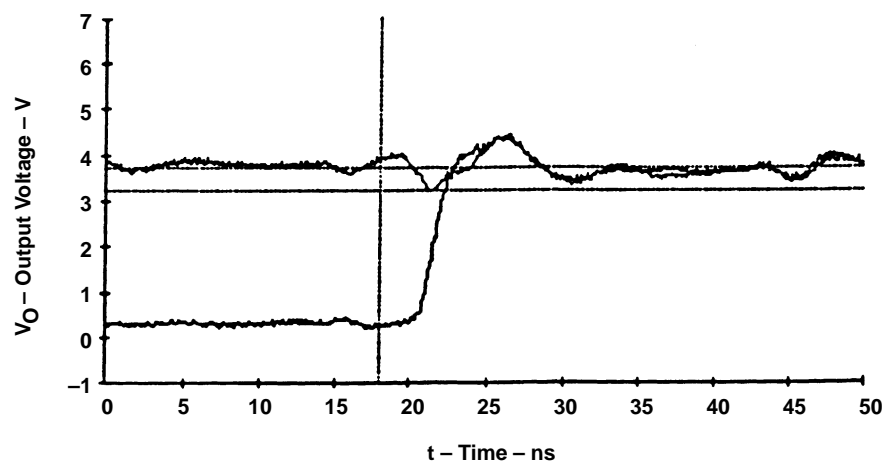
$$V_1 = 3.63 \text{ V}, V_2 = 5.31 \text{ V}, V_D = 1.69 \text{ V}$$

Figure A-2. SN74ACT3638 V_{OHV} , $V_{CC} = 5.5 \text{ V}$



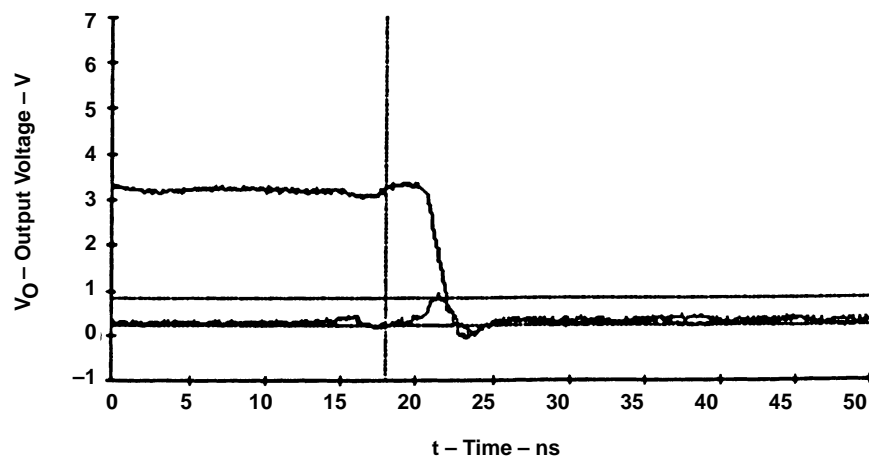
$V_1 = 3.25$ V, $V_2 = 2.93$ V, $V_D = -312.5$ mV

Figure A-3. SN74ABT3611 V_{OHV} , $V_{CC} = 5$ V



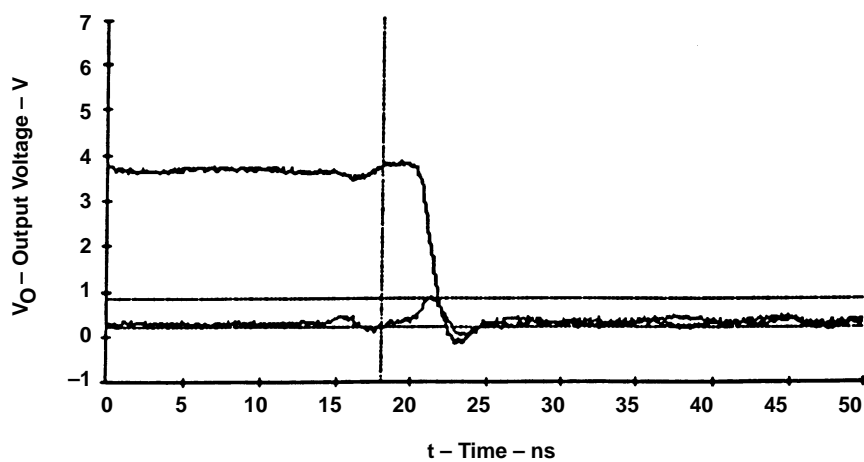
$V_1 = 3.71$ mV, $V_2 = 3.21$ mV, $V_D = -500$ mV

Figure A-4. SN74ABT3611 V_{OHV} , $V_{CC} = 5.5$ V



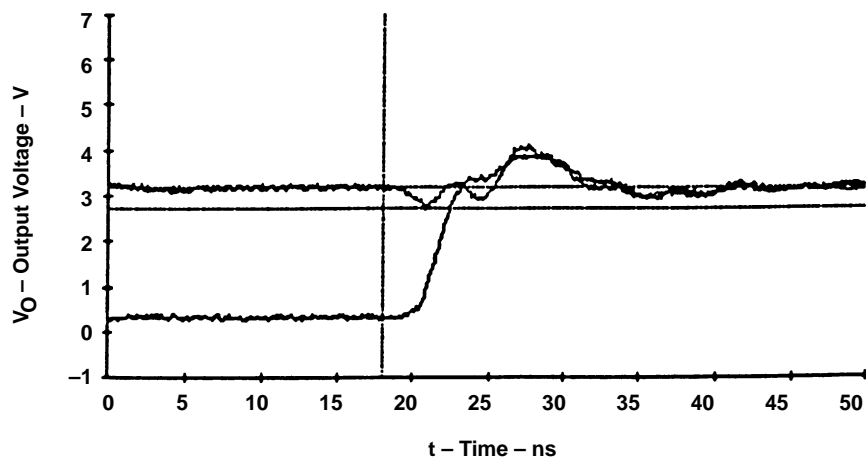
$V_1 = 218.75 \text{ mV}$, $V_2 = 843.75 \text{ mV}$, $V_D = 625 \text{ mV}$

Figure A-5. SN74ABT3611 V_{OLP} , $V_{CC} = 5 \text{ V}$



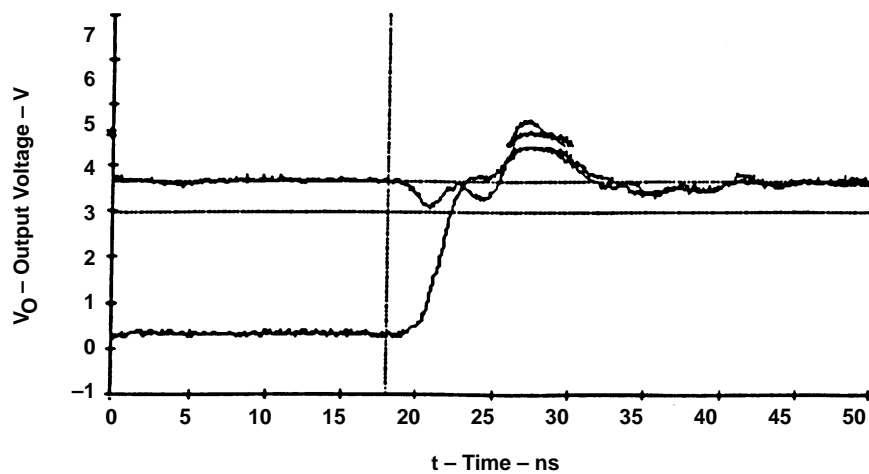
$V_1 = 218.75 \text{ mV}$, $V_2 = 843.75 \text{ mV}$, $V_D = 625 \text{ mV}$

Figure A-6. SN74ABT3611 V_{OLP} , $V_{CC} = 5 \text{ V}$



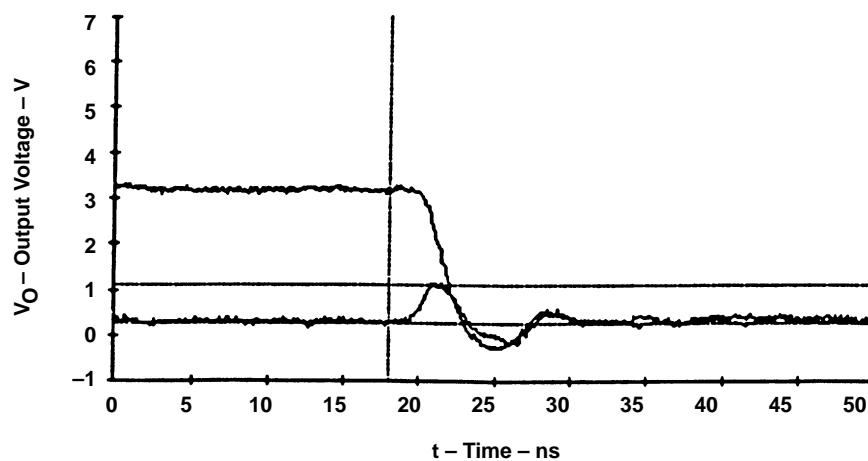
$V_1 = 3.18$ V, $V_2 = 2.71$ V, $V_D = -468.75$ mV

Figure A-7. SN74ABT3613 V_{OHV} , $V_{CC} = 5$ V



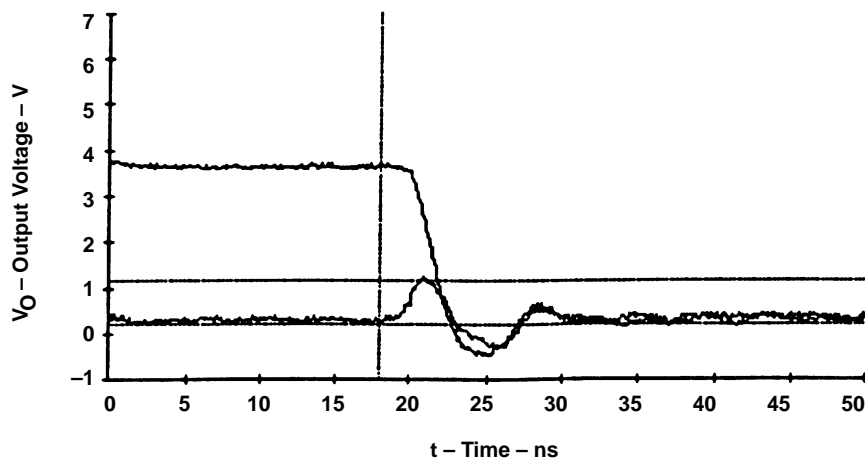
$V_1 = 3.18$ V, $V_2 = 2.71$ V, $V_D = -468.75$ mV

Figure A-8. SN74ABT3613 V_{OHV} , $V_{CC} = 5.5$ V



$$V_1 = 250\text{ mV}, V_2 = 1.12\text{ V}, V_D = 875\text{ mV}$$

Figure A-9. SN74ABT3613 V_{OLP} , $V_{CC} = 5\text{ V}$



$$V_1 = 218.75\text{ mV}, V_2 = 1.18\text{ V}, V_D = 968.75\text{ mV}$$

Figure A-10. SN74ABT3613 V_{OLP} , $V_{CC} = 5.5\text{ V}$

Appendix B

FIFO Package Types

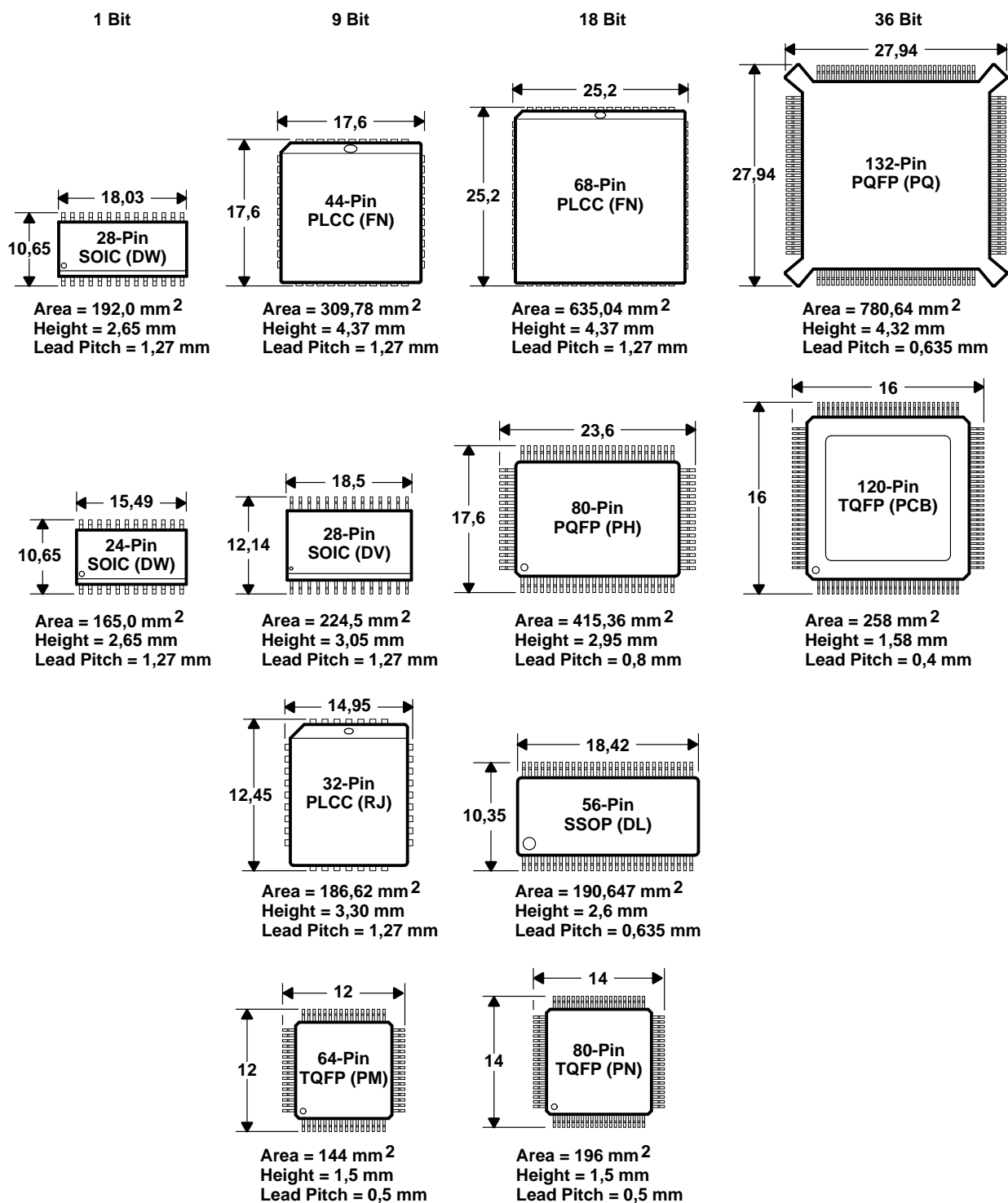
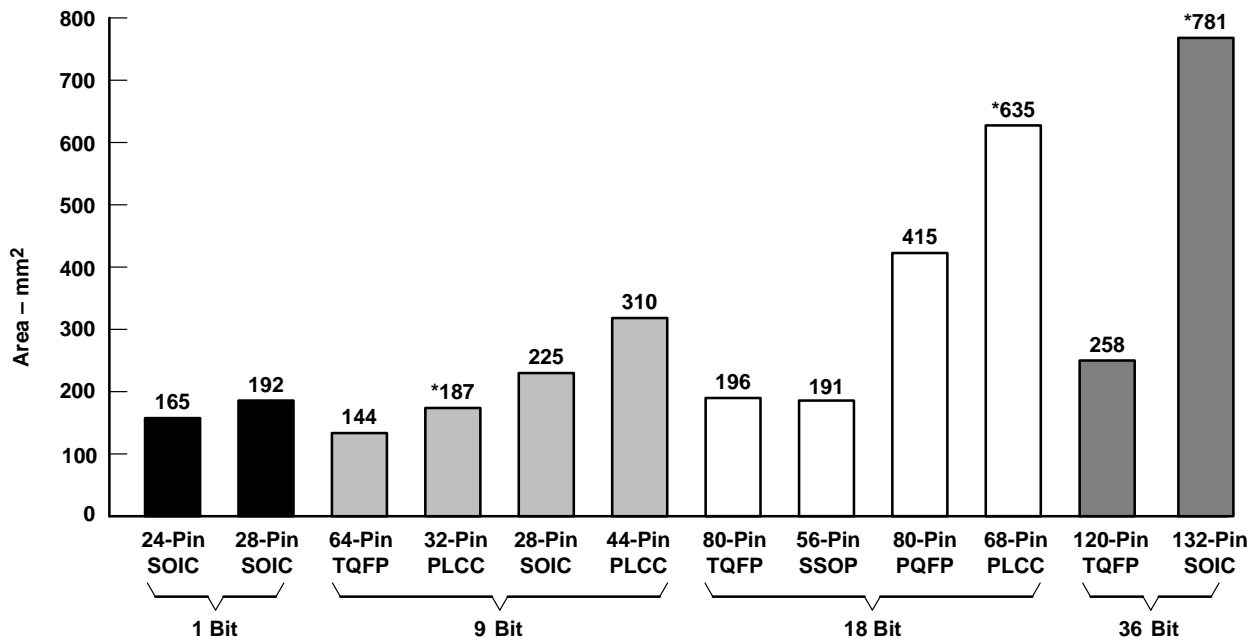


Figure B-1. Surface-Mount Package Options



*Competitors' Best Solution

Figure B–2. Surface-Mount Package Area by Package Type