FIFOs With a Word Width of One Bit

First-In, First-Out Technology

Peter Forstner
Mixed Signal Logic Products

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TEXAS INSTRUMENTS

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Introduction

In every digital system, data is continually being exchanged between various subsystems. Intermediate storage is always necessary if data arrives at the receiving subsystem at a high rate or in batches but can then only be processed slowly or irregularly. Such *intermediate stores* are familiar to us in our daily lives, for example, as queues of customers at the checkout of a supermarket or cars waiting at traffic lights. The checkout of goods at the supermarket point of sale proceeds slowly and regularly, while customers arrive there unpredictably; if many customers all want to pay at the same time, a queue builds up that the cashier processes on the principle of *first come, first served*. Queues of cars at traffic lights result from the sporadic arrival of traffic, which the lights allow to proceed only in regular batches.

An intermediate store or memory that operates on the above principle is known as a first-in, first-out (FIFO) memory. The first data written into a FIFO is also the first to leave it at readout. Texas Instruments (TI) offers a variety of FIFOs. These are available with word widths from 1 bit to 36 bits, storage densities from 64 to 2048 words of data, and clock speeds of up to 80 MHz. This application report is concerned exclusively with FIFOs having a word width of one bit and it suggests various possible applications for them.

Whenever a buffer memory is needed for serial-data transmission, there is a requirement for 1-bit-wide FIFOs. Digital telecommunications, local-area networks (LANs), serial transmission of data with the help of data compression, and communication between signal processors are all examples of serial data-transfer applications that require 1-bit-wide FIFOs. In some applications, the FIFOs are already integrated into the application-specific integrated circuit (ASIC) or the chip set with LANS. However, very often *discrete* FIFO components are required.

FIFO Basics

Every memory component for which the first word of data written to the memory is also the first to leave it when the memory is read out can be classified as a FIFO (see Figure 1). In practice, a further characteristic often required from a FIFO is asynchronism between the writing and reading processes. This kind of FIFO is known as an asynchronous FIFO.

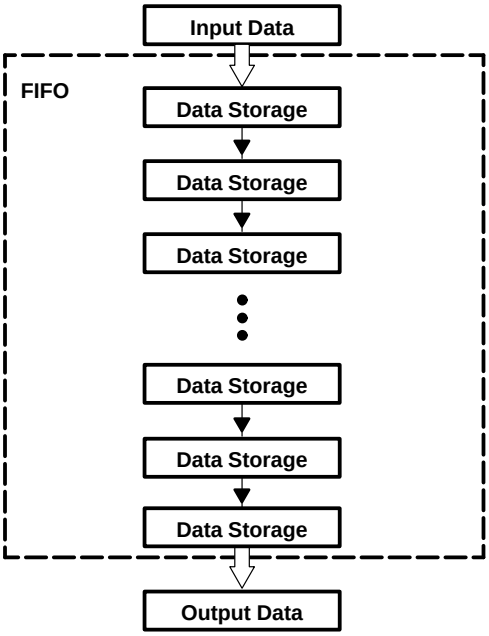


Figure 1. First-In, First-Out Data Flow

A FIFO has an input to which data words are written and a separate output from which data words are read. Since writing can take place completely asynchronously to reading, it is permissible for the writing and reading pulses to have completely different clock speeds, chosen at will. Control signals such as full, empty, half full, and almost full allow the controlling circuitry to monitor the internal state of the FIFO before every writing or reading process.

According to the control signals to write and read, asynchronous FIFOs can be classified into two groups; strobed FIFOs (see Figure 2) and clocked FIFOs (see Figure 3).

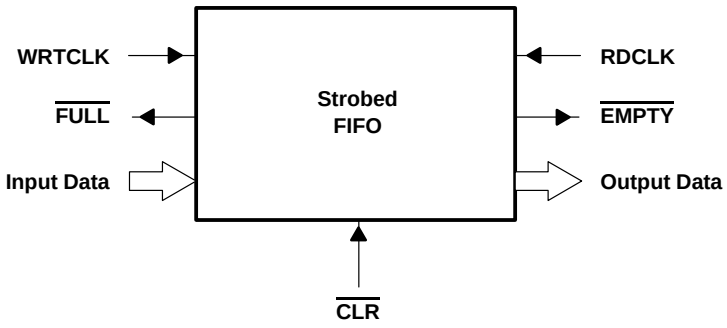


Figure 2. Connections of a Strobed FIFO

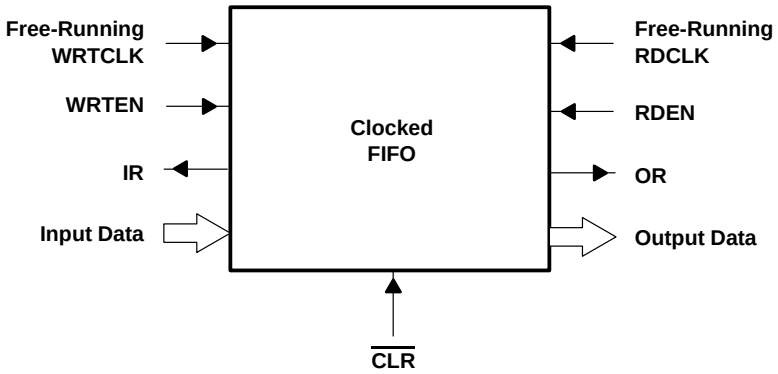


Figure 3. Connections of a Clocked FIFO

The strobed FIFO enters a word of data into its internal memory at every rising (or every falling) edge of the write clock (WRTCLK). $\overline{\text{FULL}}$ shows whether there is room in the memory for a data word. Reading a data word takes place at every rising (or falling) edge of the read clock (RDCLK). If there is no data word awaiting readout, this is indicated by the status signal $\overline{\text{EMPTY}}$. The disadvantage of this kind of FIFO is that the status signals cannot be fully synchronized with the corresponding clock signals.

Clocked FIFOs require a free-running write clock (WRTCLK) and read clock (RDCLK). The writing and reading processes are controlled by the control signals write enable (WRTEN) and read enable (RDEN). The status signals input ready (IR) and output ready (OR) indicate the internal state of the FIFO. As a result of the two free-running clock signals, all status signals can be synchronized within the FIFO. The IR signal changes its level exclusively in synchronism with the writing pulse, while OR switches synchronously with the reading pulse.

The 1-bit FIFOs in this application report (SN74ACT2226, SN74ACT2227, SN74ACT2228, and SN74ACT2229) are, without exception, clocked FIFOs with complete built-in synchronization of all available status signals, including:

Output ready (OR) synchronized with read clock (RDCLK)

Input ready (IR), half full (HF), and almost full/almost empty (AF/AE) synchronized with write clock (WRTCLK)

Telecommunications

The rapidly increasing need for telecommunication installations cannot, in the long run, be met by providing a separate line for every telephone connection; the simultaneous use of one line for several channels is a requirement. Digital transmission via pulse-code modulation (PCM) techniques enables the cost-effective use of single lines for multichannel transmission. Using these techniques, digitized telephone signals are switched successively onto a connecting line with the help of a multiplexer and separated from one another at the end of the line with a demultiplexer (see Figure 4).

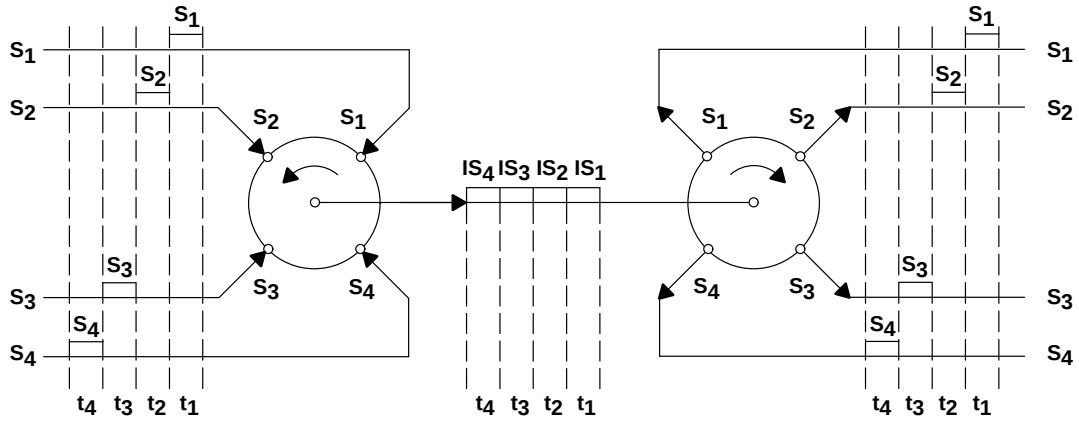


Figure 4. Time-Division Multiplex of Several Channels

With the 3.4-kHz upper bandwidth limit of a telephone channel and the internationally standardized sampling frequency for digitizing the signal (f_0 = 8 kHz), there remains enough space in the frequency band to insert the edge of the necessary bandwidth-limiting low-pass filter.

Although extensive tests of syllable intelligibility have shown that 7-bit quantization with 128 quantization intervals is adequate even with successive analog-to-digital-to-analog conversion, an 8-bit quantization with 256 intervals has been made the standard. For the compression of the instantaneous value of the signal, the logarithmic 13-segment characteristic shown in Figure 5 is used.

For the transmission of a channel, a bit rate of 8 kHz × 8 bit = 64 kbit/s is necessary and, correspondingly, a line for 32 multiplexed channels must attain a transmission rate of 64 kbit/s × 32 = 2048 kbit/s (CCITT recommendations G.732 and G.704).

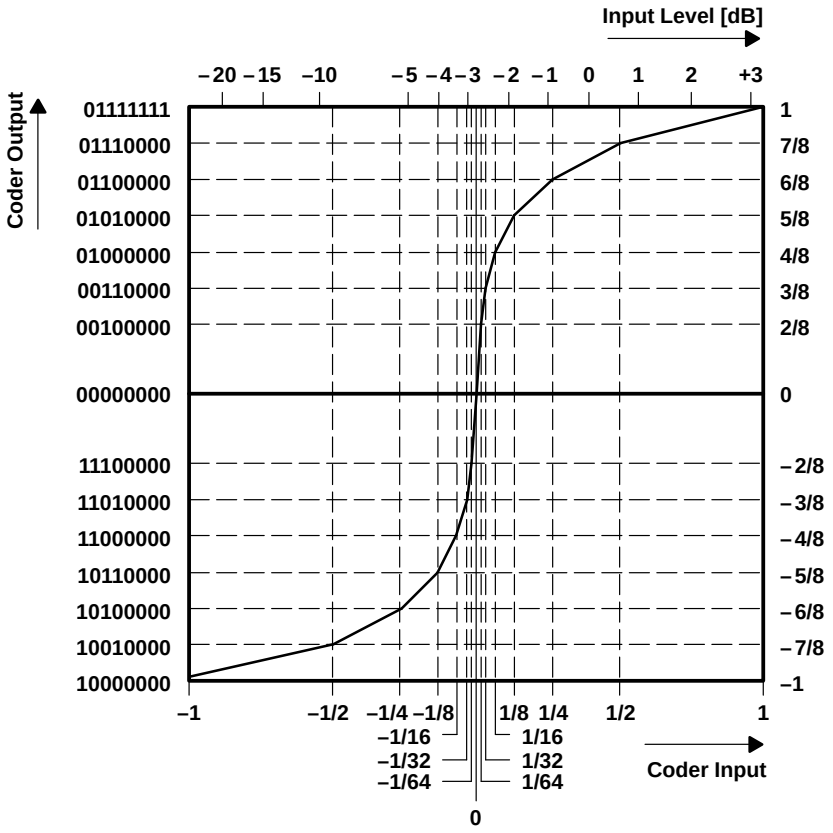


Figure 5. Logarithmic 13-Segment Characteristics for the Coding of Telephone Signals

Digital-Transmission Methods

At present, four different digital-transmission methods are used for telecommunications:

European plesiochronous digital hierarchy (PDH, see Table 1)

American plesiochronous digital hierarchy (PDH, see Table 1)

Japanese plesiochronous digital hierarchy (PDH, see Table 1)

Synchronous digital hierarchy (SDH, see Table 2)

Signals coming from various clock generators should have the same bit speeds but, in practice, the bit speed may deviate by a certain tolerance from the nominal value. These signals are referred to as plesiochronous signals.

The lack of worldwide standardization of the three PDH transmission methods makes world networking much more difficult, and the use of equipment from various manufacturers is limited to the networks of individual national telecommunications organizations. The fact that the standard for synchronous digital hierarchy (SDH, see Table 2) has worldwide validity does, however, offer the promise of assistance. SDH evolved from the North American synchronous optical network (SONET) specifications but is based (as described in the CCITT recommendations G.707, G708, and G709) on a bit rate of 155520 kbit/s (see Table 2); that is, exactly three times the SONET basic bit rate of 51840 kbit/s. The SDH basic signal is designated as synchronous transport module level one (STM-1); higher hierarchy levels are whole integer multiples of the level-one bit rate.

Table 1. Plesiochronous Digital Hierarchies

HIERARCHY LEVEL	HIERARCHIES BASED ON 2 Mbit/s	HIERARCHIES BASED ON 1.5 Mbit/s	
	EUROPE, SOUTH AMERICA	USA	JAPAN
1	2048 kbit/s	1544 kbit/s	1544 kbit/s
2	8448 kbit/s	6312 kbit/s	6312 kbit/s
3	34368 kbit/s	44736 kbit/s	32064 kbit/s
4	139264 kbit/s		97728 kbit/s

Table 2. Synchronous Digital Hierarchy and SONET

BIT RATE	SDH		SONET	
	LEVEL	SIGNAL IDENTIFICATION	LEVEL	SIGNAL IDENTIFICATION
51840 kbit/s			STS-1	OC-1
155520 kbit/s	1	STM-1	STS-3	OC-3
466560 kbit/s			STS-9	OC-9
622080 kbit/s	4	STM-4	STS-12	OC-12
933120 kbit/s			STS-18	OC-18
1244160 kbit/s			STS-24	OC-24
1866240 kbit/s			STS-36	OC-36
2488320 kbit/s	16	STM-16	STS-48	OC-48

A PDH Application Example

The plesiochronous digital hierarchy and the application of FIFOs for the synchronization of the PDH signals are demonstrated using as an example European transmissions based on a bit speed of 2048 kbit/s.

Frame Structure of the First Hierarchy Level

The bit speed of the first hierarchy level (2048 kbit/s, see Table 1) allows the transmission of 32 telephone channels, each of 64 kbit/s, over a normal telephone line. In this case, only 30 telephone conversations are transmitted, since two channels are required for the following additional information (see Figure 6):

Frame recognition word for the synchronization of the receiver

Cyclic-redundancy-check (CRC4) bits for the recognition of bit faults during the transmission

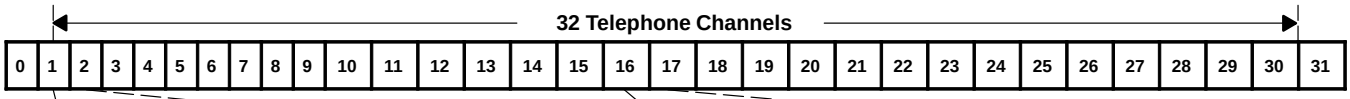
Service bits for initiating alarms

Registration bits for national and international telecommunication traffic

Telephone exchange technical identification (signalization)

Each of the eight bits of the 32 channels is multiplexed bit by bit; that is, bit 0 of the 32 channels is first sent serially over the line followed by 32 times bit 1, etc. These 8×32 bits = 256 bits are consolidated in a frame (see Figure 6). Channels 0 and 16 contain the necessary control information, while the remaining channels can be used for the transmission of 30 telephone connections. The transmission of a 256-bit frame of this kind at 2048 kbit/s requires a time period of 125 µs.

Sixteen frames together make up a $16 \times 256 = 4096$-bit multiple frame with a transmission time period of 2 ms. The 256 control bits in channels 0 and 16 can be seen in Figure 6.



FRAME NO.	FRAME BITS							
	1	2	3	4	5	6	7	8
0	C_1	0	0	1	1	0	1	1
1	D	1	D	N	S_n	S_n	S_n	S_n
2	C_2	0	0	1	1	0	1	1
3	0	1	D	N	S_n	S_n	S_n	S_n
4	C_3	0	0	1	1	0	1	1
5	0	1	D	N	S_n	S_n	S_n	S_n
6	C_4	0	0	1	1	0	1	1
7	0	1	D	N	S_n	S_n	S_n	S_n
8	C_1	0	0	1	1	0	1	1
9	0	1	D	N	S_n	S_n	S_n	S_n
10	C_2	0	0	1	1	0	1	1
11	0	1	D	N	S_n	S_n	S_n	S_n
12	C_3	0	0	1	1	0	1	1
13	0	1	D	N	S_n	S_n	S_n	S_n
14	C_4	0	0	1	1	0	1	1
15	0	1	D	N	S_n	S_n	S_n	S_n

FRAME NO.	FRAME BITS							
	1	2	3	4	5	6	7	8
0	0	0	0	0	X	Y	X	X
1	a_1	b_1	c_1	d_1	a_{17}	b_{17}	c_{17}	d_{17}
2	a_2	b_2	c_2	d_2	a_{18}	b_{18}	c_{18}	d_{18}
3	a_3	b_3	c_3	d_3	a_{19}	b_{19}	c_{19}	d_{19}
4	a_4	b_4	c_4	d_4	a_{20}	b_{20}	c_{20}	d_{20}
5	a_5	b_5	c_5	d_5	a_{21}	b_{21}	c_{21}	d_{21}
6	a_6	b_6	c_6	d_6	a_{22}	b_{22}	c_{22}	d_{22}
7	a_7	b_7	c_7	d_7	a_{23}	b_{23}	c_{23}	d_{23}
8	a_8	b_8	c_8	d_8	a_{24}	b_{24}	c_{24}	d_{24}
9	a_9	b_9	c_9	d_9	a_{25}	b_{25}	c_{25}	d_{25}
10	a_{10}	b_{10}	c_{10}	d_{10}	a_{26}	b_{26}	c_{26}	d_{26}
11	a_{11}	b_{11}	c_{11}	d_{11}	a_{27}	b_{27}	c_{27}	d_{27}
12	a_{12}	b_{12}	c_{12}	d_{12}	a_{28}	b_{28}	c_{28}	d_{28}
13	a_{13}	b_{13}	c_{13}	d_{13}	a_{29}	b_{29}	c_{29}	d_{29}
14	a_{14}	b_{14}	c_{14}	d_{14}	a_{30}	b_{30}	c_{30}	d_{30}
15	a_{15}	b_{15}	c_{15}	d_{15}	a_{31}	b_{31}	c_{31}	d_{31}

0011011 **Frame Recognition Word**
$C_4 \ldots C_1$ **CRC4 Control Bits**
D, N **Bits for Alarm Initiation**
S_i, S_n **Registration Bits**

0000XYXX **Multiple Frame Recognition Word**
$a_n \ldots d_n$ **Signalization for Channel n**

Figure 6. Frame Structure of the 2048-kbit/s Multiplex Signal (First Hierarchy Level)

Frame Structures of the Second to Fifth Hierarchy Levels

For further sections, four 2048-kbit/s signals are transmitted with successive bit-by-bit time-division multiplexing combined with the pulse-stuffing procedure at bit speeds of 8448 kbit/s, 34368 kbit/s, 139264 kbit/s, and 564992 kbit/s.

If several plesiochronous signals are multiplexed, they must be synchronized before the multiplexing process. Plesiochronous signals have nominally the same bit speeds; but, in practice, the following kinds of asynchronism can arise:

The bit rates deviate from one another within the specified tolerance (drift).

As a result of long transmission distances and significant differences of temperature, etc., the bit speeds fluctuate for short periods (jitter).

For the synchronization of many plesiochronous 2048 kbit/s signals, positive pulse-stuffing techniques are used when multiplexing these signals into an 8-mbit/s signal. The principle of this technique is based on the fact that, in the multiplexed signal, a bandwidth is made available that is wider than the nominal bit rate requires. If at particular points in the transmission information bits or empty bits (so-called stuffing bits) are sent out, the bit speed can be reduced and thus adjusted to suit the input signal. This technique also compensates for drift and jitter of the input signal.

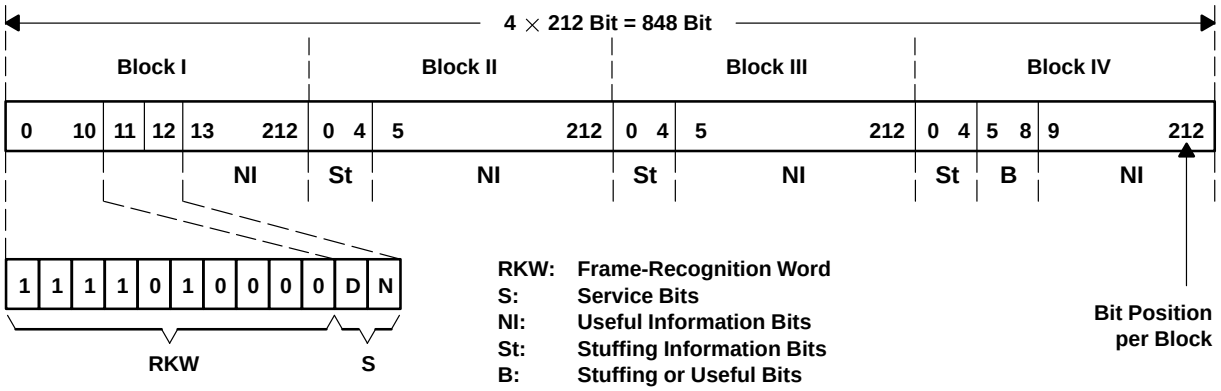


Figure 7. Frame Structure of the 8448-kbit/s Multiplex Signal (Second Hierarchy Level)

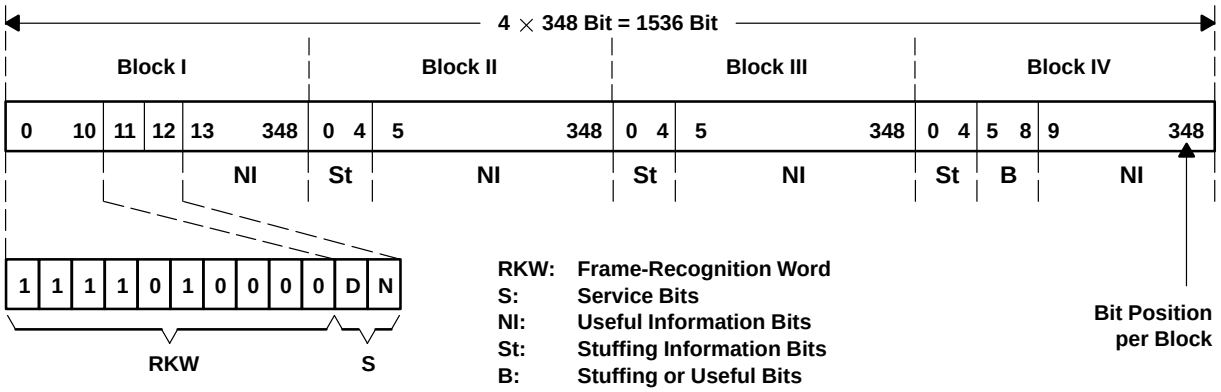


Figure 8. Frame Structure of the 34368-kbit/s Multiplex Signal (Third Hierarchy Level)

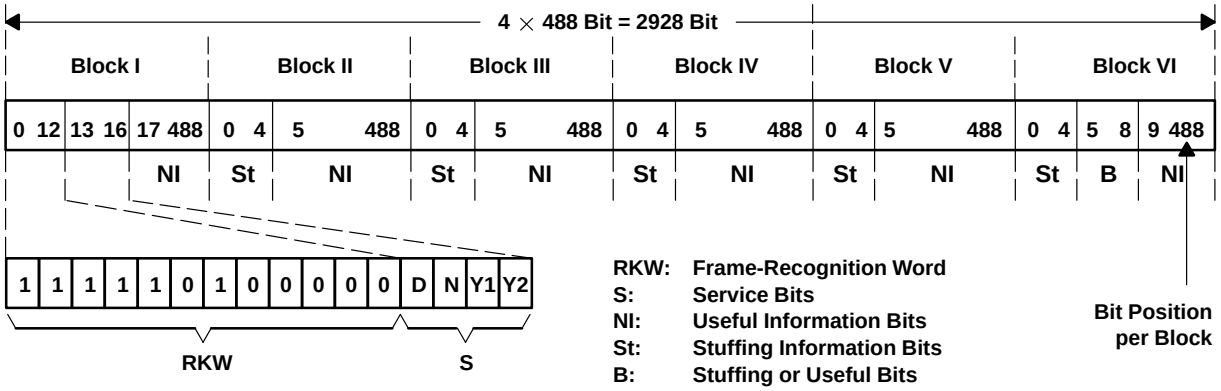


Figure 9. Frame Structure of the 139264-kbit/s Multiplex Signal (Fourth Hierarchy Level)

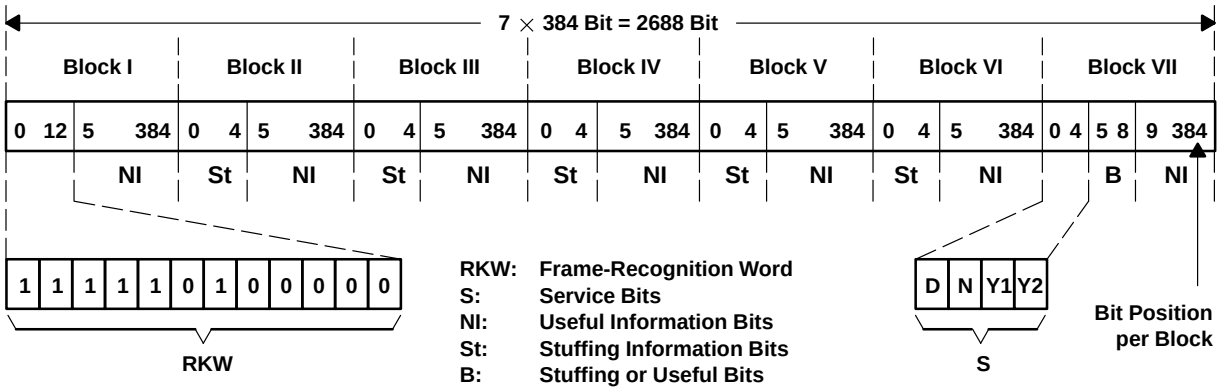


Figure 10. Frame Structure of the 564992-kbit/s Multiplex Signal (Fifth Hierarchy Level)

When multiplexing with positive pulse-stuffing techniques, a frame that is constructed with a 8448-kbit/s signal is partitioned into four blocks (see Figure 7). This frame structure envisages four stuffing bits in block IV in bit positions 5 to 8. These stuffing bits can either contain useful information or they can be empty bits. The stuffing information in bit positions 1 to 4 in blocks II, III, and IV indicates whether empty bits or useful bits are present in block IV. This 4-bit stuffing information is transmitted three times (blocks II, III, and IV) to assure a correct decision about the information content of the stuffing bits in the case of bit faults within the stuffing information. If there is a conflict between the individual bits of the three transmissions of stuffing bits, a majority decision can be used to avoid a false conclusion that would result in a bit slip and, consequently, a loss of synchronization of the 2-mbit/s systems. If, for example, one of the bit combinations 0-0-0, 0-0-1, 0-1-0, or 1-0-0 is received as stuffing information in blocks II, III, and IV for the first stuffing bit, a useful bit follows at bit position 5 in block IV; the reception of 1-1-1, 1-1-0, 1-0-1, or 0-1-1 indicates an empty bit. A 2-bit fault in the stuffing information results in the loss or gain of a bit (bit slip) and, consequently, in loss of the frame synchronism of the multiplexed signals.

Techniques similar to multiplexing with positive pulse stuffing with the 8448-kbit/s signal are also performed with the 34368-kbit/s, 139264-kbit/s, and 564992-kbit/s signals (see Figures 8, 9, and 10).

As a result of these stuffing techniques, a 8448-kbit/s frame has a transmission speed in the range of 8169-kbit/s to 8209-kbit/s useful bits. With the nominal transmission speed for four multiplexed 2048-kbit/s signals of 8192-kbit/s, fluctuations in the transmission speed in the range of about ±0.2% can be compensated for (see Tables 3, 4, 5, and 6).

Table 3. Spread of the Transmission Capacity of an 8448-kbit/s Signal Consisting of Four Multiplexed 2048-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 2048 kbit/s = 8192 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	848 bits	820 bits	822 bits	824 bits
Transmission Speed	8448 kbit/s	8169 kbit/s	8189 kbit/s	8209 kbit/s
Nominal Value		8192 kbit/s	8192 kbit/s	8192 kbit/s
Deviation from Nominal Value		−0.28%	−0.04%	+0.21%

Table 4. Spread of the Transmission Capacity of a 34368-kbit/s Signal Consisting of Four Multiplexed 8448-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 8448 kbit/s = 33792 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	1536 bits	1508 bits	1510 bits	1512 bits
Transmission Speed	34368 kbit/s	33742 kbit/s	33786 kbit/s	33831 kbit/s
Nominal Value		33792 kbit/s	33792 kbit/s	33792 kbit/s
Deviation from Nominal Value		−0.15%	−0.02%	+0.12%

Table 5. Spread of the Transmission Capacity of a 139264-kbit/s Signal Consisting of Four Multiplexed 34368-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 34368 kbit/s = 137472 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BIts
Frame Capacity	2928 bits	2888 bits	2890 bits	2892 bits
Transmission Speed	139264 kbit/s	137361 kbit/s	137457 kbit/s	137552 kbit/s
Nominal Value		137472 kbit/s	137472 kbit/s	137472 kbit/s
Deviation from Nominal Value		−0.08%	−0.01%	+0.06%

Table 6. Spread of the Transmission Capacity of a 564992-kbit/s Signal Consisting of Four Multiplexed 139264-kbit/s Signals With a Net Nominal Transmission Speed of 4 × 139264 kbit/s = 557056 kbit/s

	FRAME	USEFUL BITS		
		0 STUFFING BITS	2 STUFFING BITS	4 STUFFING BITS
Frame Capacity	2688 bits	2648 bits	2650 bits	2652 bits
Transmission Speed	564992 kbit/s	556584 kbit/s	557005 kbit/s	557425 kbit/s
Nominal Value		557056 kbit/s	557056 kbit/s	557056 kbit/s
Deviation from Nominal Value		−0.08%	−0.01%	+0.07%

Clock Adjustment With FIFOs

Clock Adjustment at the Transmitting End

A block diagram showing the principle of clock adjustment at the transmitting end with positive pulse-stuffing techniques is shown in Figure 11. In this case, each channel is provided with an elastic memory in the form of a FIFO.

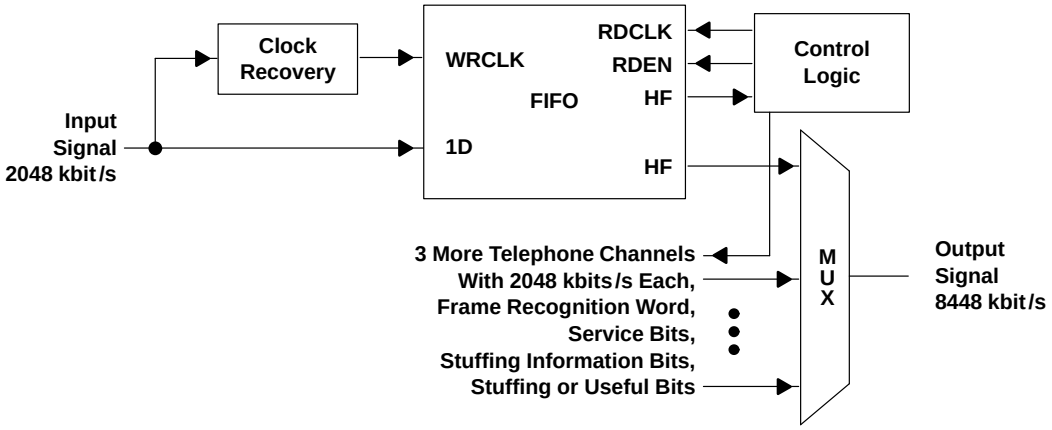


Figure 11. Clock Adjustment at the Transmitting End With Positive Pulse-Stuffing Techniques Block Diagram

The input data is written into this FIFO with the help of a circuit for clock recovery. The FIFO takes on the buffering of the input data while the frame and stuffing information is being transmitted. If information bits are to be transmitted, the control logic of the transmission path extracts the data from the FIFO. With positive pulse-stuffing techniques, the net bit speed of the transmission path is slightly higher than the bit speed of the incoming signal. As a result, the transmission-path controller reads the data from the FIFO more quickly than it can deliver it to the input channel. Whenever the FIFO contains less than a certain minimum filled level (e.g., half full), the transmission path sends at the next possible moment a stuffing bit instead of a data bit. As a result, the input channel has enough time to raise the filled level of the FIFO above the specified minimum level by writing in further data (see Figure 12).

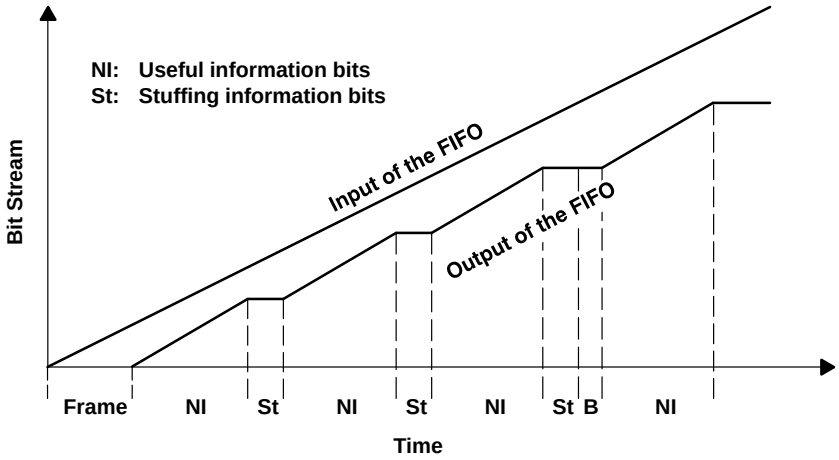


Figure 12. Bit Stream at the FIFO of the Transmitter-Clock Adjustment

If the minimum level of the FIFO when sending block II (see Figure 7) is not reached, the stuffing information in block II can no longer be changed. Accordingly, a wait must be made until the next frame when the necessary stuffing-information bits and the associated stuffing bits can be transmitted. The maximum number of data words that can be stored in the FIFO should be

Clock Adjustment at the Receiving End

There is also an elastic memory (FIFO) at the receiving end of each channel. Figure 15 shows that the information is written into the FIFO with the multiplex clock pulse divided by n. As a result of the now well-known frame structure, writing must be inhibited while the additional information is being received. The writing process also must be interrupted when stuffing bits are received (see Figure 13). Consequently, received data is written into the FIFO block by block (see Figure 14).

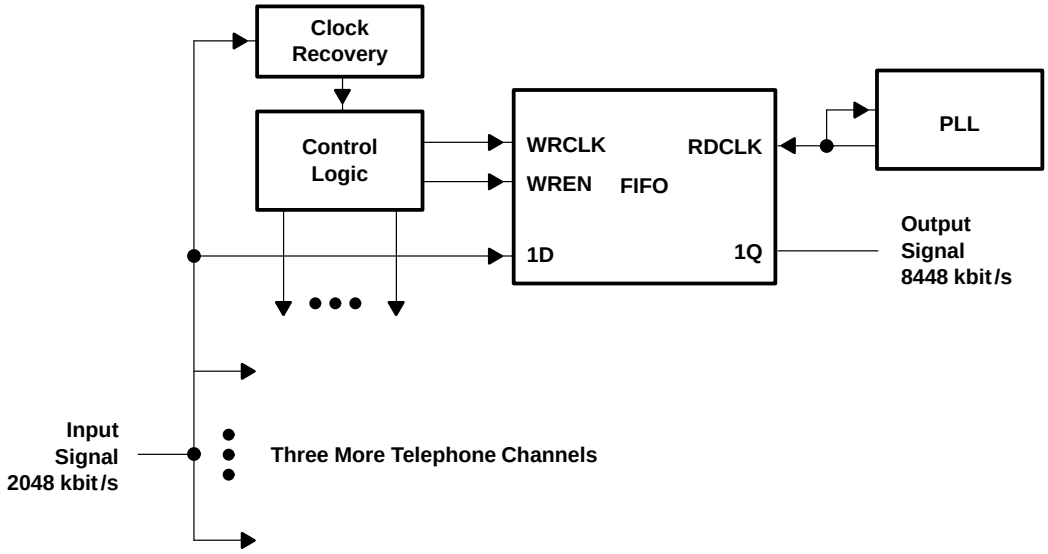


Figure 13. Clock Adjustment at the Receiving End With Positive Pulse-Stuffing Techniques Block Diagram

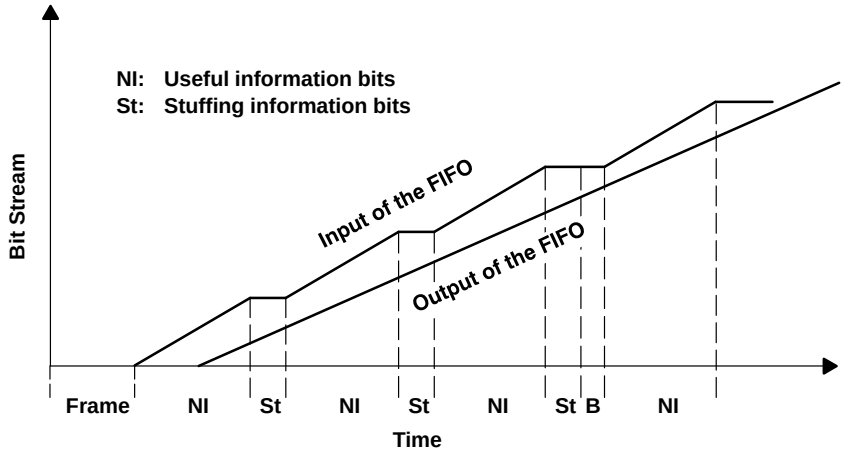


Figure 14. Bit Stream at the FIFO of the Receiver-Clock Adjustment

The write clock of the FIFO has as a nominal clock frequency (the multiplex clock divided by n); however, during the reception of the frame and the stuffing bits, several clock periods are omitted. Over a long period of time, the bit speed is identical with that of the original signal at the transmitter end (see Figure 15). As a read pulse for the FIFO, a regular clock without gaps is needed so that a continual bit stream conforming to the original signal is supplied. A PLL circuit reconstitutes this continuous clock signal from the clock signal containing gaps, although there is a small amount of jitter.

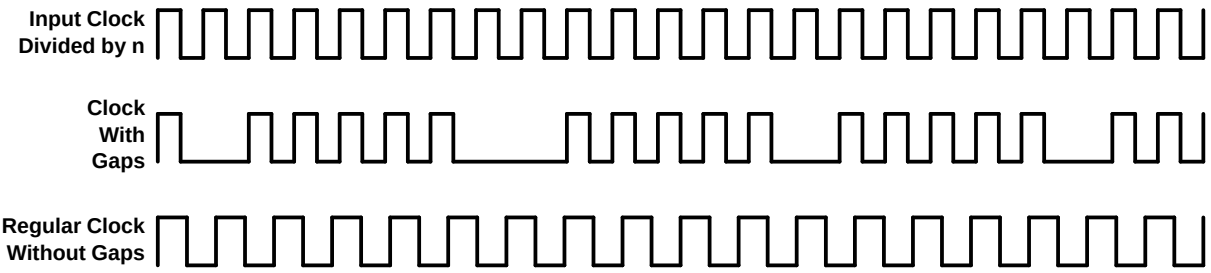


Figure 15. Clock Signals at the Receiver

Types of FIFOs Suitable for Clock Adjustment

The width of a FIFO data word for clock adjustment at the transmitting or receiving end is merely one bit and, consequently, the FIFOs listed in Table 7 can be considered as candidates for this application.

Table 7. One-Bit FIFOs From TI

FIFO TYPE	SN74ACT2226	SN74ACT2227	SN74ACT2228	SN74ACT2229
Word Width	1 bit	1 bit	1 bit	1 bit
Memory Capacity	64 words	64 words	256 words	256 words
FIFOs per Package	2	2	2	2
Clocked FIFO	√	√	√	√
f_{max}	22 MHz	60 MHz	22 MHz	60 MHz
Totem-Pole Q Output	√		√	
3-State Q Output		√		√
Half-Full Flag	√	√	√	√
Almost-Full Flag	√	√	√	√

Modems With Data Compression

Modems are now widely used for transmitting data over telephone lines. The telephone network was, however, originally developed for speech communications and for the transmission of analog audio signals. The result is that only alternating-current signals having an upper bandwidth limit of 3.4 kHz can be transmitted. Binary-digital information must be modulated, or converted, into another kind of signal. With acoustic couplers, frequency modulation is used such that a 0 is audible as a high note and a 1 as a lower note. This frequency-modulated signal is analog, with 2100 Hz used for 0 and 1700 Hz for 1. These frequencies lie within the frequency band that can be transmitted over a telephone line. The maximum transmission rate is only 600 baud.

Since significantly higher frequencies cannot be transmitted by a telephone network, a trick must be used to attain higher transmission speeds. If the number of possible states (e.g., frequencies) is created from two to four, two bits can be transmitted simultaneously without exceeding the upper bandwidth limit of 3.4 kHz. A further sophistication of this multistage modulation process to 16 or even 32 states (4 or 5 bits can be simultaneously transmitted) resulted in modems having a transmission capacity of up to 9600 bit/s but at the same time a transmission system that was more susceptible to interference.

A further increase of transmission speed by means of yet more sophisticated modulation methods would have been difficult; therefore, data compression has been used to improve performance. This involves examining the bit stream for redundant information, then compressing it. The receiver recognizes the parts of the signal that have been compressed and expands them in order to reconstitute the original signal. In a typical case, redundancy of the transmitted bit stream allows a 50% reduction of the original data, whereby the possibility for compression can typically range from 0% to 75%.

If, for example, a computer sends data via synchronous serial interface to a modem having a data rate of 4800 baud, the modem uses data compression to reduce the information to a transmission speed of 2400 baud and subsequently sends it without problems over a telephone line (see Figure 16). Variations in the compressibility of the signal are, in this case, buffered by a FIFO. If the transmitted data is not compressible, the data received from the interface line is temporarily stored by a FIFO in the modem. When the potential for data compression increases to over 50%, the modem again accepts data stored in the FIFO. Only if the compressibility of the transmitted data deviates significantly and for a long time from the average value (50%) must the arriving data stream be halted or the data stream that is leaving be interrupted.

The same speed variations arise with data expansion at the receiver as with compression at the transmitter. A FIFO also is used here to buffer the data and to ensure a constant flow of data to the receiver.

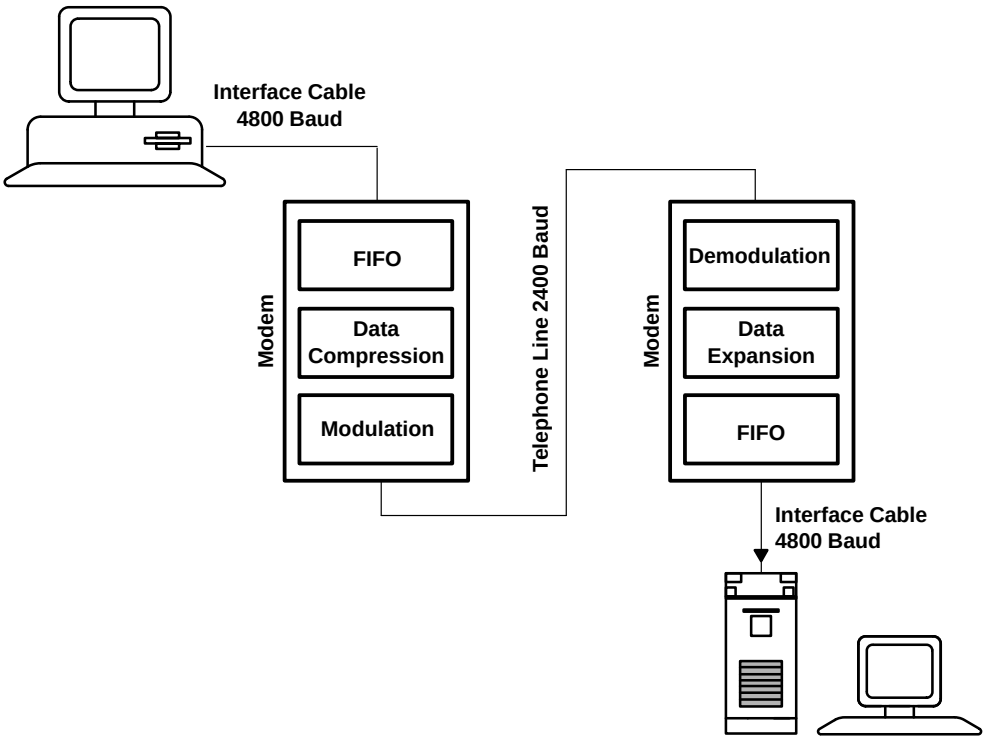


Figure 16. Data Transmission by Modem With Data Compression

Since in this application a serial stream needs to be buffered by the FIFO, the FIFOs having a word width of one bit shown in Table 7 are suitable. The two FIFOs needed for duplex operation (for transmitter and receiver) have already been integrated with these FIFO types into a single package.

Signal-Processor Interfaces

The signal processors from TI's TMS320CXX family have one or more serial ports to allow them to communicate with other signal processors or for data exchange with peripheral equipment such as the analog interface circuit (AIC). For data transmission, the signal processors make use of the following signals:

Transmit clock – clock transmit (CLKX)

Transmitter control – frame sync transmit (FSX)

Transmit data – data transmit (DX)

Receiver clock – clock receive (CLKR)

Receiver control – frame sync receive (FSR)

Receive data – data receive (DR)

The protocol for the transmission of data is shown in Figure 17. The fact that data is to be transmitted is signaled by FSX, which occurs on the falling edge of the clock pulse CLKX. To make the waveform of the signal processor in Figure 17 compatible with that required by the FIFO, both the clock signal CLKX and the control signal FSX must be programmed to give an inverted output. The TMS320C30 offers the possibility of programming both the polarity of the clock signal and the control signal. The resulting signals shown in Figure 18 are directly compatible with the FIFO.

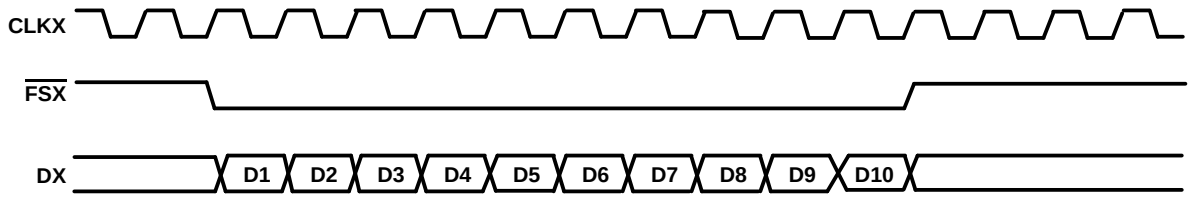


Figure 17. Serial-Port Data-Transmission Protocol of a TMS320CXX

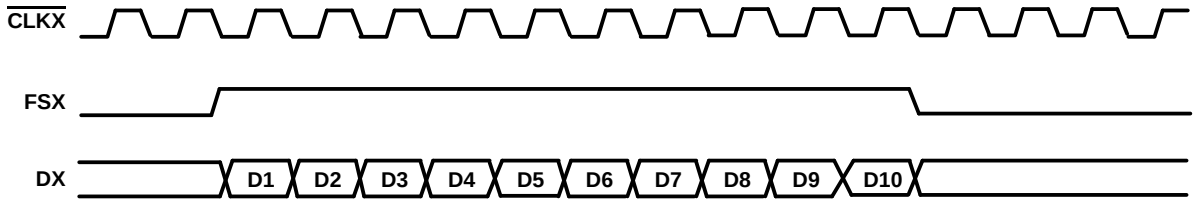


Figure 18. Serial-Port Data-Transmission Protocol With Inverted Signals

With data transmission via a serial port, both the transmitter and the receiver must normally be ready to operate simultaneously since the TMS320CXX has only a single word of internal buffer memory apart from the transmit and receive buffers. If a SN74ACT2229 FIFO is switched into the communication channel, both transmitter and receiver do not need to transfer data simultaneously. Each participant can complete the data transfer when time allows. The time that is saved is available for processing other jobs.

Figure 19 shows the connection of two TMS320C30 devices. The connection of an analog interface circuit (AIC) to a TMS320C30 is made similarly. Since two independent FIFOs are integrated into a single SN74ACT2229, full-duplex operation is possible with only one package.

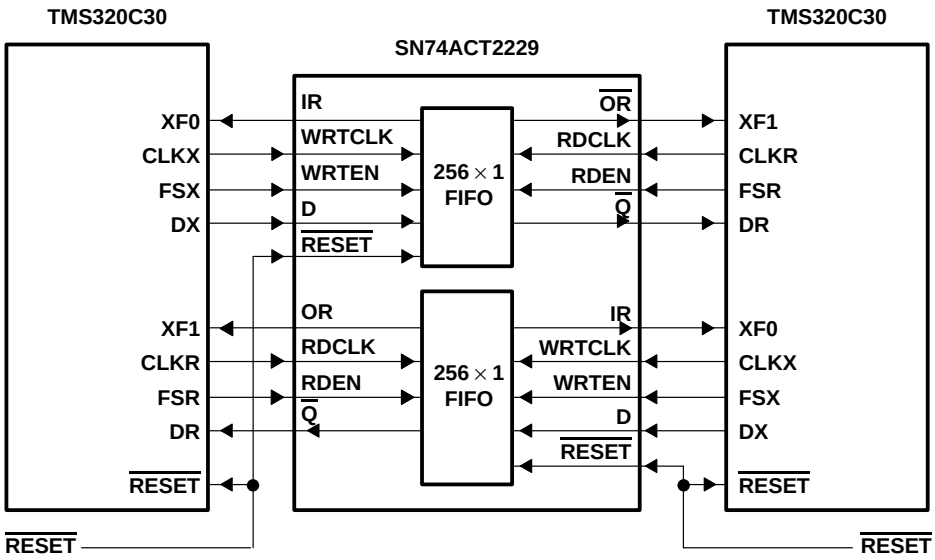


Figure 19. Connection of Two Signal Processors via a Serial Port With the Help of the FIFO SN74ACT2229

Teletext Decoders

With teletext, pages of text are transmitted as digital information in addition to the normal television signal. To be compatible with existing TV receivers, this digital information is transmitted in the picture-frequency blanking interval. The invisible picture lines, sent during beam flyback but after those for picture synchronization, contain the digital teletex data instead of picture information (see Figure 20). With D2-MAC, 360 bits with a bit rate of 20.25 Mbit/s are transmitted per TV line; therefore, the teletext information occupies 17.8 µs of the 64 µs for which the TV line lasts. In this example, a D2-MAC decoder extracts the digital teletext information from the television signal and conducts it to a 512 x 1 FIFO (see Figure 21). The D2-MAC decoder writes the data block by block at a rate of 20.25 Mbit/s into the FIFO. The teletext module is now able to read out and process the 360-bit digital information within 64 µs at a significantly slower rate of up to 5.625 Mbit/s. In this example, the FIFO undertakes the adjustment and synchronization of the two different rates.

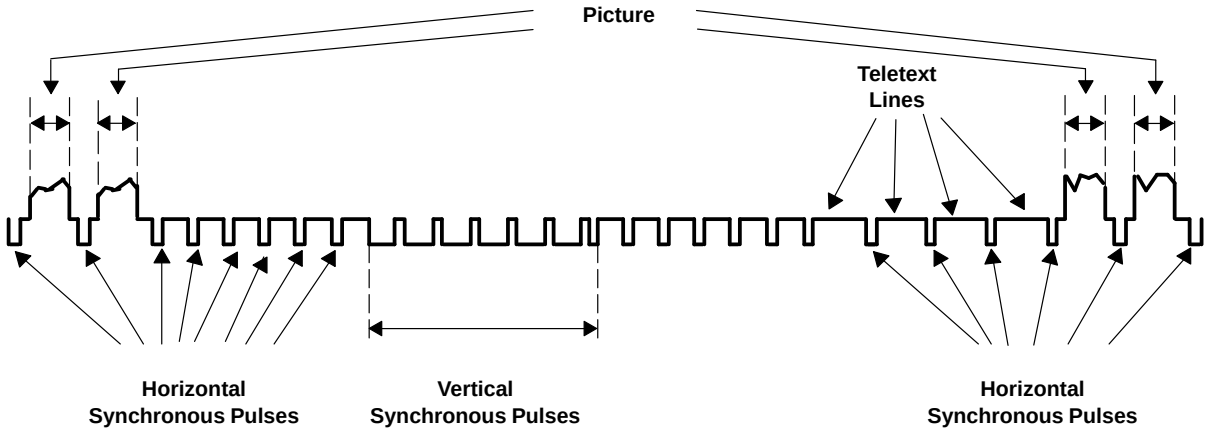


Figure 20. Video Signal

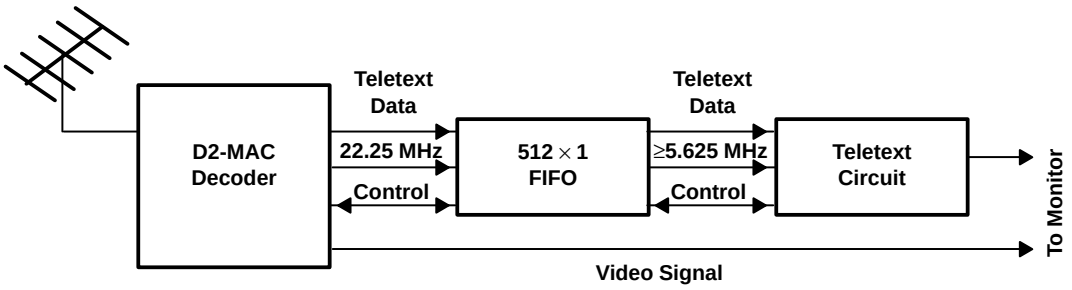


Figure 21. Teletext Decoder With 1 × 512 FIFO Block Diagram

The 512 × 1 FIFO of Figure 21 can be achieved by cascading the two 256 × 1 FIFOs of the circuit SN74ACT2228 or SN74ACT2229. Figure 22 shows how to cascade both SN74ACT2229 FIFOs to one 512 × FIFO.

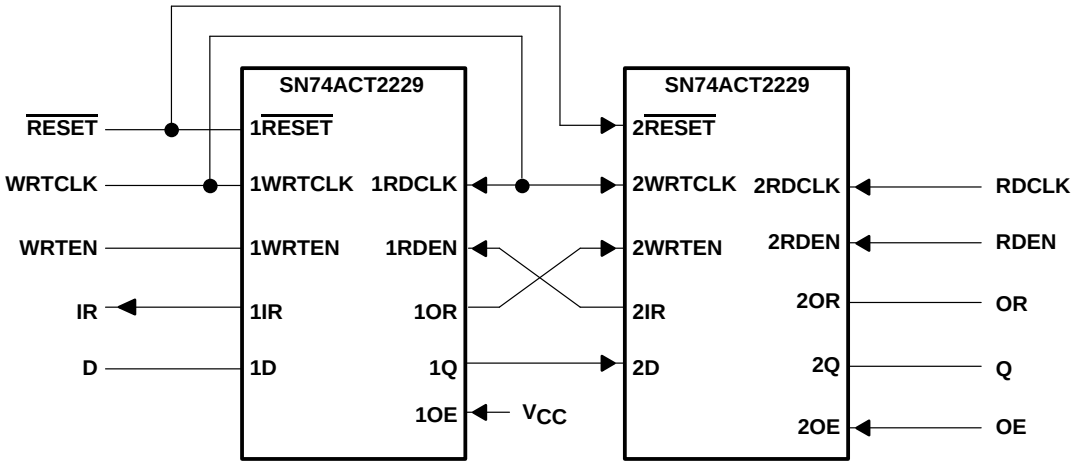


Figure 22. Extending Memory Depth of a SN74ACT2229 FIFO to 512 × 1 Bit

Summary

FIFOs offer the solution to problems in a wide variety of applications. Asynchronous FIFOs can be classified into two groups according to the control signals used for writing and reading: strobed FIFOs (Figure 2) and clocked FIFOs (Figure 3).

The decision of which of these types to use is dependent on the application. Since the status lines with strobed FIFOs cannot be fully synchronized, in case of doubt, a clocked FIFO is preferred. Only the clocked FIFO provides completely synchronized status lines.

FIFOs can be further classified according to their word width and memory capacity. The main application of the FIFOs having a word width of one bit is in telecommunications. However, many additional applications can be envisaged in a wide range of digital electronics. When serial data needs to be buffered and synchronized, these FIFOs are usually the logical and correct choice.