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Low cost DECT Power Amplifier PH97005

Preliminary Application Note
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Abstract

Application of new *5th generation* discrete bipolar RF transistors facilitates design of a low cost two-stage power amplifier for DECT systems, having a power gain of 26 dB and an overall efficiency better than 40%. The amplifier operates from a single supply voltage, includes bias circuitry for load power adjustment and on/off switching and is mounted on a bilayer pcb, requiring 10 x 20 mm. A description is given of the circuit design and the board layout, including measurement results.

INTRODUCTION

This note describes the application of two of the new *5th generation* silicon bipolar RF transistors in SOT343R plastic SMD package in a two-stage power amplifier (PA), designed for use in DECT cordless telephone systems. These transistors, manufactured according to the new *double-poly* process, are characterised by their high transition frequency (f_T > 20 GHz) at low supply voltages, resulting in a superior power gain at microwave frequencies, usually a field dedicated to GaAs-devices. Two layers of polysilicon are used: one for contacting the base, yielding a low base resistance and one to form the emitter, resulting in a steep emitter dope profile and an effective emitter width of 0.5 µm. A buried N-layer (collector) is placed within a P-substrate, which is connected to the emitter package lead, which enables the die to be placed on the ground plane, reducing emitter inductance and thermal resistance. Figure 1 shows a cross section of a *double-poly* buried layer transistor.

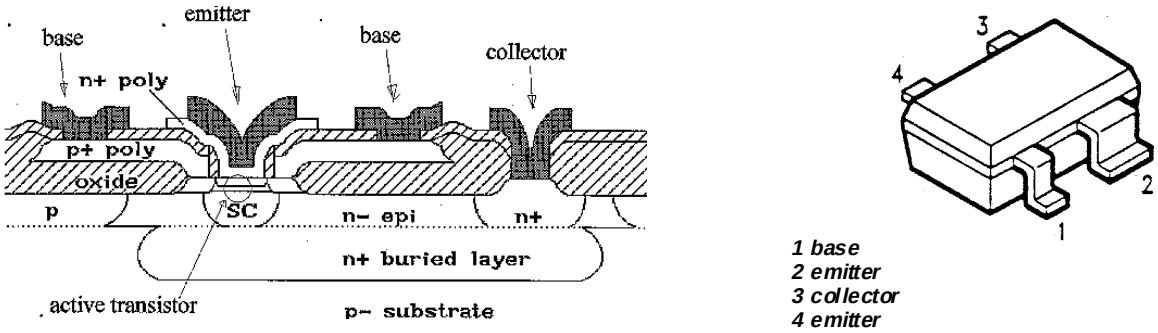

Figure 1: Cross section and package of the double-poly buried layer RF transistors.

With only two *double-poly* transistors a complete amplifier line-up can be realised, offering 26 dBm of output power with more than 26 dB power gain. The amplifier requires a single supply voltage of 3.6 V and typically has 44% efficiency. The biasing circuitry uses only one NPN transistor pair, which also performs load power adjustment and on/off switching functions. Thanks to the low component count and simple matching networks the entire amplifier (including bias part) only measures 10 x 20 mm.
As compared to a previous demonstration board, PH96060 (Preliminary Application Note RNR-T45-96-T-838) this one offers lower additional component count, but is less suitable for PHS application.

The main features of the PA are:

- low component count
- small size
- high efficiency
- single supply operation

CHARACTERISTICS

(unless otherwise specified the operating frequency is 1. 89 GHz, the supply voltage is 3.6 V, the input power is 0 dBm and the period is 10 ms with a duty cycle of 1:8)

Parameter	Specification	Typical	Condition
General parameters			
Supply voltage (Vs)	3.2 ≤ 3.6 ≤ 4.2 V		
Control voltage (Vc)	on state: 3.6 V off state: 0 V		
Frequency range	1.88 - 1.92 GHz		
Type of operation	pulsed		duty cycle ≤ 50%
Source and load impedance	50 Ω		
Power gain (G_p)	≥ 26 dB	26.3 dB	P_o = 26 dBm
Output power (P_o)	≥ 26 dBm	26.3 dBm	
Avg. supply current	11 mA		P_o = 26 dBm
Efficiency	≥ 40%	44%	P_o = 26 dBm
Input VSWR	2 :1		
Isolation (relative to input power)	≥ 50 dB	57 dB	Vc = 0 V
Spurious	≤ -60 dBc		V_s = 3.2..4.2 V VSWR 6 : 1, all phases
Leakage current in off-state	≤ 10 µA		Vc = 0 V
Harmonics: 2^{nd} 3^{rd}	≤ -30 dBm ≤ -30 dBm	-34 dBm -13 dBm	
Load mismatch:	No degradation		P_o = 26 dBm, V_s ≤ 4.5 V VSWR 6 : 1, all phases
Printed circuit board	FR4 bilayer (h=0.7; ε_r=4.6; tanδ=0.02)		
Dimensions	10 x 20 mm (including bias circuitry)		

Table 1: Characteristics of the DECT PA PH97005.

CIRCUIT DESCRIPTION

Figure 2 shows circuit diagram of the DECT PA including both RF transistors, matching circuits and biasing circuit. The appendix contains the part list of the demo board.

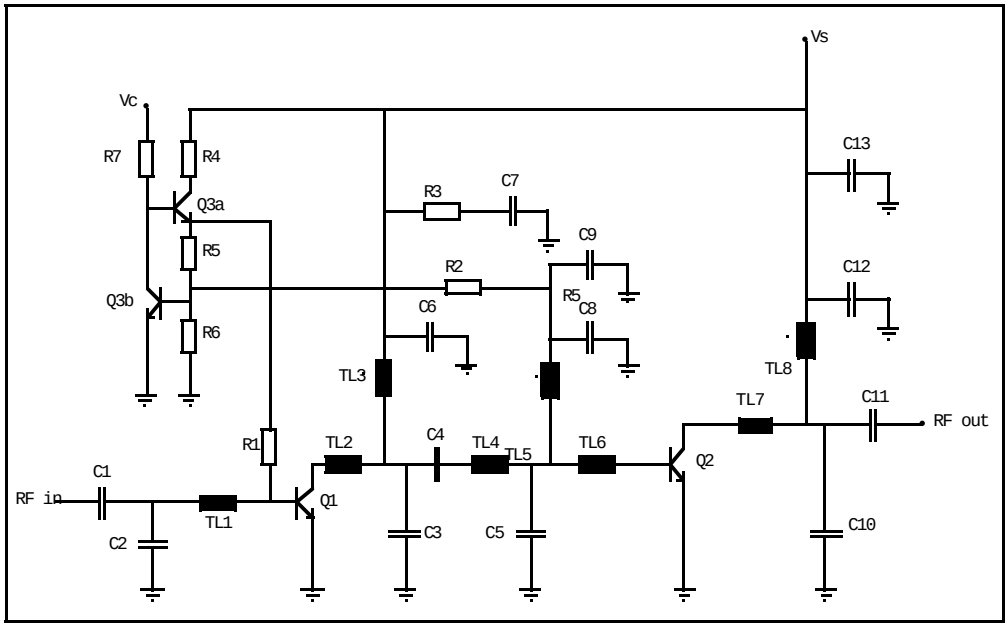

Figure 2: Circuit diagram of the DECT PA demo board PH97005.

RF transistors

The RF chain of the PA consists of two transistor stages: a BFG425W (Q1) wideband transistor, operating in class A and a BFG21W (Q2), operating in class AB.
In accordance with the above settings the measured source and load impedances of both transistors are given in table 2.

Transistor	Source impedance (Z_s)	Load impedance (Z_l)
BFG425W (V_{ce}=3.6 V; Ic=30 mA; f=1.89 GHz)	12 + 0.7 j Ω	52 + 102 jΩ
BFG21W (V_{ce}=3.6 V; P_o=26 dBm; f=1.89 GHz)	8 -4.5 j Ω	12 - 3.5 j Ω

Table 2 : Source and load impedances of the applied RF transistors.

Small signal S-parameter data for the BFG425W as well as large signal Spice parameters of both the BFG425W and the BFG21W are available on floppy disc.

The RF transistors have two emitters leads, which have to be carefully grounded to ensure stable operation and performance according to specification. Typically, the inductance of the vias has to be kept below 0.1 nH.

Impedance matching

The impedance matching part consists of three separate sections: the input, the interstage and the output matching networks. The purpose of these networks is to enable the RF transistors to give optimum performance with respect to power gain, output power and efficiency. Fortunately, the impedance levels of the applied *double-poly* transistors are not exceptionally high or low, so they're rather easy to match.
Decoupling is done by using capacitors C1, C4, C6, C8, C11 and C12, which are series resonant at 1.9 GHz. Capacitors C7 (with resistor R3) and C9 are used to suppress low frequency instability.

At the input side shunt capacitor C2 and series transmission line TL1 match the 50 Ω source to the base of Q1. Base resistor R1 is used for biasing and has no effect on matching.

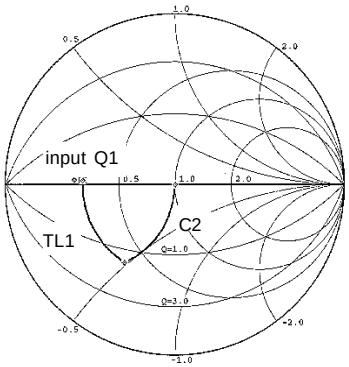

Fig. 3a: Input matching.

Between the collector of Q1 and the base of Q2 matching is done by series transmission line TL2, shunt capacitor C3 and series transmission lines TL4 and TL6. Both shunt capacitors C3 and C5 (partly) compensate the influence of bias stubs TL3 and TL5, which are both shorter than a quarter wavelength.

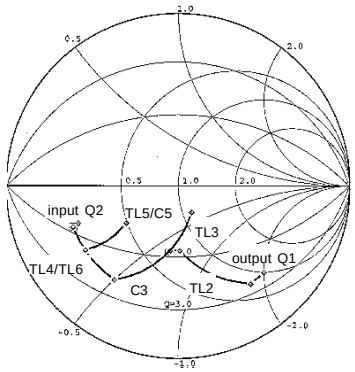

Fig. 3b: Interstage matching.

The output match is done by series transmission line TL7 and shunt capacitor C10. Again this capacitor also compensates the influence of bias stub TL6.

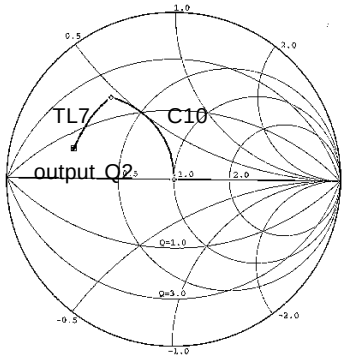

Fig. 3c: Output matching.

Biasing

The biasing part of the PA is centered around a dual NPN transistor, Q3 a and b. The circuit offers a temperature compensated bias voltage for both the first and the second RF stages. Unlike the previous demo board PH96060, the circuit is activated when Vc is high, which is beyond 2.4 V. The bias output voltage for the first stage is a little higher than for the second stage. Due to series resistor R1, the fist stage is current driven and operates in class A. The second stage is driven by at the knee voltage (0.7 V) and operates in class AB. Series resistor R2 protects Q2 from thermal runaway.

The current design of the PA doesn't include any measures to reduce adjacent channel power due to switching transients. The slope of the RF pulse can be too steep and has to be relaxed to comply to the approval specification. This can be done by placing a capacitor at the base of Q3a. Experimental investigation has shown that a 10 nF capacitor approximately offers a 20 dB improvement of the adjacent channel power.

Recommendations for use

Figure 4 shows how the PA should be connected.

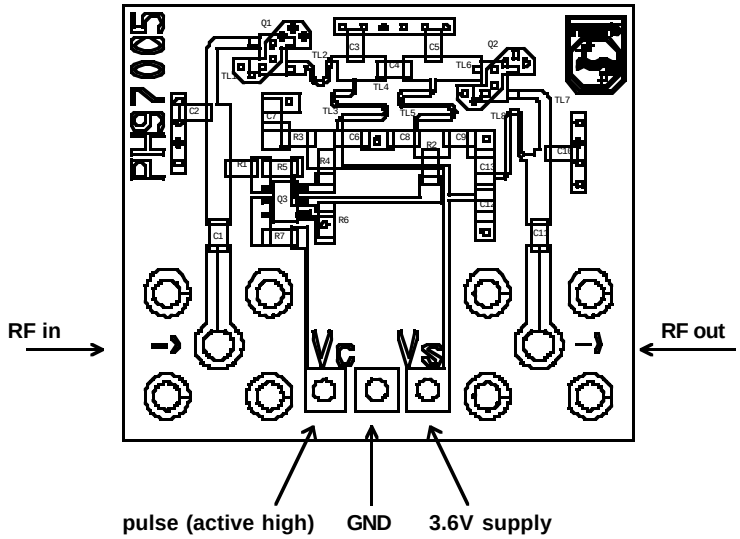

Figure 4: Schematic view of the PA connections.

In pulsed condition at nominal supply voltage and output power level, the load can be mismatched (VSWR ≤ 6 : 1, all phases) without damage.
The PA can also be operated in CW, but only when the output is properly matched with 50 Ω. When a mismatched load is applied when the amplifier is operated in CW, this will cause damage of the final stage.

BOARD LAYOUT

Figure 5 shows the layout of the PCB, which has the following properties:

type: FR4 bilayer (backside ground)
h = 0.71 mm
t = 35 µm (Cu cladding, not coated)
ε_r = 4.6
tanδ = 0.02

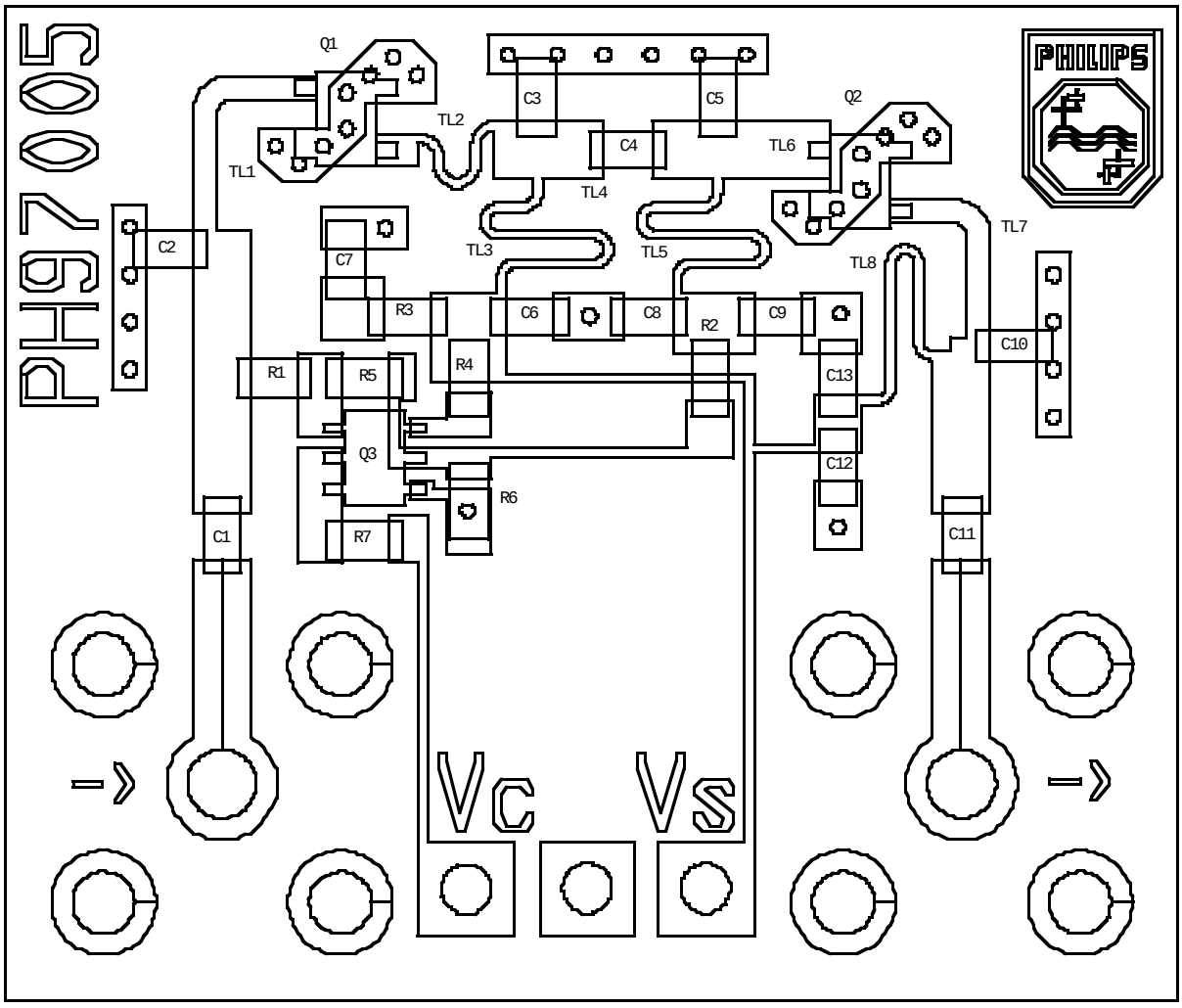

Figure 5: Layout of the DECT PA demo board.

All resistors and capacitors used are Philips 0603 SMD types. Appendix A contains the part list of the demo board. The position of components C2, C3, C5 and C10 is critical.
The artwork file is available on floppy disc (DXF format).

MEASUREMENT RESULTS

Measurements under pulsed conditions, with a 10 ms period and a duty cycle of 1:8.
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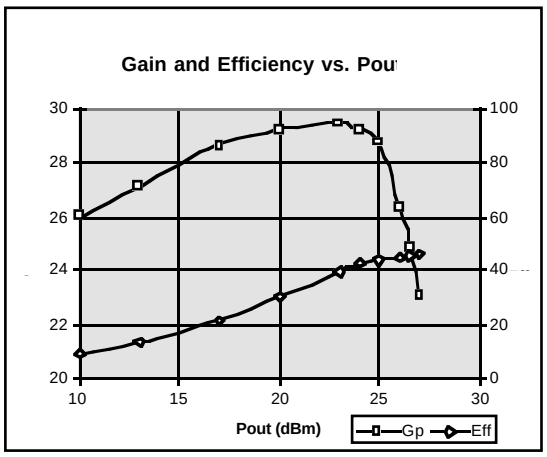

Figure 6a: f = 1.89 GHz; Vs = 3.6 V; V_c = 3.6 V.

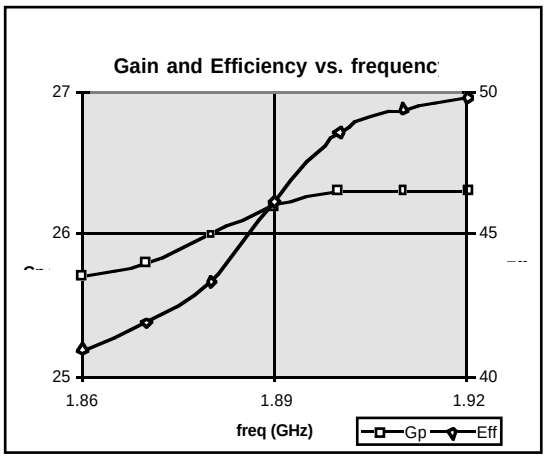

Figure 6b: Vs = 3.6 V; P_{in} = 0 dBm; V_c = 3.6 V.

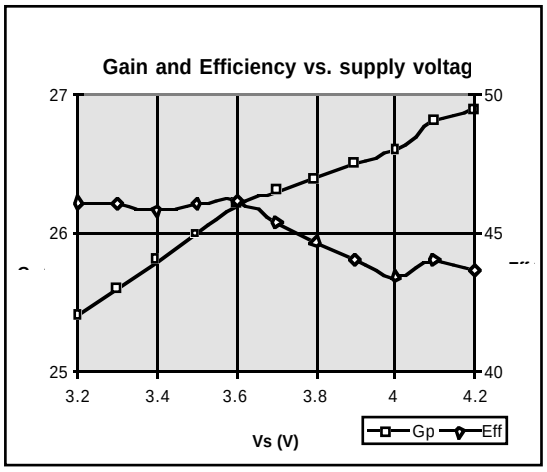

Figure 6c: f = 1.89 GHz; P_{in} = 0 dBm; V_c = 3.6 V.

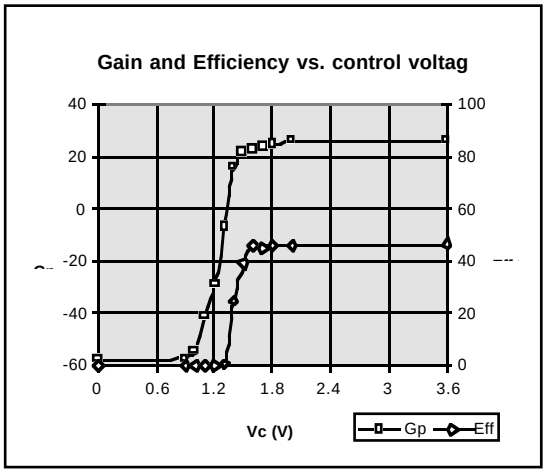

Figure 6d: f = 1.89 GHz; Vs = 3.6 V; P_{in} = 0 dBm.

APPENDIX

Part list DECT PA demo board PH97005

Resistors

R1	560
R2	56
R3	10
R4	220
R5	82
R6	330
R7	1 K

C1	8.2p
C2	1.8p
C3	1.8p
C4	8.2p
C5	3.3p
C6	8.2p
C7	10n
C8	8.2p
C9	1n
C10	2.7p
C11	8.2p
C12	8.2p
C13	1n

Transmission lines

TL1	L = 6.5 mm W = 0.45 mm
TL2	L = 3.0 mm W = 0.15 mm
TL3	L = 7.5 mm W = 0.15 mm
TL4	L = 2.0 mm W = 1.15 mm
TL5	L = 7.5 mm W = 0.15 mm
TL6	L = 2.0 mm W = 1.15 mm
TL7	L = 5.0 mm W = 0.45 mm
TL8	L = 6.5 mm W = 0.15 mm

Transistors

Q1	BFG425W
Q2	BFG21W
Q3	PUMX1

Capacitors