DATA SHEET

SAA7167A
YUV-to-RGB Digital-to-Analog Converter DAC

Preliminary specification
File under Integrated Circuits, IC22

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Philips Semiconductors

PHILIPS

YUV-to-RGB Digital-to-Analog Converter DAC

SAA7167A

FEATURES

- On-chip mixing of digital video data and analog RGB signals
- Supports video input format of YUV 4 : 2 : 2, 4 : 1 : 1, 2 : 1 : 1 andRGB 5 : 6 : 5
- Video input rate up to 66 MHz
- Allows for both binary and two's complement video input data
- Triple 8-bit DACs for video output
- Built-in voltage output amplifier
- Provide keying control with external key and internal 8-bit, 2×8-bit and 3×8-bit pixel colour key
- Programmable via the I^2C-bus
- 5 V CMOS device; LQFP48 package.

GENERAL DESCRIPTION

The SAA7167A is a mixed-mode designed IC containing a video data path, keying control block, analog mixer, and a voltage output amplifier, capable of converting digital video data to analog RGB video, and then mixing video and external analog RGB inputs.

The video data path contains a data re-formatter, YUV-to-RGB colour space matrix as well as triple DACs for video data processing. An analog mixer performs multiplexing between DAC outputs of the video path and external analog RGB inputs.

The final analog outputs are buffered with built-in voltage output amplifiers to provide the direct driving capability for a 150 Ω load. Figure 1 shows the overall block diagram.

The operation of SAA7167 is controlled via the I^2C-bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.75	5.25	V
V_{DDA}	analog supply voltage	4.75	5.25	V
T_{amb}	operating ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7167A	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

BLOCK DIAGRAM

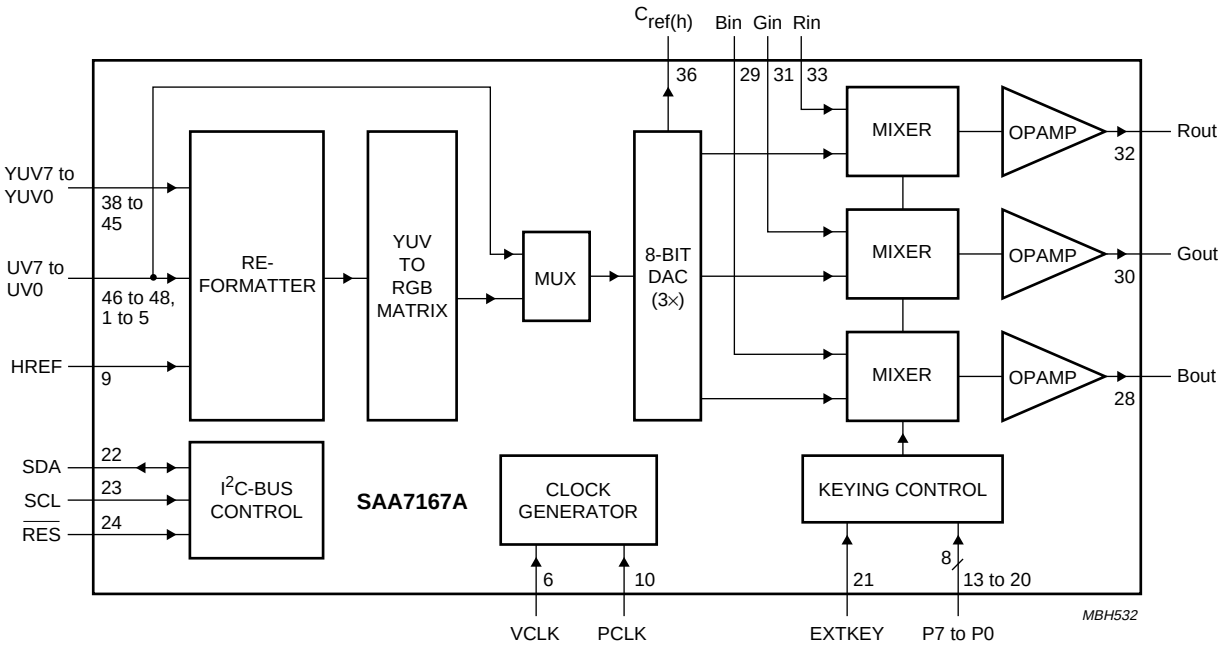


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	I/O
UV4	1	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV3	2	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV2	3	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV1	4	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV0	5	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
VCLK	6	video clock input	I
V_{DDD}	7	digital supply voltage	I/O
V_{SSD}	8	digital ground	I/O
HREF	9	horizontal reference input signal	I
PCLK	10	pixel clock input	I
AP	11	test pins, normally connected to ground	I
SP	12	test pins, normally connected to ground	I
P7	13	pixel bus input 7 (for keying control)	I
P6	14	pixel bus input 6 (for keying control)	I
P5	15	pixel bus input 5 (for keying control)	I
P4	16	pixel bus input 4 (for keying control)	I
P3	17	pixel bus input 3 (for keying control)	I
P2	18	pixel bus input 2 (for keying control)	I
P1	19	pixel bus input 1 (for keying control)	I
P0	20	pixel bus input 0 (for keying control)	I
EXTKEY	21	external key signal input	I
SDA	22	I^2C-bus data line	I/O
SCL	23	I^2C-bus clock line	I
$\overline{RES}$	24	set to LOW to reset the I^2C-bus	I
n.c.	25	not connected	–
V_{SSA2}	26	analog ground 2	I/O
V_{DDA2}	27	analog supply voltage 2	I/O
Bout	28	analog Blue signal output	O
Bin	29	analog Blue signal input	I
Gout	30	analog Green signal output	O
Gin	31	analog Green signal input	I
Rout	32	analog Red signal output	O
Rin	33	analog Red signal input	I
V_{SSA1}	34	analog ground 1	I/O
V_{DDA1}	35	analog supply voltage 1	I/O
$C_{ref(h)}$	36	capacitor for reference high voltage output (2.25 V)	I/O

SYMBOL	PIN	DESCRIPTION	I/O
n.c.	37	not connected	–
YUV7	38	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV6	39	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV5	40	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV4	41	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV3	42	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV2	43	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV1	44	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV0	45	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
UV7	46	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV6	47	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV5	48	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I

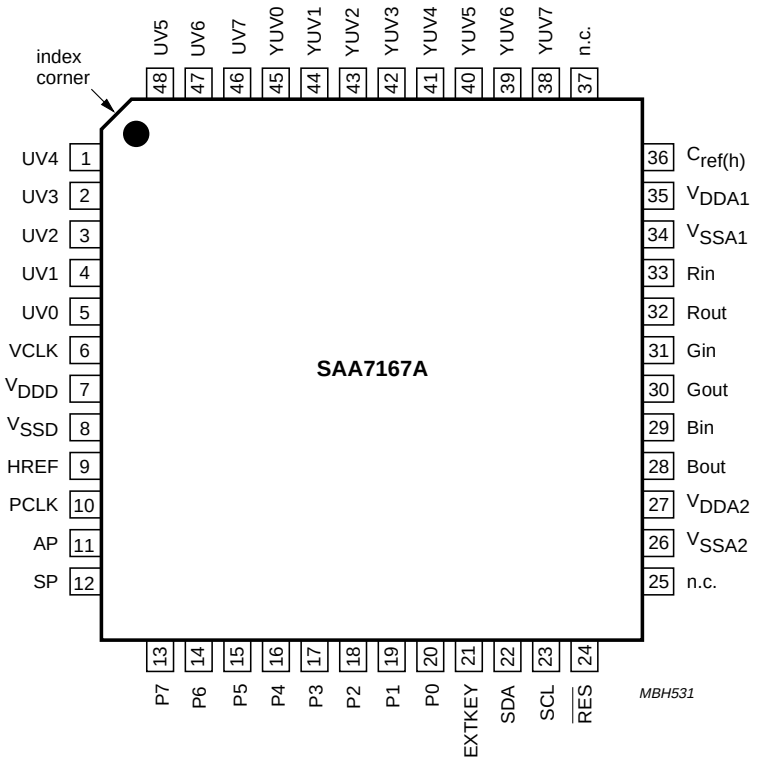


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA7167A contains a video data path, 3 analog mixers and voltage output amplifiers for the RGB channels respectively, a keying control block as well as an I^2C-bus control block.

Video data path

The video data path includes a video data re-formatter, a YUV-to-RGB colour space conversion matrix, and triple 8-bit DACs.

RE-FORMATTER

The re-formatter de-multiplexes the different video formats YUV 4 : 1 : 1, 4 : 2 : 2 or 2 : 1 : 1 to internal YUV 4 : 4 : 4, which can then be processed by the RGB matrix. The pixel byte sequences of those video input formats are shown in Tables 1 to 4.

Table 1 Pixel byte sequence of 4 : 2 : 2

INPUT	PIXEL BYTE SEQUENCE OF 4 : 2 : 2					
YUV0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y data	0	1	2	3	4	5
UV data	0		2		4	

Table 2 Pixel byte sequence of 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE OF 4 : 1 : 1							
YUV0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	X	X	X	X	X	X	X	X
UV1	X	X	X	X	X	X	X	X
UV2	X	X	X	X	X	X	X	X
UV3	X	X	X	X	X	X	X	X
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y data	0	1	2	3	4	5	6	7
UV data	0				4			

Table 3 Pixel byte sequence of 2 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE OF 2 : 1 : 1							
YUV0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
YUV1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
YUV2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
YUV3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
YUV4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
YUV5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
YUV6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
YUV7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y data	X	0	X	2	X	4	X	6
UV data	0	X	0	X	4	X	4	X

Table 4 Pixel byte sequence of 5 : 6 : 5

INPUT	PIXEL BYTE SEQUENCE OF RGB 5 : 6 : 5			
UV7	G0	G0	G0	G0
UV6	R4	R4	R4	R4
UV5	R3	R3	R3	R3
UV4	R2	R2	R2	R2
UV3	R1	R1	R1	R1
UV2	R0	R0	R0	R0
UV1	G5	G5	G5	G5
UV0	G4	G4	G4	G4
YUV7	G3	G3	G3	G3
YUV6	G2	G2	G2	G2
YUV5	G1	G1	G1	G1
YUV4	B4	B4	B4	B4
YUV3	B3	B3	B3	B3
YUV2	B2	B2	B2	B2
YUV1	B1	B1	B1	B1
YUV0	B0	B0	B0	B0
RGB data	0	1	2	3

For RGB 5 : 6 : 5 video inputs, the video data are just directly bypassed to triple DACs.

The input video data can be selected to either two's complement (I^2C-bus DRP-bit = 0) or binary offset (DRP-bit = 1). The video input format is selected by I^2C-bus bits FMTC1 and FMTC0.

The rising edge of HREF input defines the start of active video data. When HREF is inactive, the video output will be blanked.

YUV-TO-RGB MATRIX

The matrix converts YUV data, in accordance with CCIR-601, to RGB data with approximately 1.5 LSB deviation to the theoretical values for 8-bit resolution.

TRIPLE 8-BIT DACS

Three identical DACs for R, G and B video outputs are designed with voltage-drive architecture to provide high-speed operation of up to 66 MHz conversion data rate. A $C_{ref(h)}$ pin is provided to allow for one external de-coupling capacitor to be connected between the internal reference voltage source and ground.

Analog mixers and keying control

The analog mixers are controlled to switch between the outputs from the video DACs and analog RGB inputs by a keying signal. The analog RGB inputs need to interface with analog mixers in the way of DC-coupling, also these RGB inputs are limited to RGB signals without a sync level pedestal. The keying control can be enabled by setting I^2C bit KEN = 1. Two kinds of keying are possible to generate: one is external key (from EXTKEY pin when KMOD2 to KMOD0 are logic 0), and the other is the internal pixel colour key (when KMOD2 to KMOD0 are not logic 0) generated by comparing the input pixel data with the internal I^2C-bus register value KD7 to KD0. Controlled by KMOD2 to KMOD0 bits, there are 4 ways to compare the pixel data (see Table 5).

Table 5 KMOD2 to KMOD0

KMOD2 to KMOD0	PIXEL TYPE	REMARK
1 0 0	8-bit pixel	pseudo colour mode
1 0 1	2 × 8-bit pixel	high colour mode 1 with pixels given at both rising and falling edges of PCLK
1 1 0	2 × 8-bit pixel	high colour mode 2 with pixels given only at rising edges of PCLK
1 1 1	3 × 8-bit pixel	true colour mode

Since only one control register KD7 to KD0 provides the data value for pixel data comparison, when at 2 × 8-bit or 3 × 8-bit pixel input modes, it is presumed that all input bytes (lower, middle, or higher) of each pixel must be same as KD7 to KD0 in order to make graphics colour key active.

The polarity of EXTKEY can be selected with KINV. With KINV = 0, EXTKEY = HIGH switches analog mixers to select DAC outputs. Before the internal keying signal switches the analog multiplexers, it can be further delayed up to 7 PCLK cycles with the control bits KDLY2 to KDLY0.

Voltage output amplifiers

Before the analog input enters the analog mixers, it passes through voltage output amplifiers. Level shifters are used internally to provide an offset of 0.2 V and an amplifier gain of 2 for analog inputs to match with the output levels from DACs. After buffering with voltage output amplifiers, the final RGB outputs can drive a 150 Ω load directly (25 Ω internal resistor, 50 Ω external serial resistor, and 75 Ω load resistor at monitor side (see Fig.9).

The output voltage level of DAC ranges from the lowest level 0.2 V (zero code) to the highest level 1.82 V (all one code).

With the digital input YUV video data in accordance with CCIR-601, the RGB output of 8-bit DAC actually ranges from the 16th step (black) to the 235th step (white). Therefore, after the voltage divider with external serial resistor and monitor load resistor, the output voltage range to monitor is approximately 0.7 V (peak-to-peak).

I²C-bus control

Only one control byte is needed for the SAA7167A.
The I²C-bus format is shown in Table 6.

Table 6 I²C-bus format; see notes 1 to 7

S	slave address	A	subaddress	A	data	A	P

Notes

1. S = START condition.
2. Slave address = 1011 111X; this slave address is identical to the one for the SAA9065.
3. A = acknowledge; generated by the slave.
4. Subaddress = subaddress byte.
5. Data = data byte.
6. P = STOP condition.
7. X = R/$\overline{W}$ control bit:
   a) X = 0; order to write.
   b) X = 1; order to read (not used for SAA7167A).

Table 7 Control data byte

SUBADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00	KMOD2	KMOD1	KMOD0	DRP	KEN	KINV	FMTC1	FMTC0
01	0	0	0	0	0	KDLY2	KDLY1	KDLY0
02	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

Table 8 Bit functions in data byte; notes 1 and 2

BIT	DESCRIPTION
FMTC1 and FMTC0	video format control: 00; YUV 4 : 2 : 2 01; YUV 4 : 1 : 1 10; YUV 2 : 1 : 1/CCIR-656 11; RGB 5 : 6 : 5
KINV	key polarity: KINV = 0: EXTKEY = HIGH for analog mixer to select DAC outputs KINV = 1: EXTKEY = HIGH for analog mixer to select analog RGB inputs
KEN	key enable: 0 = disable 1 = enable
DRP	UV input data code: 0 = two's complement; 1 = binary offset
KMOD2 to KMOD0	keying mode: 000; external key 100; 8-bit pixel colour key 101; 2 × 8-bit pixel colour key (with two-edge clock latching for pixel input) 110; 2 × 8-bit pixel colour key (with one-edge clock latching for pixel input) 111; 3 × 8-bit pixel colour key (with one-edge clock latching for pixel input) all other combinations are reserved
KDLY2 to KDLY0	added keying delay cycles (from 0 to 7 PCLK)
KD7 to KD0	the data value compared for 8, 16 or 24-bit pixel colour key

Notes

1. All I^2C-bus control bits are initialized to logic 0 after $\overline{RES}$ is activated.
2. PCLK should be active in any event to allow for correct operation of I^2C-bus programming.

DC CHARACTERISTICS

T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.75	5.0	5.25	V
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
I_{DDtot}	total supply current (f_{clk} = 66 MHz)	–	105	–	mA
V_{IH}	HIGH level input voltage (pin SDA)	3	–	V_{DDD} + 0.5	V
V_{IL}	LOW level input voltage (pin SDA)	–0.5	–	+1.5	V
V_{IH}	HIGH level digital input voltage	2	–	–	V
V_{IL}	LOW level digital input voltage	–	–	0.8	V
V_{in}	full-scale analog RGB inputs	–	0.7	–	V
V_{out}	full scale analog RGB outputs (for 150 Ω load)	–	1.4	–	V
DNL	differential non-linearity error of video output	–	–	1	LSB
INL	integral non-linearity error of video output	–	–	1	LSB

AC CHARACTERISTICS

T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCLK					
f_{clk}	video clock rate	–	–	66	MHz
δ	duty factor of VCLK	40	50	60	%
PCLK					
f_{clk}	pixel clock rate				
	8-bit pixel colour key; see Fig.4	–	–	77.5	MHz
	2 × 8-bit pixel colour key; mode 1; see Fig.5	–	–	50	MHz
	2 × 8-bit pixel colour key; mode 2; see Fig.6	–	–	80	MHz
	3 × 8-bit pixel colour key; see Fig.7	–	–	77.5	MHz
δ	duty factor of PCLK	40	50	60	%
t_{su1}	digital input set-up time to VCLK rising edge	3	–	–	ns
t_{h1}	digital input hold time to VCLK rising edge	2	–	–	ns
t_{su2}	digital input set-up time to PCLK rising edge	0	–	–	ns
t_{h2}	digital input hold time to PCLK rising edge	4.2	–	–	ns
t_{su3}	digital input set-up time to PCLK falling edge	–1	–	–	ns
t_{h3}	digital input hold time to PCLK falling edge	6	–	–	ns
t_{sw}	switching time between video DAC/analog inputs; note 1	–	–	15	ns
T_{group}	overall group delay from digital video inputs to analog outputs (see Fig.8):				
	YUV video input mode	–	$20T_{VCLK} + t_{PD}$	–	ns
	RGB video input mode	–	$12T_{VCLK} + t_{PD}$	–	ns
t_r	DAC analog output rise time (see Fig.8); note 2	–	3.5	–	ns
t_f	DAC analog output fall time (see Fig.8); note 2	–	3.5	–	ns
t_s	DAC analog output settling time (see Fig.8); note 3	–	16.5	–	ns
t_{PD}	DAC analog output propagation delay (see Fig.8); note 4	–	20	–	ns
Analog outputs from analog inputs					
G_v	voltage gain	–	2.0	–	
B	bandwidth (–3 dB)	160	–	–	MHz
SR	slew rate	100	110	–	V/µs

Notes

1. Switching time measured from the 50% point of the EXTKEY transition edge to the 50% point of the selected analog output transition.
2. DAC output rise/fall time measured between the 10% and 90% points of full scale transition.
3. DAC settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.
4. DAC analog output propagation delay measured from the 50% point of the rising edge of VCLK to the 50% point of full-scale transition.

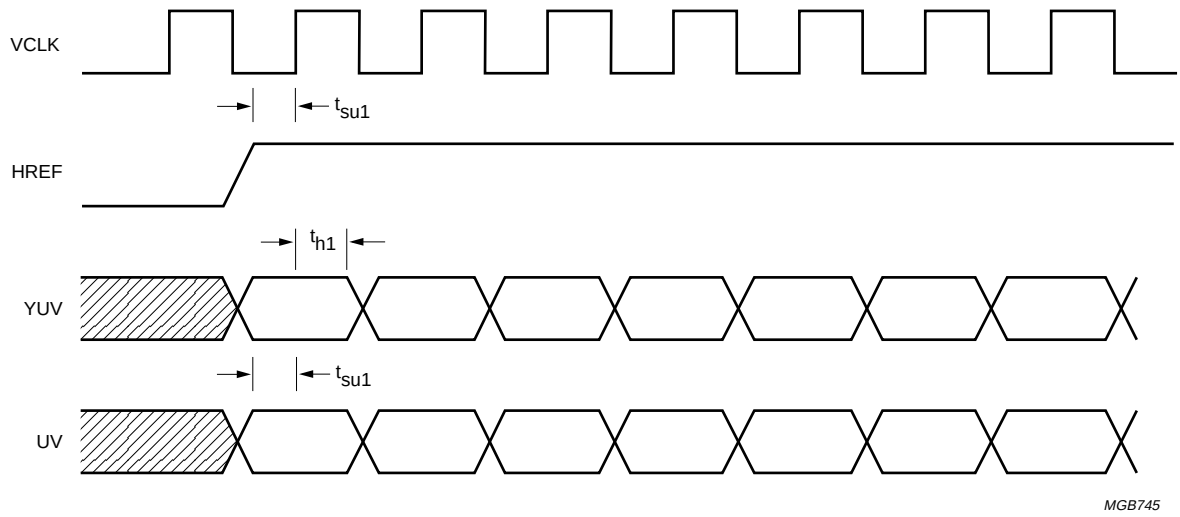


Fig.3 Video data input timing.

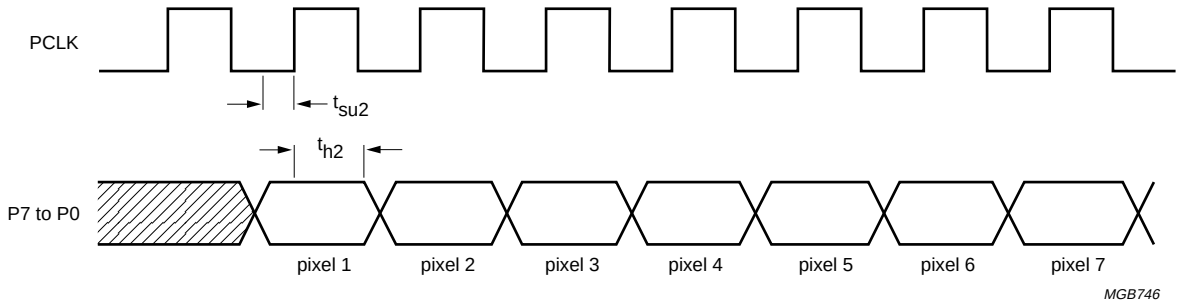


Fig.4 Pixel data timing; 8-bit pixel colour key.

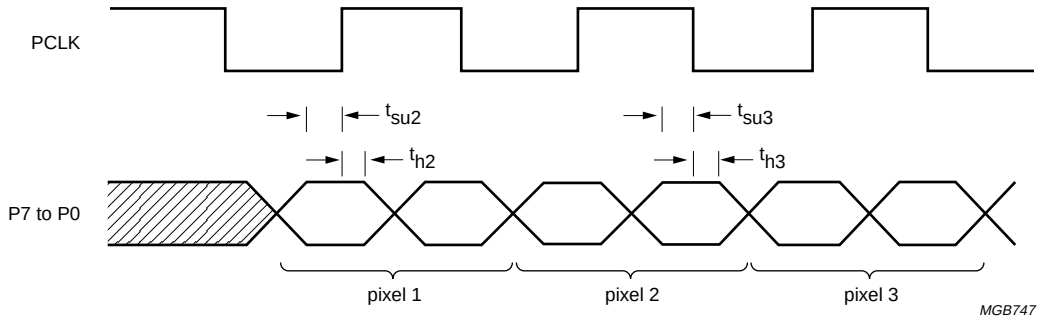


Fig.5 Pixel data input timing; 2×8-bit pixel colour key; mode 1.

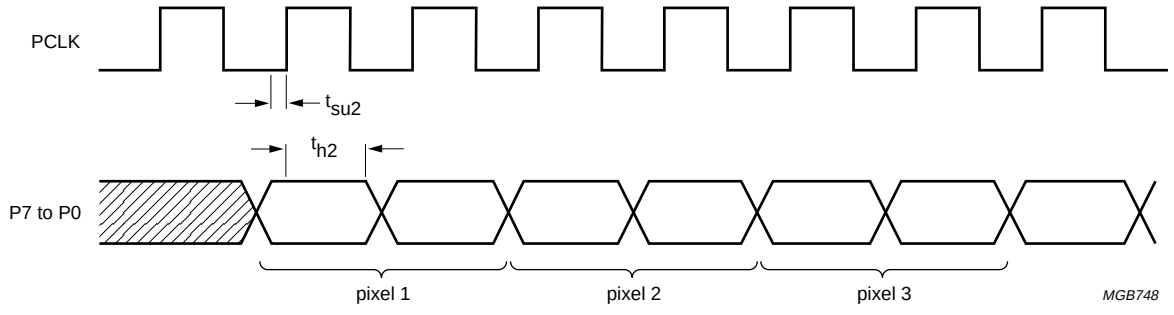


Fig.6 Pixel data input timing; 2×8-bit pixel colour key; mode 2.

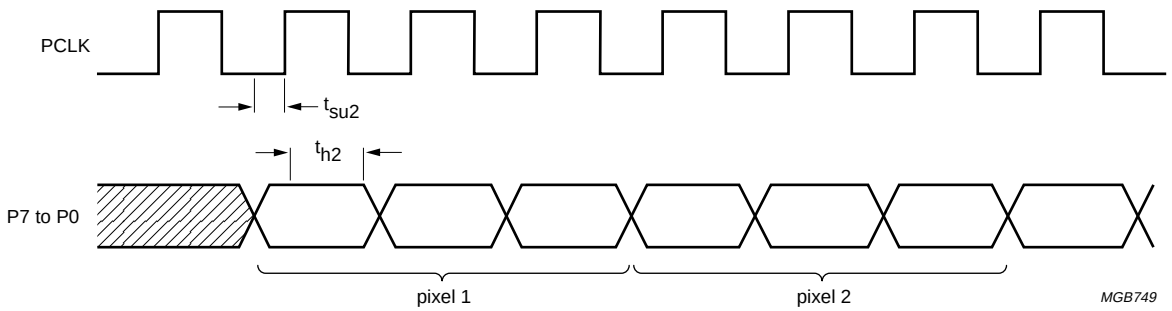


Fig.7 Pixel data input timing; 3×8-bit pixel colour key.

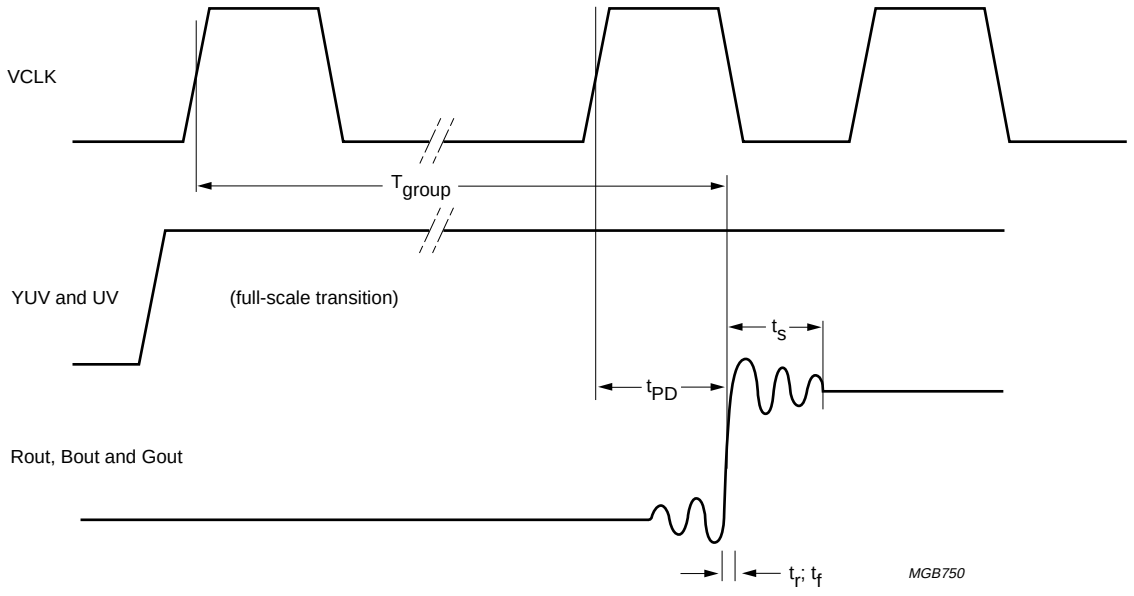


Fig.8 DAC output timing.

APPLICATION INFORMATION

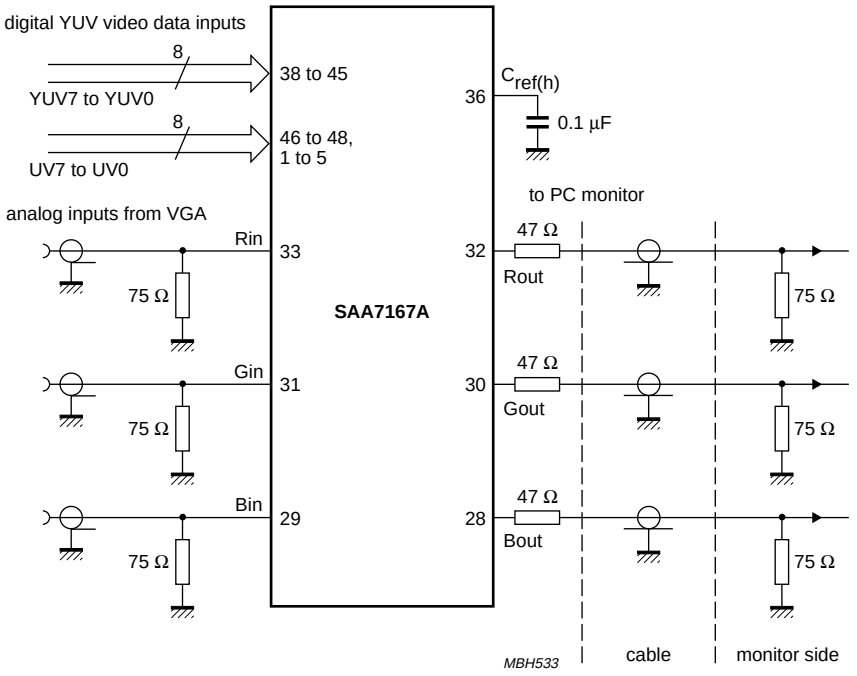
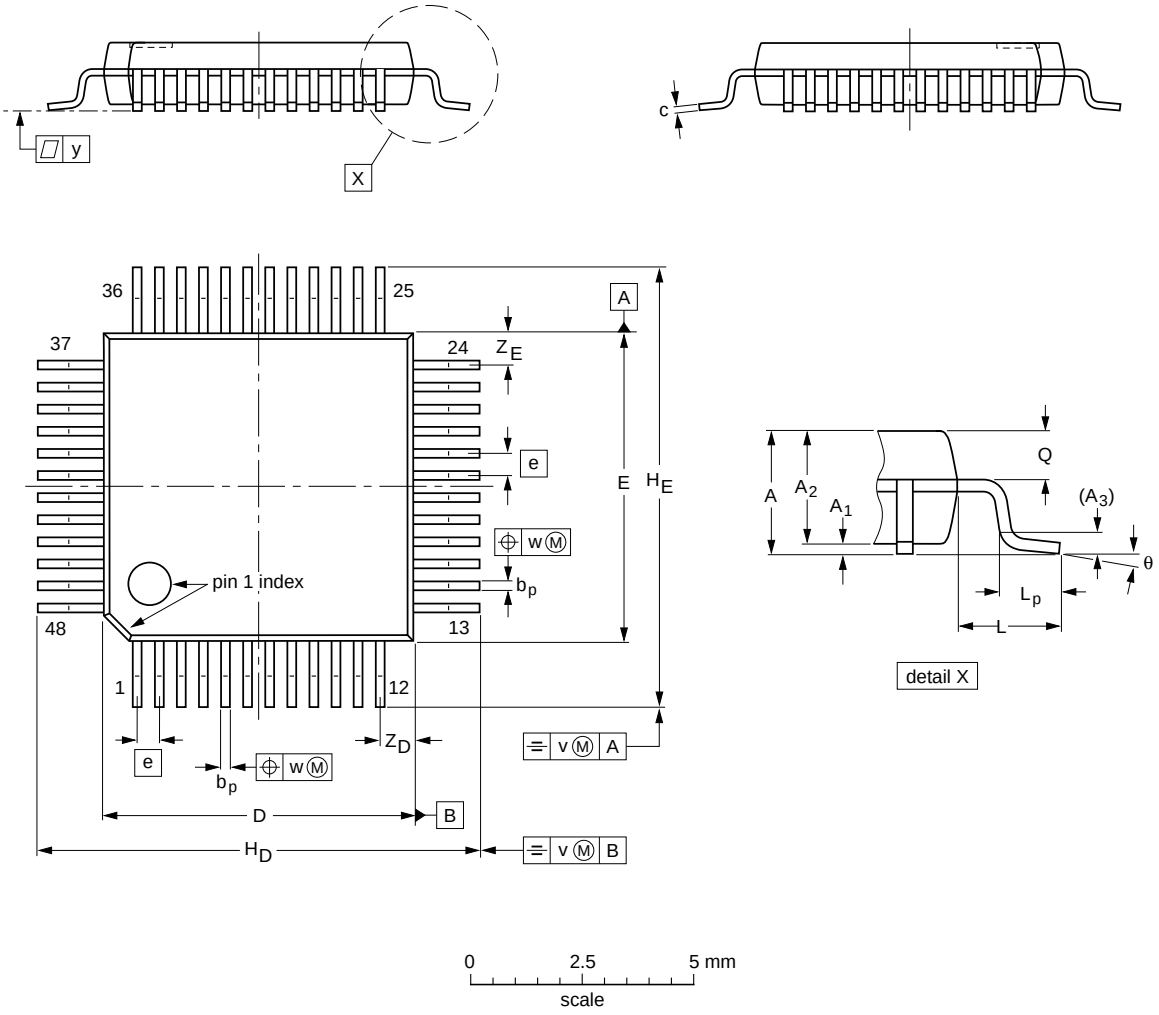


Fig.9 Typical application diagram for analog circuits.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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