

DATA SHEET

SAA6581T RDS/RBDS demodulator

Product specification
Supersedes data of 2001 May 07
File under Integrated Circuits, IC01

2002 Jan 14

RDS/RBDS demodulator**SAA6581T****FEATURES**

- Integrated switched capacitor filter
- Demodulates European Radio Data System (RDS) or the USA Radio Broadcast Data System (RBDS) signals
- Oscillator frequencies: 4.332 or 8.664 MHz
- Integrated ARI clamping
- CMOS device
- Single supply voltage: 5 V
- Extended temperature range: -40 to $+85$ °C
- Low number of external components.

APPLICATIONS

The RDS/RBDS system offers a large range of applications from the many functions that can be implemented. For car radios the most important are:

- Program Service (PS) name
- Traffic Program (TP) identification
- Traffic Announcement (TA) signal
- Alternative Frequency (AF) list
- Program Identification (PI)
- Enhanced Other Networks (EON) information.

GENERAL DESCRIPTION

The RDS/RBDS demodulator is a CMOS device with integrated filtering and demodulating of RDS/RBDS signals coming from a multiplexed input data stream. Data signal RDDA and clock signal RDCL are provided as outputs for further processing by a suitable microcomputer, for example CCR921 and CCR922.

The SAA6581T replaces SAA6579 in function and pin-compatibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.0	5.0	5.5	V
V_{DDD}	digital supply voltage	4.0	5.0	5.5	V
$I_{DD(tot)}$	total supply current	–	6.0	–	mA
$V_{i(MPX)}$	RDS input sensitivity at pin MPX	1	–	–	mV
$f_{i(xtal)}$	crystal input frequency	–	4.332	–	MHz
		–	8.664	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6581T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

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BLOCK DIAGRAM

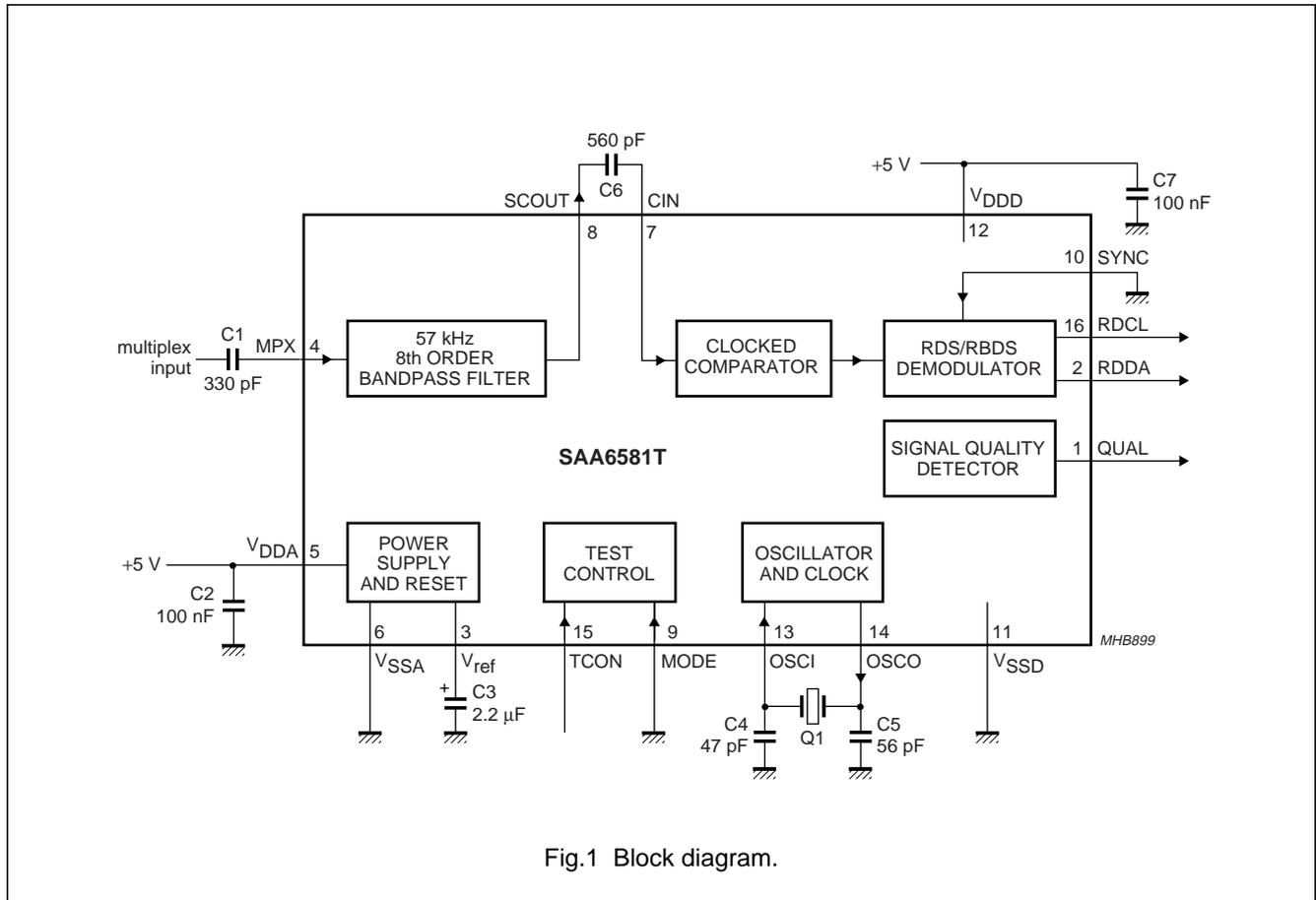


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
QUAL	1	signal quality indication output
RDDA	2	RDS data output
V _{ref}	3	reference voltage output (1/2V _D DA)
MPX	4	multiplex signal input
V _D DA	5	analog supply voltage (5 V)
V _{SS} A	6	analog ground (0 V)
CIN	7	comparator input
SCOUT	8	switched capacitor filter output
MODE	9	oscillator frequency select input
SYNC	10	ARI clamping control input
V _{SS} D	11	digital ground (0 V)
V _D DD	12	digital supply voltage (5 V)
OSCI	13	oscillator input
OSCO	14	oscillator output
TCON	15	test control input
RDCL	16	RDS clock output

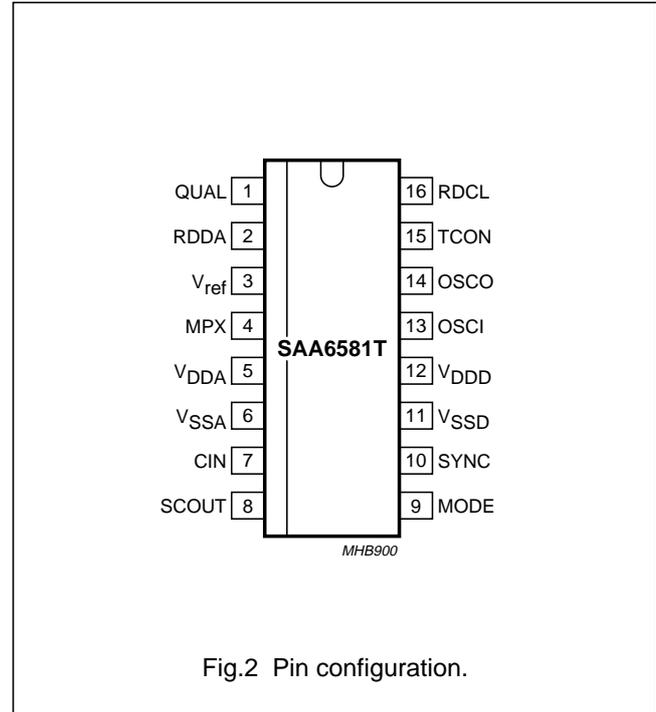


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

RDS/RBDS signal demodulation

BANDPASS FILTER

The bandpass filter has a centre frequency of 57 kHz. It selects the RDS/RBDS sub-band from the multiplex signal MPX and suppresses the audio signal components. The filter block contains an analog anti-aliasing filter at the input followed by an 8th order switched capacitor bandpass filter and a reconstruction filter at the output.

CLOCKED COMPARATOR

The comparator digitizes the output signal from the 57 kHz bandpass filter for further processing by the digital RDS/RBDS demodulator. To attain high sensitivity and to avoid phase distortion, the comparator input stage has automatic offset compensation.

DEMODULATOR

The demodulator provides all functions of the SAA6579 and improves performance under weak signal conditions.

Demodulator functions include:

- 57 kHz carrier regeneration from the two sidebands (Costas loop)
- Symbol integration over one RDS clock period
- Bi-phase symbol decoding
- Differential decoding
- Synchronization of RDS/RBDS output data.

The RDS/RBDS demodulator recovers and regenerates the continuously transmitted RDS/RBDS data stream in the MPX signal and provides clock RDCL for the output signals and data output RDDA for further processing by an RDS/RBDS decoder, for example CCR921 or CCR922.

ARI CLAMP

The demodulator checks the input signal for presence of RDS only, or RDS plus ARI transmissions. After a fixed test period, if the SYNC input is set HIGH the demodulator locks in the 'verified' condition (see Table 1). If SYNC is set LOW, the ARI clamping is reset (disabled). After SYNC returns to HIGH, the demodulator resumes checking the input signal.

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Table 1 Control pin SYNC

SYNC	ARI CLAMPING
LOW	internal ARI clamping disabled
HIGH	ARI clamping allowed to be logged

SIGNAL QUALITY DETECTION

Output QUAL indicates the safety of the regenerated RDS data (HIGH = 'good' data; LOW = 'unsafe' data).

Oscillator and system clock generator

For good performance of the bandpass and demodulator stages, the demodulator requires a crystal oscillator with a frequency of 4.332 or 8.664 MHz. The demodulator can operate with either frequency (see Table 2), so that a radio set with a microcontroller can run, in this case, with one crystal only. The demodulator oscillator can drive the microcontroller, or vice versa.

Table 2 Control pins TCON and MODE

TCON	MODE	OSCILLATOR FREQUENCY
HIGH	LOW	4.332 MHz
HIGH	HIGH	8.664 MHz

The clock generator generates the internal 4.332 MHz system clock and timing signal derivatives.

Power supply and internal reset

The demodulator has separate power supply inputs for the digital and analog parts of the device. For the analog functions an additional reference voltage ($\frac{1}{2}V_{DDA}$) is internally generated and available via the output pin V_{ref} . The demodulator requires a defined reset condition. The demodulator generates automatically a reset signal after the power supply V_{DDA} is switched on, or at a voltage-drop.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	6.5	V
V_n	voltage at pins 1 to 4, 7 to 10, and 13 to 16 with respect to pins 6 and 11	pins 5 and 12 are connected to V_{DD}	-0.5	$V_{DD} + 0.5 \leq 6.5$	V
$V_{i(MPX)(p-p)}$	input voltage at pin MPX (peak-to-peak value)	note 1	-	6	V
I_i	input current at pins 1 to 5, 7 to 11 and 13 to 16	pins 6 and 11 are connected to ground	-10	+10	mA
$I_{lu(prot)}$	latch-up protection current in pulsed mode	$T_{amb} = -40$ to $+85$ °C with voltage limiting -2 to +10 V	-100	+100	mA
		$T_{amb} = 25$ °C with voltage limiting -2 to +12 V	-200	+200	mA
		$T_{amb} = -40$ to $+85$ °C without voltage limiting	-10	+10	mA
T_{amb}	ambient temperature		-40	+85	°C
T_{stg}	storage temperature		-65	+150	°C
V_{es}	electrostatic handling voltage	note 2	-4000	+4000	V
		note 3	-500	+500	V

Notes

1. Without latching in the entire temperature range.
2. Human body model (equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor).
3. Machine model (equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor and 0.75 μ H inductance).

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	104	K/W

CHARACTERISTICS: DIGITAL PART

$V_{DDA} = V_{DDD} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.0	5.0	5.5	V
I_{DDD}	digital supply current		–	1.5	–	mA
P_{tot}	total power dissipation		–	30	–	mW
Inputs						
V_{IL}	LOW-level input voltage at pins TCON, OSCI, SYNC and MODE		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage at pins TCON, OSCI, SYNC and MODE		$0.7V_{DDD}$	–	–	V
$I_{i(pu)}$	input pull-up current at pins TCON and MODE	$V_{IH} = 3.5\text{ V}$	–10	–20	–	μA
Outputs						
V_{OL}	LOW-level output voltage at pins QUAL, RDDA and RDCL	$I_{OL} = 2\text{ mA}$	–	–	0.4	V
V_{OH}	HIGH-level output voltage at pins QUAL, RDDA and RDCL	$I_{OH} = -0.02\text{ mA}$	4.0	–	–	V
Crystal parameters						
$f_{i(xtal)}$	crystal input frequency	TCON = HIGH; MODE = LOW	–	4.332	–	MHz
		TCON = HIGH; MODE = HIGH	–	8.664	–	MHz
$ \Delta f_{osc} $	adjustment tolerance of oscillator frequency		–	–	30×10^{-6}	
$ \Delta f_{osc(T)} $	temperature drift of oscillator frequency	$T_{amb} = -40\text{ to }+85\text{ °C}$	–	–	30×10^{-6}	
C_L	load capacitance		–	30	–	pF
R_{xtal}	crystal resonance resistance		–	–	120	Ω

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CHARACTERISTICS: ANALOG PART

$V_{DDA} = V_{DDD} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.0	5.0	5.5	V
$ V_{DDA} - V_{DDD} $	difference between analog and digital supply voltages		–	0	0.5	V
$I_{DD(tot)}$	total supply current		–	6.0	–	mA
V_{ref}	reference voltage	$V_{DDA} = 5\text{ V}$	2.25	2.5	2.75	V
$Z_{o(Vref)}$	output impedance at pin V_{ref}		–	25	–	k Ω
MPX input (signal before the capacitor on pin MPX)						
$V_{i(MPX)(rms)}$	RDS amplitude (RMS value)	$\Delta f = \pm 1.2\text{ kHz}$ RDS-signal; $\Delta f = \pm 3.2\text{ kHz}$ ARI-signal	1	–	–	mV
$V_{i(max)(p-p)}$	maximum input signal capability (peak-to-peak value)	$f = 57 \pm 2\text{ kHz}$	200	–	–	mV
		$f < 50\text{ kHz}$	1.4	–	–	V
		$f < 15\text{ kHz}$	2.8	–	–	V
		$f > 70\text{ kHz}$	3.5	–	–	V
$R_{i(MPX)}$	input resistance	$f = 0\text{ to }100\text{ kHz}$	40	–	–	k Ω
57 kHz bandpass filter						
f_c	centre frequency	$T_{amb} = -40\text{ to }+85\text{ °C}$	56.5	57.0	57.5	kHz
B_{-3dB}	–3 dB bandwidth		2.5	3.0	3.5	kHz
$G_{SCOUT-MPX}$	signal gain	$f = 57\text{ kHz}$	17	20	23	dB
α_{sb}	stop band attenuation	$\Delta f = \pm 7\text{ kHz}$	31	–	–	dB
		$f < 45\text{ kHz}$	40	–	–	dB
		$f < 20\text{ kHz}$	50	–	–	dB
		$f > 70\text{ kHz}$	40	–	–	dB
$R_{o(SCOUT)}$	output resistance at pin SCOUT	$f = 57\text{ kHz}$	–	30	60	Ω
Comparator input (pin CIN)						
$V_{i(min)(rms)}$	minimum input level (RMS value)	$f = 57\text{ kHz}$	–	1	10	mV
R_i	input resistance		70	110	150	k Ω

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TIMING DATA

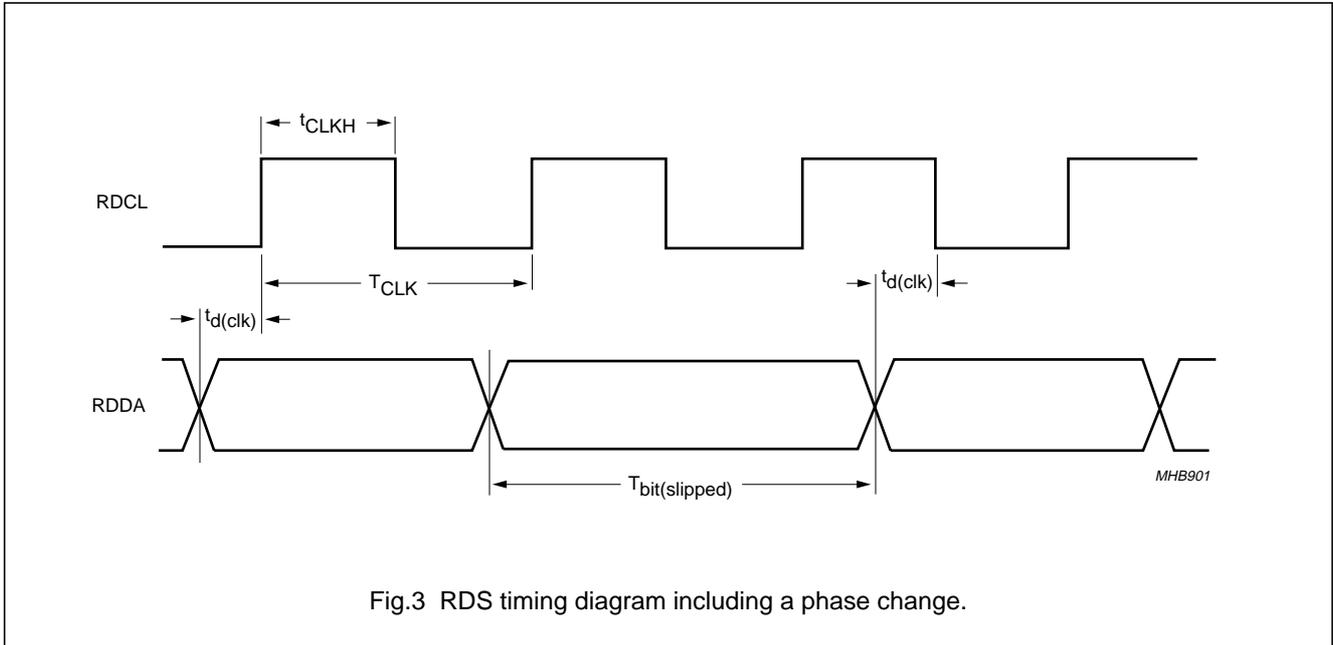


Fig.3 RDS timing diagram including a phase change.

Table 3 RDS timing (see Fig.3)

SYMBOL	PARAMETER	TYP.	UNIT
$t_{d(clk)}$	clock-data delay	4	μs
T_{CLK}	clock period	842	μs
t_{CLKH}	clock HIGH time	421	μs
$T_{bit(slipped)}$	slipped data bit period	1263	μs

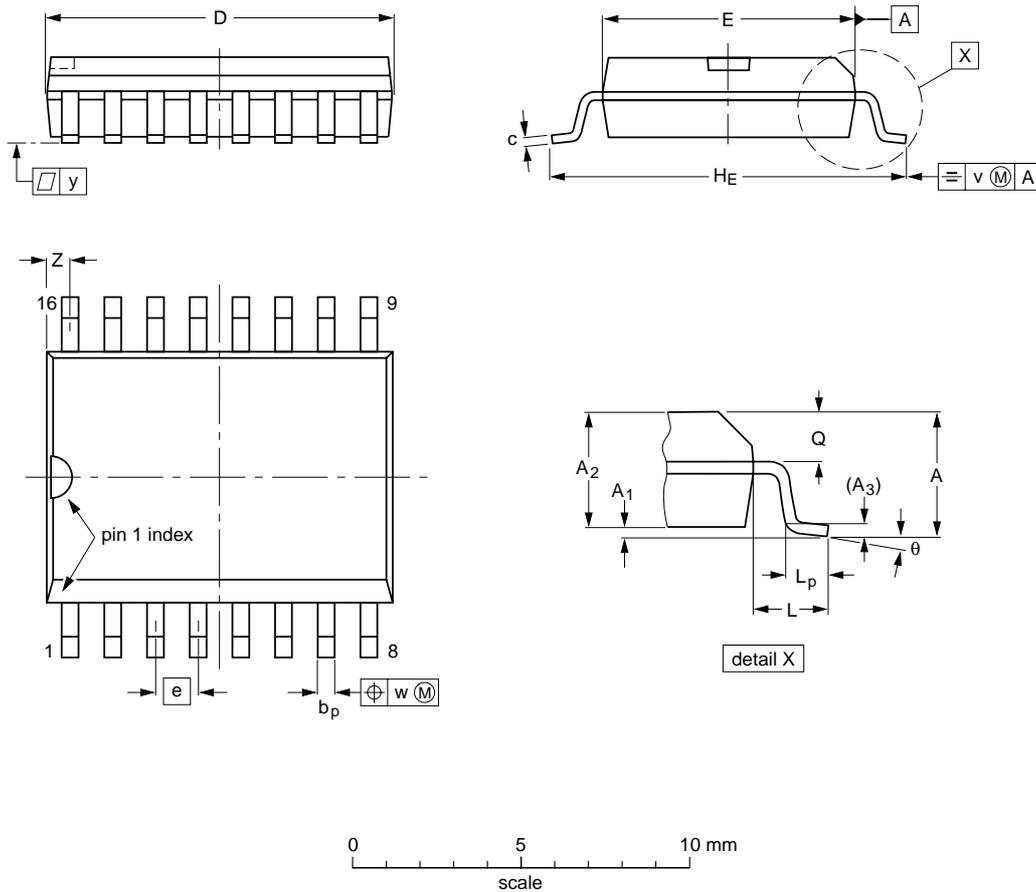
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				97-05-22 99-12-27

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SOLDERING**Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

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