1GHz low-voltage single Fractional-N synthesizer SA7015

DESCRIPTION

The SA7015 is a monolithic low power, high performance frequency synthesizer fabricated in QUBiC BiCMOS technology. It is compatible with the main synthesizer of the SA7025. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main divider to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A three modulus prescaler (divide by 64/65/72) is integrated on chip with a maximum input frequency of 1.0GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface.

FEATURES

- Operation up to 1.0GHz at 3V
- Fast locking by “Fractional-N” divider
- Internal charge pump and fractional compensation
- 3-line serial interface bus
- Low power consumption
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity:$V_{RF\ IN}$ = -20dBm

PIN CONFIGURATION

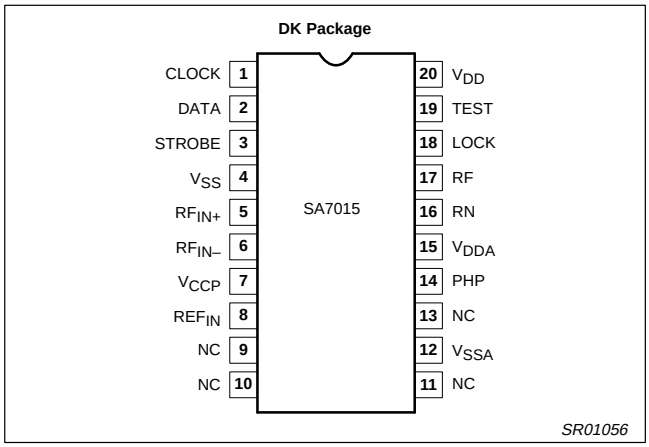

Figure 1. Pin Configuration

APPLICATIONS

- ADC (American Digital Cellular)
- Cellular radio
- Spread-Spectrum receivers
- Portable battery-powered radio equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA7015DK	SOT266-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
ΔV_{GND}	Difference in voltage between ground poins (these pins should be connected together)	-0.3 to +0.3	V
P_{TOT}	Total power dissipation		mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W. This device is ESD sensitive.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
NC	9	Not connected
NC	10	Not connected
NC	11	Not connected
V_{SSA}	12	Analog ground
NC	13	Not connected
PHP	14	Phase detector output
V_{DDA}	15	Analog supply voltage.
RN	16	Charge pump current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage.

BLOCK DIAGRAM

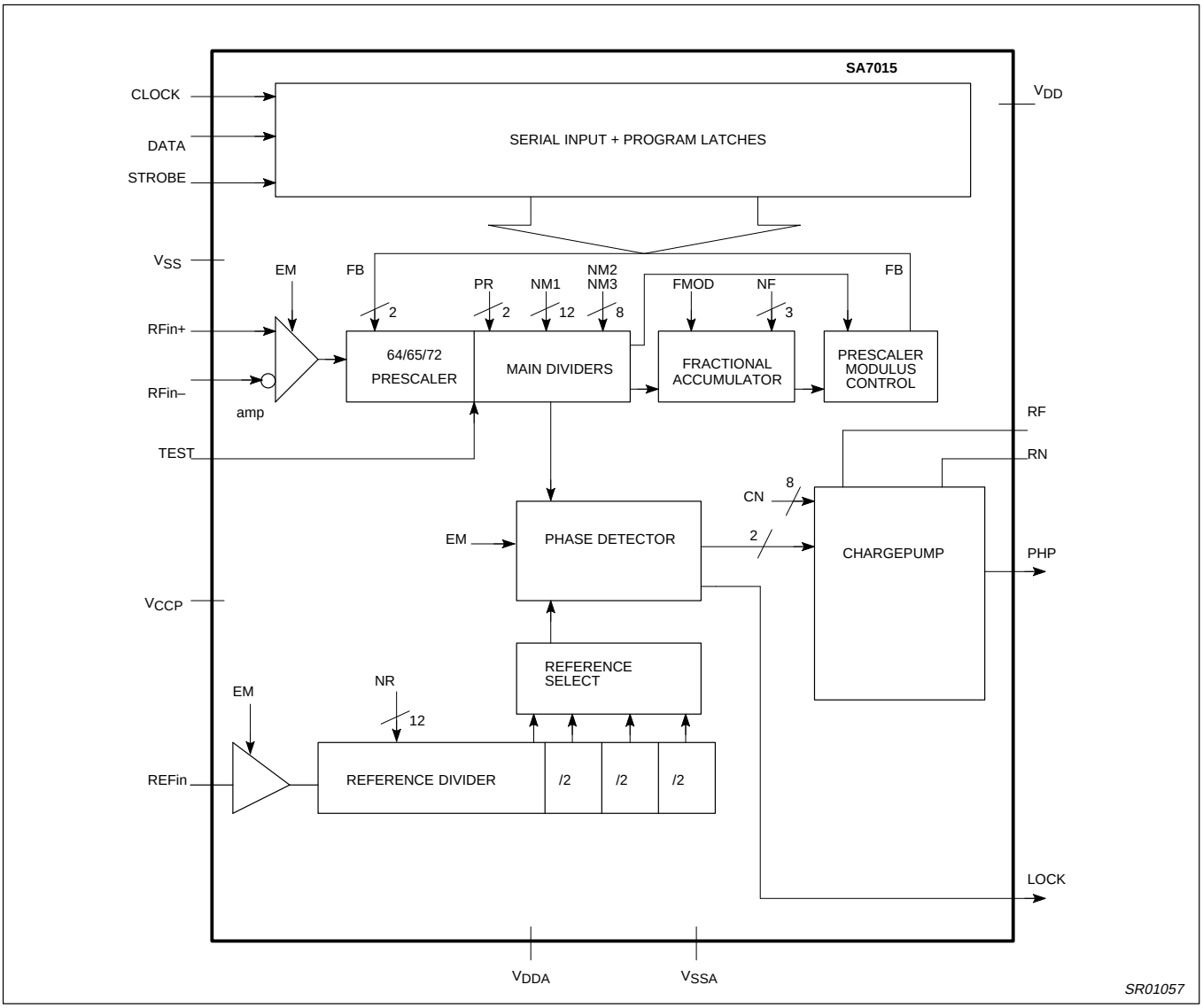

Figure 2. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_{DD} = V_{DDA} = V_{CCP} = 3V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{SUPPLY}	Recommended operating conditions	V_{CCP} = V_{DD}, $V_{DDA} \geq V_{DD}$	2.7		5.5	V
$I_{STANDBY}$	Total standby supply currents	EM = EA = 0, I_{RN} = I_{RF} = I_{RA} = 0		50	500	µA
I_{TOTAL}	Operational supply current[4]			5.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		0.7xV_{DD}		V_{DD}	V
V_{IL}	Low level input voltage range		0		0.3xV_{DD}	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{DD}-0.4			V
Charge pump PHP (notes 3, 5): V_{DDA} = 3V/IRx = 25µA or V_{DDA} = 5V/IRx = 62.5µA, V_{PHP} in range, unless otherwise specified						
$\|I_{RX}\|$	Setting current for RN or RF	2.7V < V_{DDA} < 5.5V		25		µA
		4.5V < V_{DDA} < 5.5V		62.5		
V_{PHP}	Output voltage range		0.7		V_{DDA}-0.8	V
I_{PHP}	Output current[7]	I_{RN} = -62.5µA, V_{PHP} = V_{DDA}/2 (Note 7)	440	550	660	µA
		I_{RN} = -25µA, V_{PHP} =V_{DDA}/2	175	220	265	
ΔI_{PHP}	Relative output current variation	I_{RN} = -62.5µA[1,7]		2	6	%
I_{PHP_PN}	Output current matching	I_{RN} = -25µA, V_{PHP} =V_{DDA}/2 (Note 7)			±50	µA
		I_{RN} = -62.5µA, V_{PHP} = V_{DDA}/2			±65	
I_{PHP_I}	Output leakage current (pump not active)	V_{PHP} =0.7 to V_{DDA}-0.8	-20	0.1	20	nA
Fractional compensation pump V_{RN} = V_{DDA}, V_{PHP} = V_{DDA}/2						
I_{PHP_F}	Fractional compensation output current PHP vs F_{RD}	I_{RF} = -62.5µA;F_{RD} = 1 to 7 (Note 7)	-625	-400	-250	nA
		I_{RF} = -25µA;F_{RD} = 1 to 7	-250	-180	-100	

AC ELECTRICAL CHARACTERISTICS

V_{DD} = V_{DDA} = 3V; T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider guaranteed and tested on an automatic tester. Some performance parameters may be improved by using optimized layout.						
f_{RF_IN}	Input signal frequency	Pin = -20dBm, Direct coupled input	0	1.0		GHz
		Pin = -20dBm, 1000pF input coupling		1.0		
V_{RF_IN}	Input sensitivity	f_{IN} = 1000MHz	-20		0	dBm
Reference divider (V_{DD} = V_{DDA} = 3V or V_{DD} = 3V / V_{DDA} = 5V)						
f_{REF_IN}	Input signal frequency	2.7 < V_{DD} and V_{DDA} < 5.5V			25	MHz
		2.7 < V_{DD} and V_{DDA} < 4.5V			30	
V_{REF_IN}	Input signal range, AC coupled	2.7 < V_{DD} and V_{DDA} < 5.5V	500			mV_{P-P}
		2.7 < V_{DD} and V_{DDA} < 4.5V	300			
Z_{REF_IN}	Reference divider input impedance			100		kΩ
				2		pF
Serial interface						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
t_{SW}	Pulse width; STROBE		30			ns
t_{SW}	Pulse width; STROBE	A word, PR = '01'	(NM2x65)/Fvco +Tw			
		A word, PR = '10'	[NM2x65 + (NM3+1)x72]/Fvco +Tw			

NOTES:

1. The relative output current variation is defined thus : $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I2 - I1)}{I(I2 + I1)}$ withV1=0.7V,V2=Vdda-0.8V
2. FRD is the value of the fractional accumulator
3. Monotonicity is guaranteed with CN = 0 to 255
4. Power supply current measured in loop
5. Specification condition : CN = 255
6. The matching is defined by the sum of the P and the N pump for a given output voltage.
7. Limited analog supply voltage to 4.5 to 5.5V
8. For F_{IN} <50MHz, low frequency operation requires DC coupling and a minimum input slew rate of 32V/µs.
9. Guaranteed by design

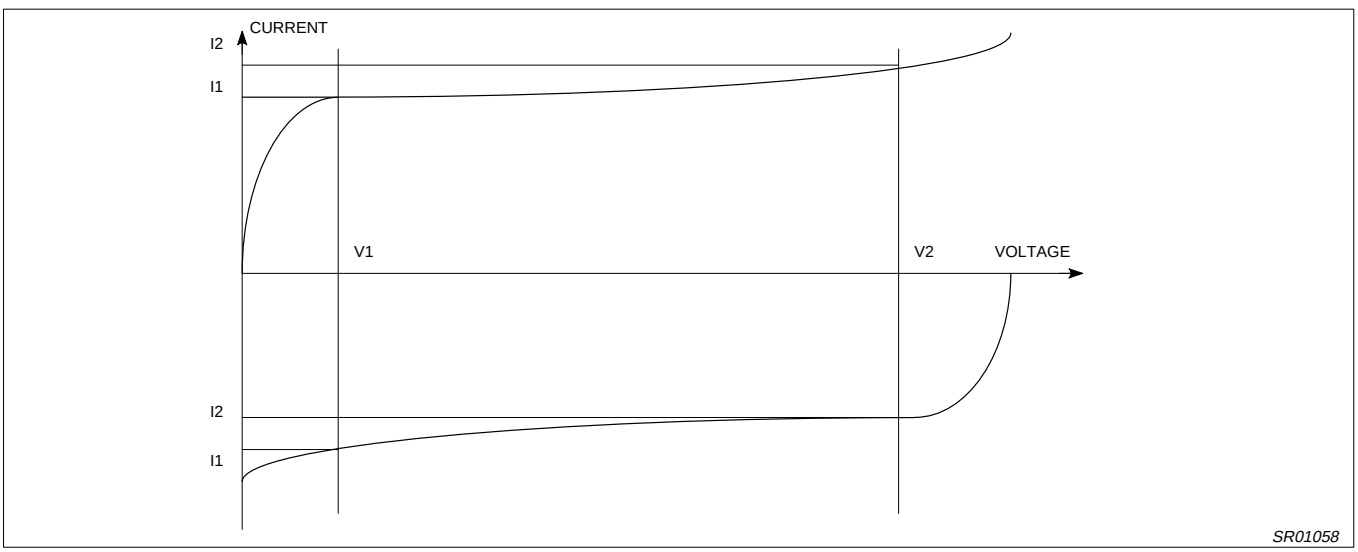

Figure 3. Relative Output Current Variation

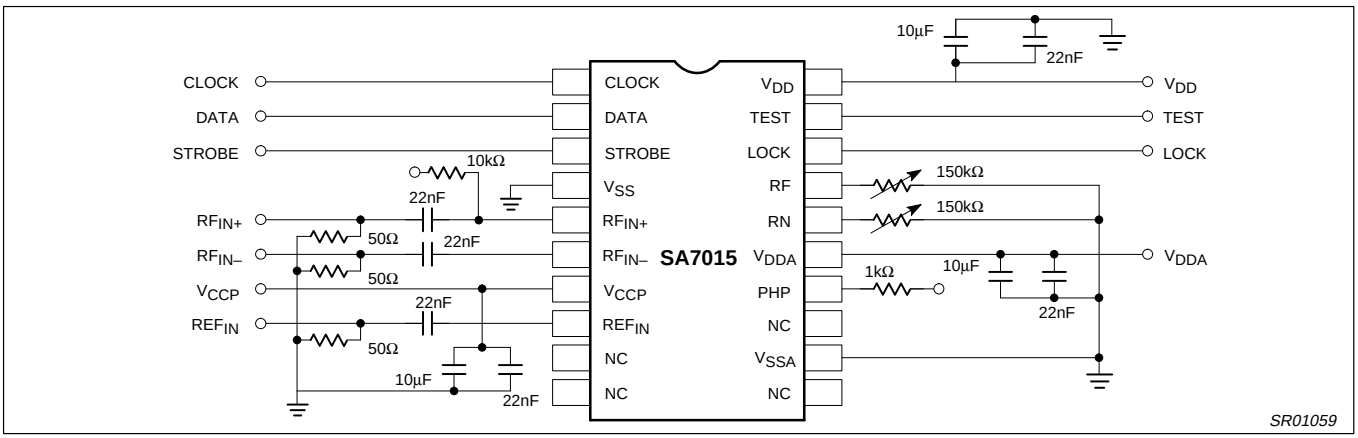

Figure 4. Test Circuit

AC TIMING CHARACTERISTICS

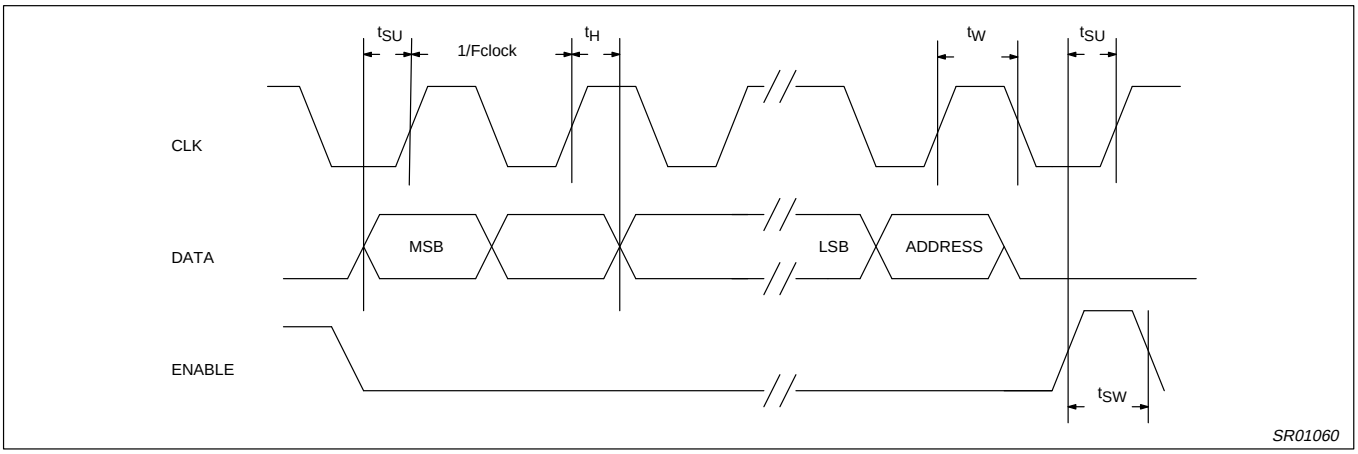

Figure 5. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial input programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DAC, selection and enable bits. The programming data is structured into 24- or 32-bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE=H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 3 words must be sent: D,B, and A. Figure 4 and Table 1 show the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is strored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider input. CN is only loaded from the temporary registers when a short 24-bit A0 word is issued. CN will be directly loaded by programming a long 32-bit A1 word. The flag LONG in the D word determines whether A0 (LONG='0') or A1 (LONG='1') format is applicable. The A word contains new data for the main divider.

Main divider synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO cycles.

For PR='01' Tstrobe_min $\left(\frac{1}{F_{VCO}}\ (NM2.65)\ +\ T_W\right)$

For PR='10' Tstrobe_min

$\left(\frac{1}{F_{VCO}}\ (NM2.65)\ +\ (NM3\ +\ 1)\ 72)\ +\ T_W\right)$

Reference Divider

The input signal on REF_in is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the EM bit. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR=4 to 4095) followed by a three bit binary counter. The 2 bit SM register determines which of the 4 output pulses is selected as the phase detector input.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (-20dBm at 1.0GHz) making the prescaler ideally suited to direct interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/72, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM='1'. Disabling means that all currents in the prescaler are switched off.

The main divider consists of a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Tables 2 and 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explainded in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD='1'. Each time the accumulator overflows, the feedback to the prescaler will select on cycle using prescaler ratio R2 instead of R1. The mean division ratio over Q main divider will then be NQ=N+NF/Q

Programming a fraction means the prescaler with main divider will divide by N or N+1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the content of the fractional accumulator FRD, which is used for fractional current compensation.

Internal Registers

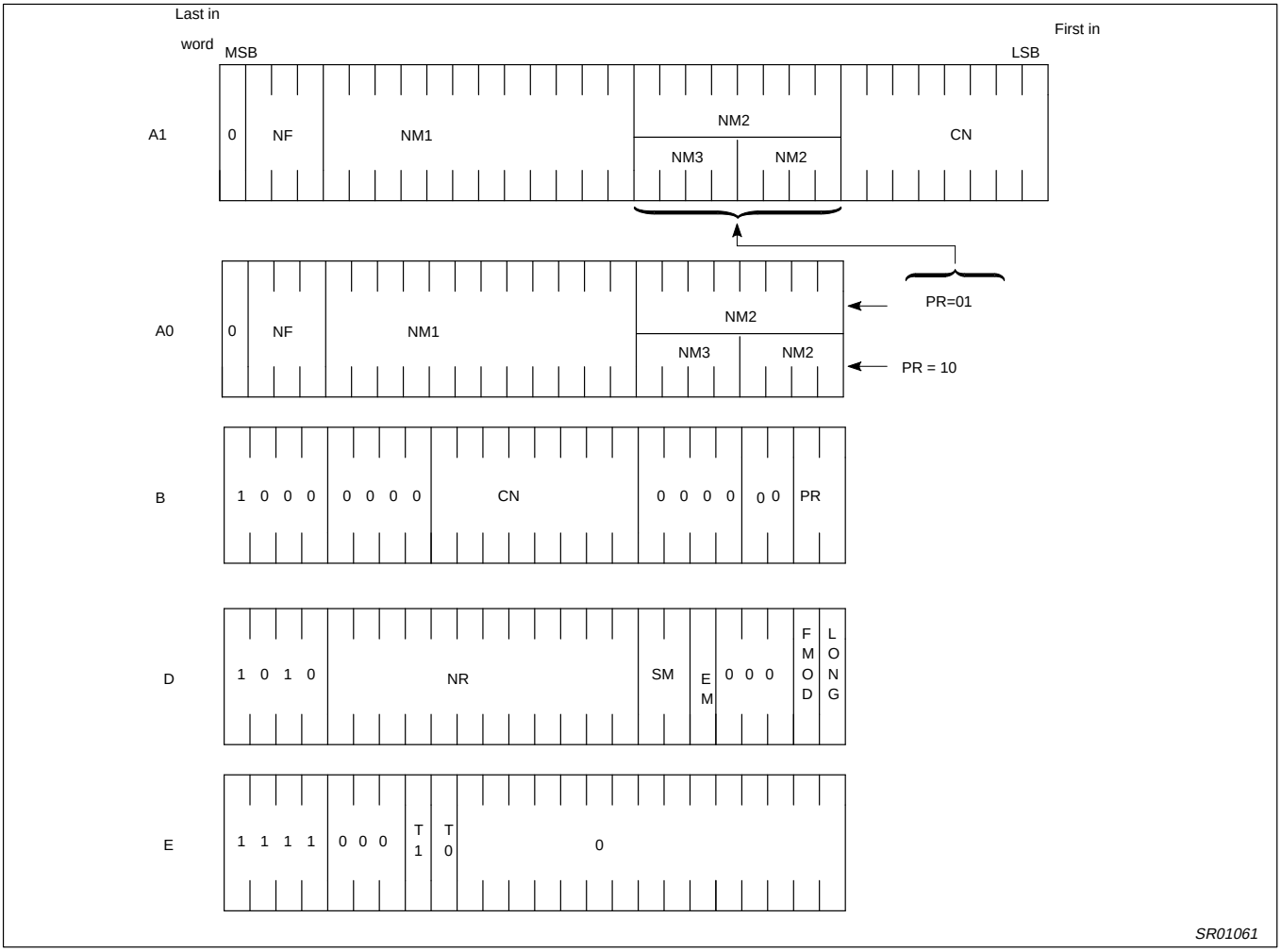

Figure 6. Serial Bus Timing Diagram

Table 2. Register Description

SYMBOL	BITS	FUNCTION
NM1	12	Number of main divider cycles when prescaler modulus=64
NM2	4 or 8	Number of main divider cycles when prescaler modulus=65
NM3	4	Number of main divider cycles when prescaler modulus=72
PR	2	Prescaler type in use PR=”01”: modulus 2 prescaler (64/65) PR=”10”: modulus 3 prescaler (64/65/72)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection “1”: modulo 8 “0”: modulo5
LONG	1	A word format selection “0”: 24 bit A0 format “1”: 32 bit A1 format
CN	8	Binary current setting factor for the chargepump
EM	1	Enable bit. “1”: synthesizer is ON
SM	2	Reference divider output selection SM=”00”: No extra division on reference divider SM=”01”: Extra divide by 2 SM=”10”: Extra divide by 4 SM=”11”: Extra divide by 8
NR	12	Reference divider ratio

Table 3. Prescaler Ratio

The total division ration from prescaler to the phase detector may be expressed as:	
if PR= ‘01’	N = (NM1 + 2) x 64 + NM2 x 65
if PR= ‘10’	N = (NM1 + 2) x 64 + N2 x 65 + (NM3 + 1) x 72
When the fractional accumulator overflows, the divide ratio is increased by 1	

Table 4. PR Modulus

PR	Modulus prescaler	Bit capacity		
		NM1	NM2	NM3
01	2	12	8	-
10	3	12	4	4

Phase Detector

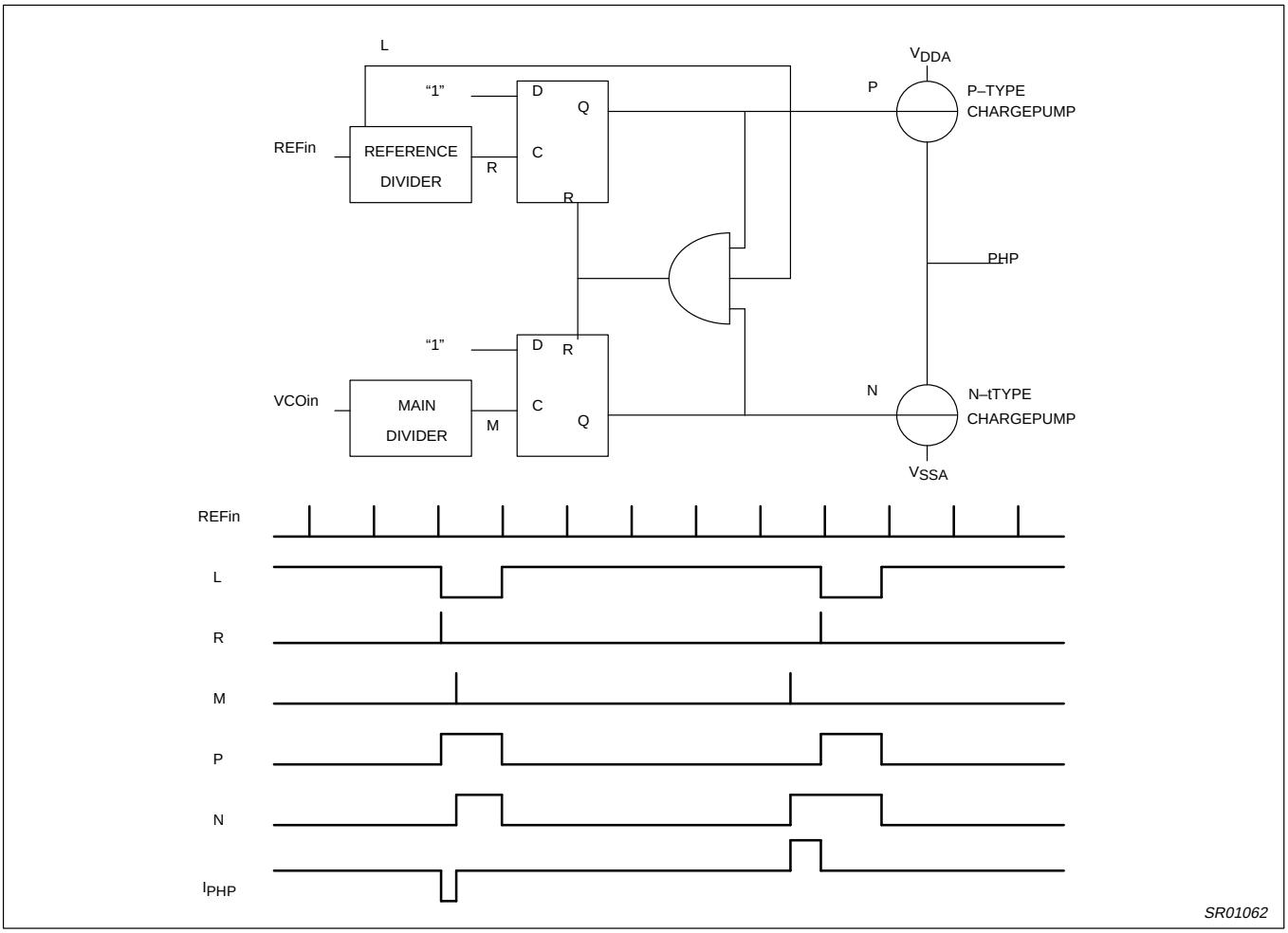

Figure 7. Phase Detector Structure with Timing

The phase detector is a two D-type flip-flop phase and frequency detector shown in Figure 7. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error, this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive an on-chip chargepump. A source current from the chargepump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA7015 has two current setting pins: RN and RF. The active chargepump current and the fractional compensation current are linearly dependent on the current connected between the current setting pin and V_{SSA}. The typical value R (current setting resistor) can be calculated with the formula: $R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$

The current can be set to zero by connecting the corresponding pin to V_{DDA}. All currents are off when the part is disabled through the EM bit of the serial interface.

Chargepump output and fractional compensation current

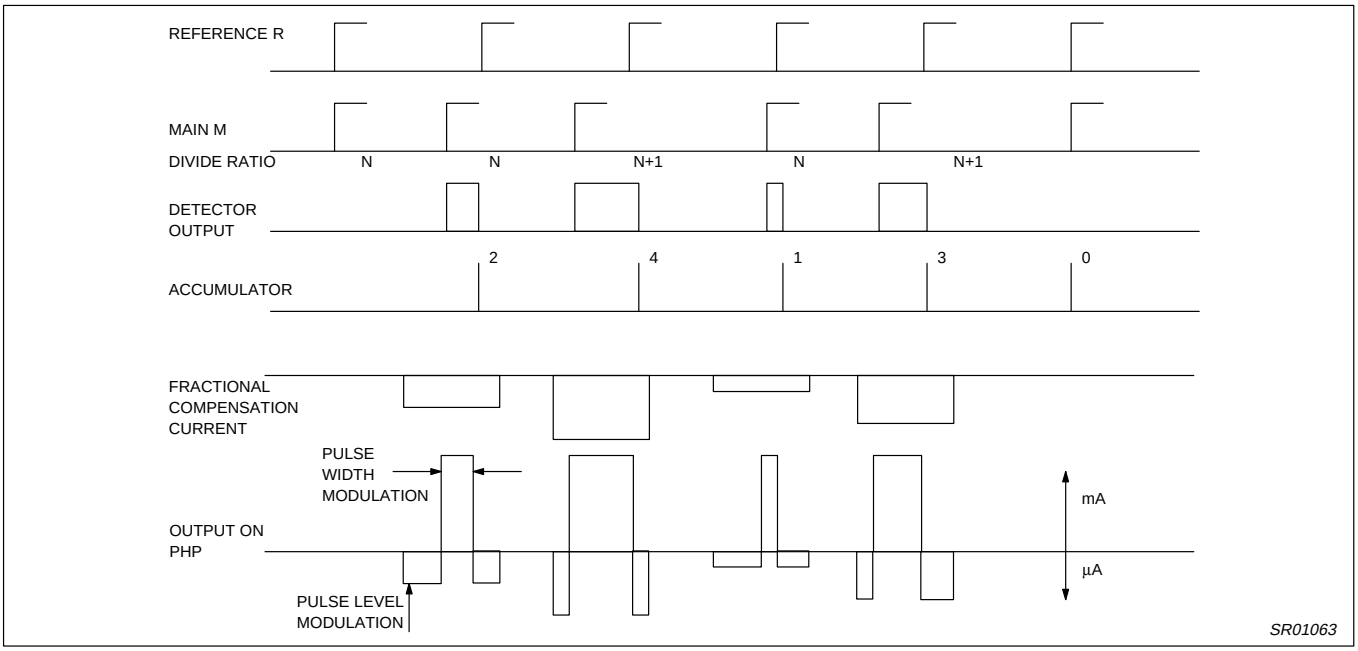

Figure 8. Waveforms for NF = 2, Fraction = 0.4

The chargepump on pin PHP is driven by the phase detector and the current value is determined by the current at pin RN and the CN DAC which is driven by a register of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD. The timing for the fractional compensation is derived from the reference divider. The current is on during one input reference cycle before and one cycle after the output signal to the phase comparator. Figure 8 shows the waveform for a typical case.

$I_{PHP} = I_{NOMINAL} + I_{FRACTIONAL\_COMPENSATION}$

$I_{NOMINAL} = CN * I_{RN}/32$: charge pump current

$I_{FRACTIONAL\_COMPENSATION} = FRD * I_{RF}/128$: fractional compensation current.

Figure 9 shows that for a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the input RN, RF is approximately $\frac{I_{RN}}{I_{RF}} = \frac{(Q \cdot F_{VCO})}{(3 \cdot CN \cdot F_{REF})}$

where :

Q=fractional-N modulus

F_{VCO} = input frequency of the prescaler

F_{REF} = input frequency of the reference divider.

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REFin. The lock condition is also fulfilled when the synthesizer is disabled.

Test Modes

The lock ouput is selectable as F_{REF}, F_{MAIN} and lock. Bits T1 and T0 of the E word control the selection.

T1=0 and T0=0 or the E register is not programmed : lock output is configured as lock indicator.

T1=0 and T0=1, the lock output gives the output of the reference divider

T1=1 and T0=1, the lock output gives the output of the main divider.

The E register is reset to 0 anytime the D word is programmed.

The test input pin (Pin 19) is a buffured logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the main divider; while in this condition the input to the prescaler, RFin, may be connected to V_{CCP} through a 10kΩ resistor in order to place the prescaler output into a known state.