DATA SHEET

SA2421
2.45 GHz low voltage RF transceiver

Product specification
Supersedes data of 2000 Feb 11

2000 Mar 13

Philips
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2.45 GHz low voltage RF transceiver SA2421

DESCRIPTION

The SA2421 transceiver is a combined low–noise amplifier, receive mixer, transmit mixer and LO buffer IC designed using a 20 GHz f_T BiCMOS process, QUBiC2, for high–performance low–power communication systems for 2.4–2.5 GHz applications. The LNA has a 3.2 dB noise figure at 2.45 GHz with 14.3 dB gain and an IP3 intercept of –3 dBm at the input. The wide–dynamic–range receive mixer has a 11.2 dB noise figure and an input IP3 of +2.5 dBm at 2.45 GHz. The nominal current drawn from a single 3 V supply is 34 mA in transmit mode and 20 mA in receive mode. The SA2421 differs from the SA2420 by removal of the LO doubler and LO switch. The LNA reverse isolation is improved, and a separate pin is allocated for the transmit output.

FEATURES

- Low current consumption: 34 mA nominal transmit mode and 20 mA nominal receive mode
- High system power gain: 24 dB (LNA + Mixer) at 2.45 GHz
- Excellent gain stability versus temperature and supply voltage
- Separate Rx IN and Tx OUT pins
- Wide IF range: 50–500 MHz
- –10dBm typical LO input power
- Improved LNA reverse isolation S12
- TSSOP24 package

PIN CONFIGURATION

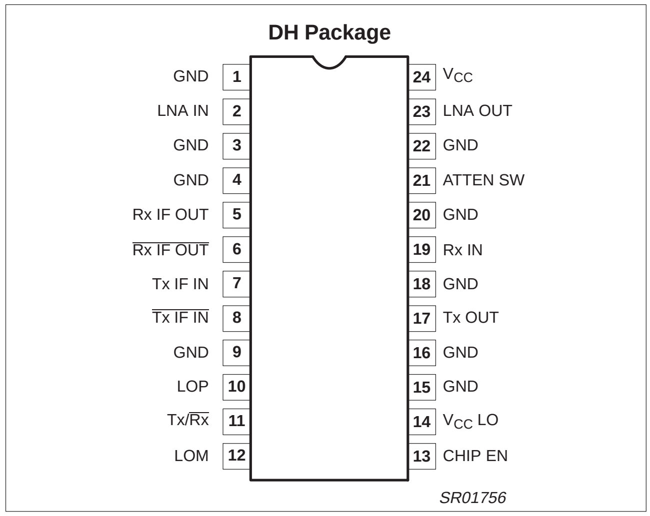


Figure 1. Pin configuration

APPLICATIONS

- IEEE 802.11 (WLAN)
- 2.45 GHz ISM band

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	–40°C to +85°C	SA2421DH	SOT355-1

BLOCK DIAGRAM

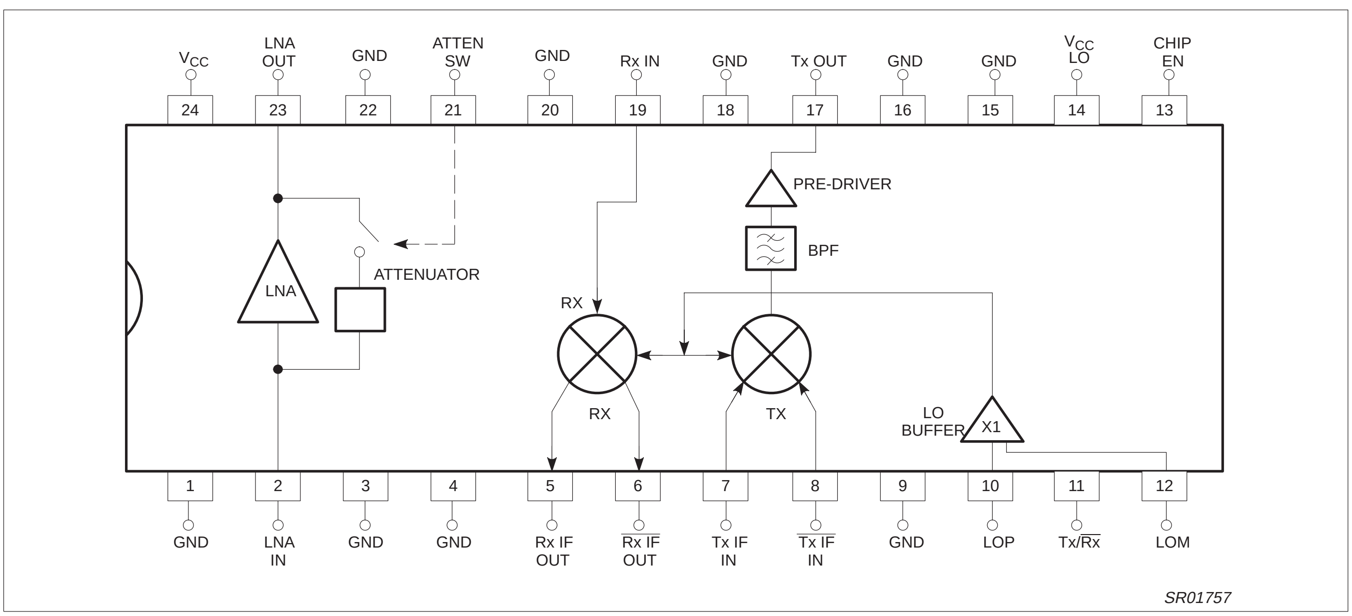


Figure 2. SA2421 block diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	–0.3 to +6	V
V_{IN}	Voltage applied to any pin	–0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_{amb} = 25°C (still air) 24-Pin Plastic TSSOP	555	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power (RF/IF/LO pins)	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTES:
1. Transients exceeding these conditions may damage the product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, and absolute maximum ratings may impact product reliability θ_{JA}: 24-Pin TSSOP = 117°C/W
3. IC is protected for ESD voltages up to 2000 V, human body model.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_{amb}	Operating ambient temperature range	–40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_{amb} = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CCTX}	Total supply current, Transmit	Tx/Rx = Hi	22	34	42	mA
I_{CCRX}	Total supply current, Receive	Tx/Rx mode = Lo, LNA = Hi gain	14	20	26	mA
$I_{CC\ OFF}$	Power down mode	Tx/$\overline{Rx}$ = GND Atten SW = V_{CC} Enable = GND			10	µA
V_{LNA-IN}	LNA input voltage	Receive mode		0.855		V
$V_{LO\ GHz}$	LO buffer DC input voltage	Tx/Rx = Lo	–0.1		V_{CC}	V
$V_{TX\ IF}$	Tx Mixer input voltage	Tx/Rx = Hi		1.7		V
$V_{TX\ IFB}$	Tx Mixer input voltage	Tx/Rx = Hi		1.7		V
I_{BIAS}	Input bias current	Logic 1		6		µA
		Logic 0		0		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3 V, T_{amb} = 25°C; LO_{IN} = –10 dBm @ 2.1 GHz; f_{RF} = 2.45 GHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
f_{RF}	RF frequency range[3]		2.4		2.45		2.5	GHz
f_{IF}	IF frequency range[3]		300		350		400	MHz
LNA High gain mode (In = Pin 2; Out = 23)								
S_{21}	Amplifier gain	LNA gain = Hi		13.3	14.3	15.3		dB
S_{12}	Amplifier reverse isolation	LNA gain = Hi			–32			dB
S_{11}	Amplifier input match[1]	LNA gain = Hi			–10			dB
S_{22}	Amplifier output match[1]	LNA gain = Hi			–9			dB
ISO	Isolation: LO_X to LNA_{IN}	LNA gain = Hi			–43			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Hi			–15			dBm
IP3	Amplifier input third order intercept	f_1 - f_2 = 1 MHz, LNA gain = Hi		–4.5	–3.2	–1.9		dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Hi		3.1	3.2	3.3		dB
LNA High Overload Mode (low gain mode)								
S_{21}	Amplifier gain	LNA gain = Low		–18.5	–19.4	–20.3		dB
S_{12}	Amplifier reverse isolation	LNA gain = Low			–26			dB
S_{11}	Amplifier input match[1]	LNA gain = Low			–8			dB
S_{22}	Amplifier output match[1]	LNA gain = Low			–8			dB
ISO	Isolation: LO_X to LNA_{IN}	LNA gain = Low			–45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Low			2			dBm
IP3	Amplifier input third order intercept	f_1 – f_2 = 1 MHz, LNA gain = Low			18			dBm
NF	Amplifier noise figure (50 Ω)	LNA gain = Low			18.5			dB
Rx Mixer (Rx IN = Pin 19, IF = Pins 5 and 6, LO = Pin 10 or 12, P_{LO} = –10 dBm)								
PG_C	Power conversion gain into 50 Ω : matched to 50 Ω using external balun circuitry.	f_S = 2.45 GHz, f_{LO} = 2.1 GHz, f_{IF} = 350 MHz		9.5	10	10.5		dB
S_{11-RF}	Input match at RF (2.45 GHz)[1]				–11			dB
NF_M	SSB noise figure (2.45 GHz) (50 Ω)			9.8	11.2	12.5		dB
P_{-1dB}	Mixer input 1 dB gain compression				–10.5			dBm
IP3	Input third order intercept	f_1 – f_2 = 1MHz		1.8	2.2	2.6		dBm
Rx Mixer Spurious Components (P_{IN} = P_{-1dB})								
P_{RF-IF}	RF feedthrough to IF[4]	C_L = 2 pF per side			-35			dBc
P_{LO-IF}	LO feedthrough to IF[5]	C_L = 2 pF per side			-32			dBc

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
Tx Mixer (Tx OUT = Pin 17, IF = Pins 7 and 8, LO = Pin 10 or 12, P_{LO} = –10 dBm)								
PG_C	Power conversion gain: R_L = 50 Ω R_S = 50 Ω	f_S = 2.45 GHz, f_{LO} = 2.1 GHz, f_{IF} = 350 MHz		22.5	23	23.5		dB
$S_{11–RF}$	Output match at RF (2.45 GHz)[1]				–10			dB
NF_M	SSB noise figure (2.45 GHz) (50 Ω)			10.9	11.2	11.5		dB
P_{-1dB}	Output 1dB gain compression				4.2			dBm
IP3	Output third order intercept	$f_1 – f_2$ = 1 MHz		10.1	12.2	14.3		dBm
Tx Mixer Spurious Components ($P_{OUT} = P_{–1dB}$)								
P_{IF-RF}	IF feedthrough to RF[4]				–50			dBc
P_{LO-RF}	LO feedthrough to RF[5]				–22			dBc
$P_{IMAGE-RF}$	Image feedthrough to RF[6]				–20			dBc
LO Buffer								
$P_{LO\ IN}$	LO drive level		–15		–10		–5	dBm
S_{11-LO}	Mixer input match (LO = 2.1 GHz)				–10			dB
f_{LOG}	LOG frequency range[3]		1.9		2.1		2.3	GHz
Switching[2]								
t_{Rx-Tx}	Receive-to-transmit switching time				1			µs
t_{Tx-Rx}	Transmit-to-Receive switching time				1			µs
$t_{POWER\ UP}$	Chip enable time				1			µs
$t_{PWR\ DWN}$	Chip disable time				1			µs

NOTES:
1. With simple external matching
2. With 50 pF coupling capacitors on all RF and IF parts
3. This part has been optimized for the stated frequency range. Operation outside this frequency range may yield performance other than specified in this datasheet.
4. Measured 5dB lower than 1dB compression point, with typical output matching network.
5. Measured at 1dB compression point.
6. With typical output matching network (no image reject mixer is used).

Table 1. Truth Table

Chip-En	ATT-SW	T_X–$\overline{R_X}$	Mode	LNA Gain	R_X Mixer	T_X Mixer and Predriver
0	X	X	Sleep	N/S	off	off
1	1	0	Receive	+14.3 dB	on	off
1	0	0	Receive	–19 dB	on	off
1	X	1	Transmit	N/S	off	on

FUNCTIONAL DESCRIPTION

The SA2421 is a 2.45 GHz transceiver front-end available in the TSSOP-24 package. This integrated circuit (IC) consists of a low noise amplifier (LNA) and up- and down-converters. There is an enable/disable switch available to power up/down the entire chip in 1 µs, typically. This transceiver has several unique features.

The LNA has two operating modes: 1) high gain mode with a gain = +14.3 dB; and 2) low gain mode with a gain –19 dB. The switch for this option is internal and is controlled externally by high and low logic to the pin. When the LNA is switched into the attenuation mode, active matching circuitry (on-chip) is switched in (reducing the number of off-chip components required). To reduce power consumption when the chip is transmitting, the LNA is automatically switched into a “sleep” mode (internally) without the use of external circuitry.

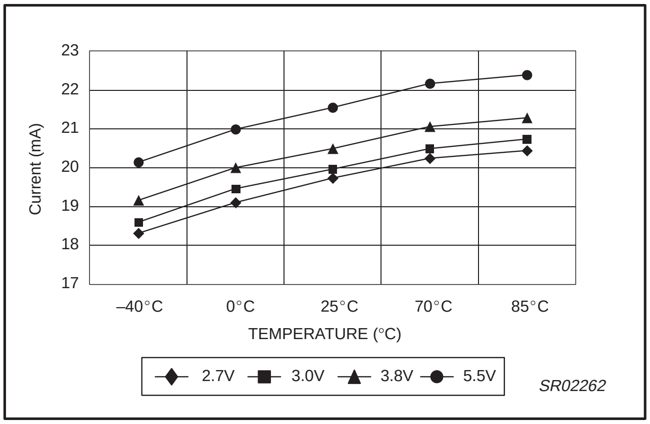


Figure 3. LNA / Receive Supply Current vs Supply Voltage and Temperature

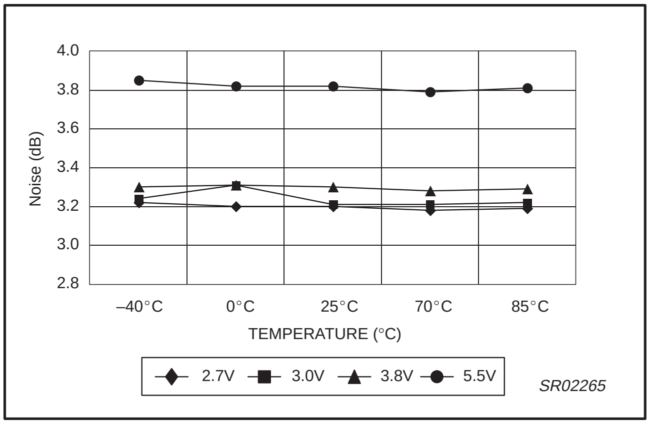


Figure 6. LNA Noise Figure vs Supply Voltage and Temperature

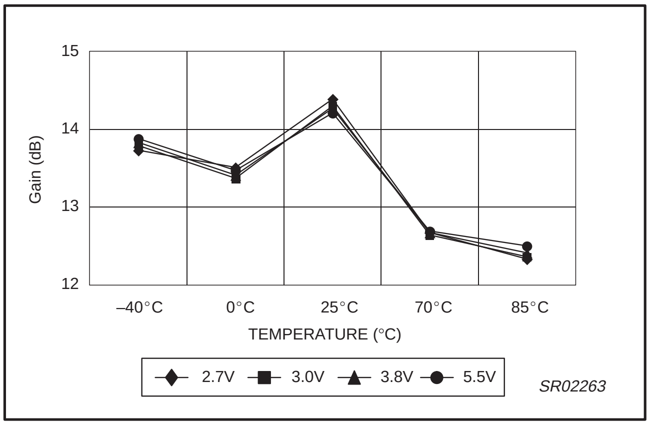


Figure 4. LNA Gain vs Supply Voltage and Temperature

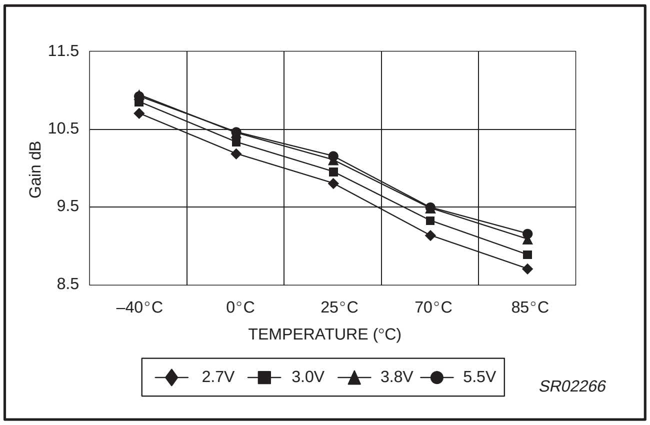


Figure 7. RX Gain vs Supply Voltage and Temperature

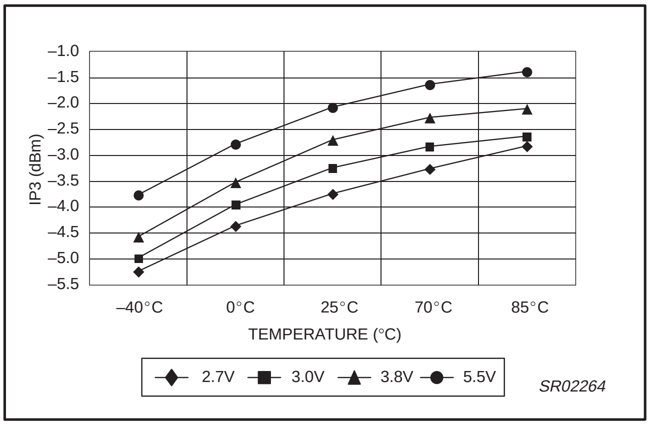


Figure 5. LNA Input IP3 vs Supply Voltage and Temperature

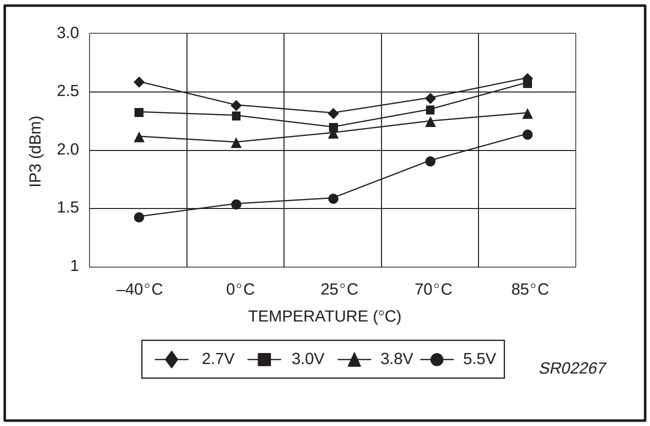


Figure 8. Receive Input IP3 vs Supply Voltage and Temp

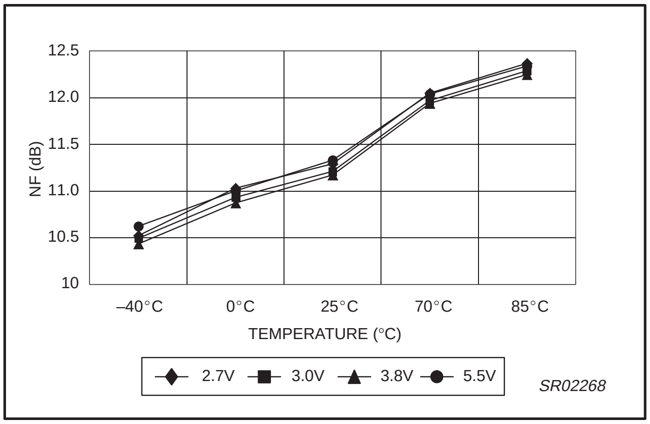


Figure 9. Receive Noise Figure vs Supply Voltage and Temp

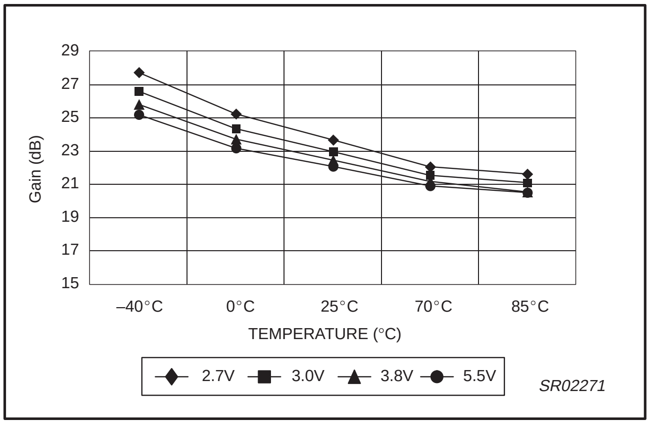


Figure 12. Transmit Gain vs Supply Voltage and Temp

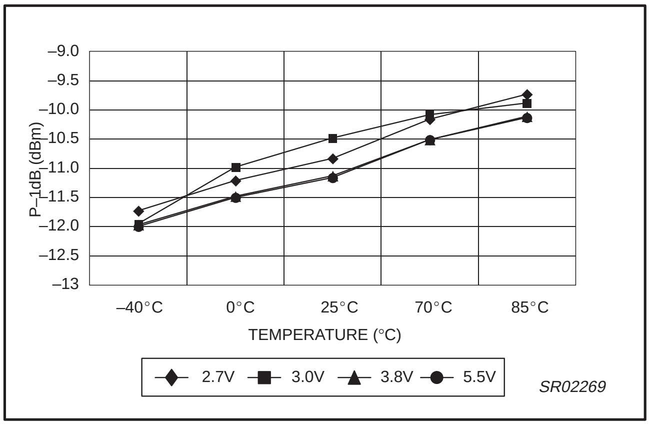


Figure 10. RX 1dB Compression vs Supply Voltage and Temp

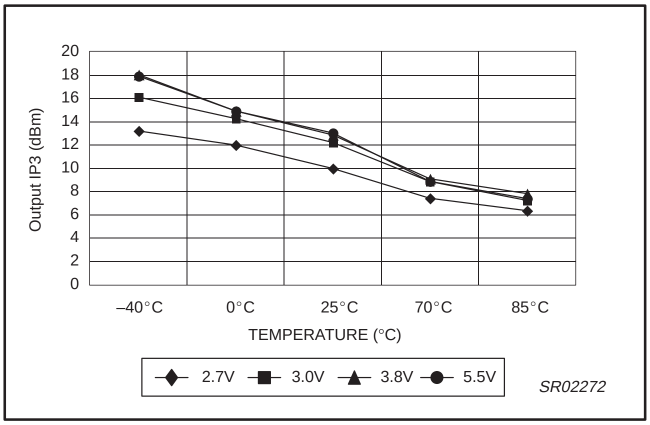


Figure 13. Transmit Output IP3 vs Supply Voltage and Temp

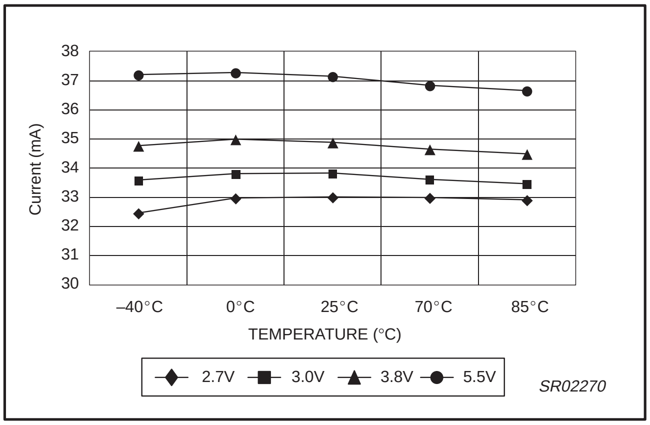


Figure 11. Transmit Current vs Supply Voltage and Temp

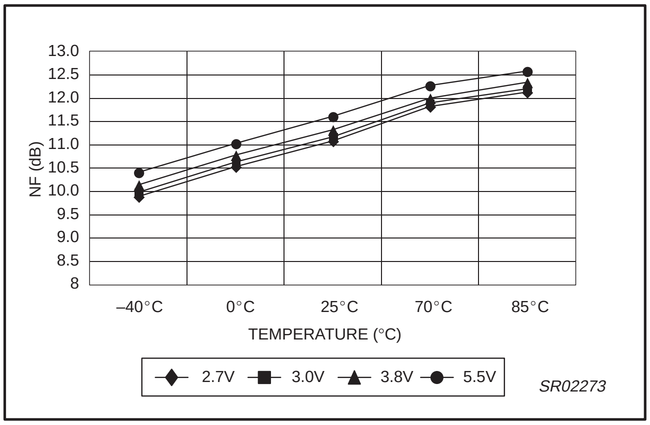


Figure 14. Transmit Noise Figure vs Supply Voltage and Temp

2.45 GHz low voltage RF transceiver SA2421

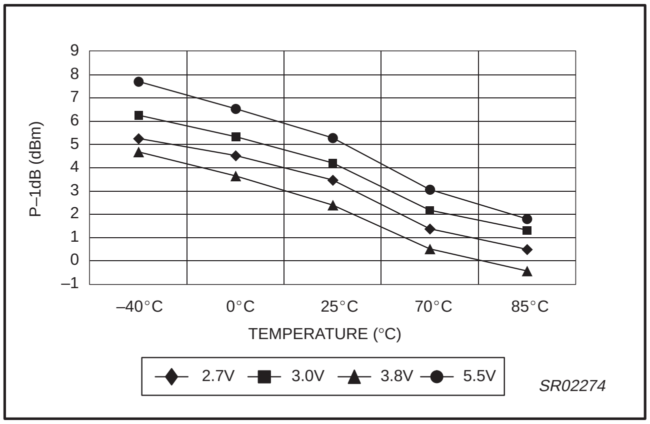


Figure 15. TX 1dB compression vs Supply Voltage and Temp

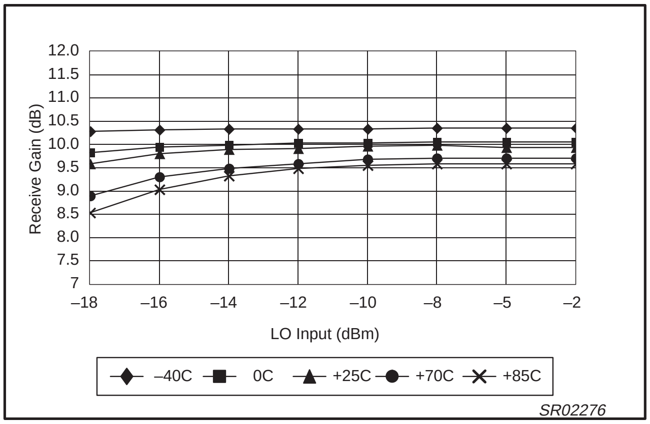


Figure 17. Receive Gain vs LO Input over Temp Range

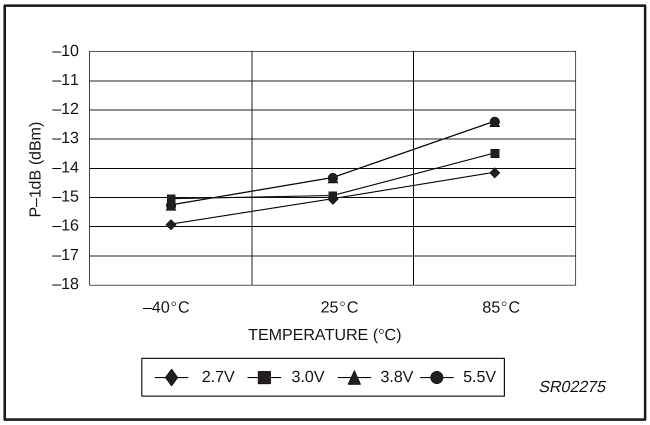


Figure 16. LNA 1dB compression vs Supply Voltage and Temp

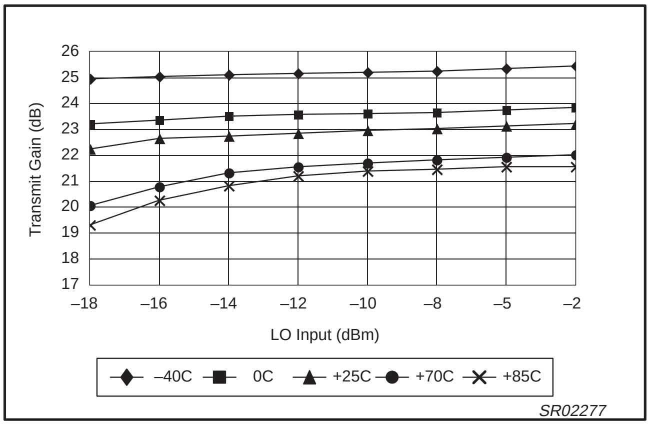


Figure 18. Transmit Gain vs LO Input over Temp Range

The Rx IN port is matched to 50 Ω and has an input IP3 of +2.2 dBm (mixer only). The down-convert mixer is buffered and has open collectors at the pins to allow for matching to common SAW filters. The up convert mixer has an input pin to output pin gain of 23 dB. The output of the up-converter is designed for a power level = +4.2 dBm (P_{-1dB}).

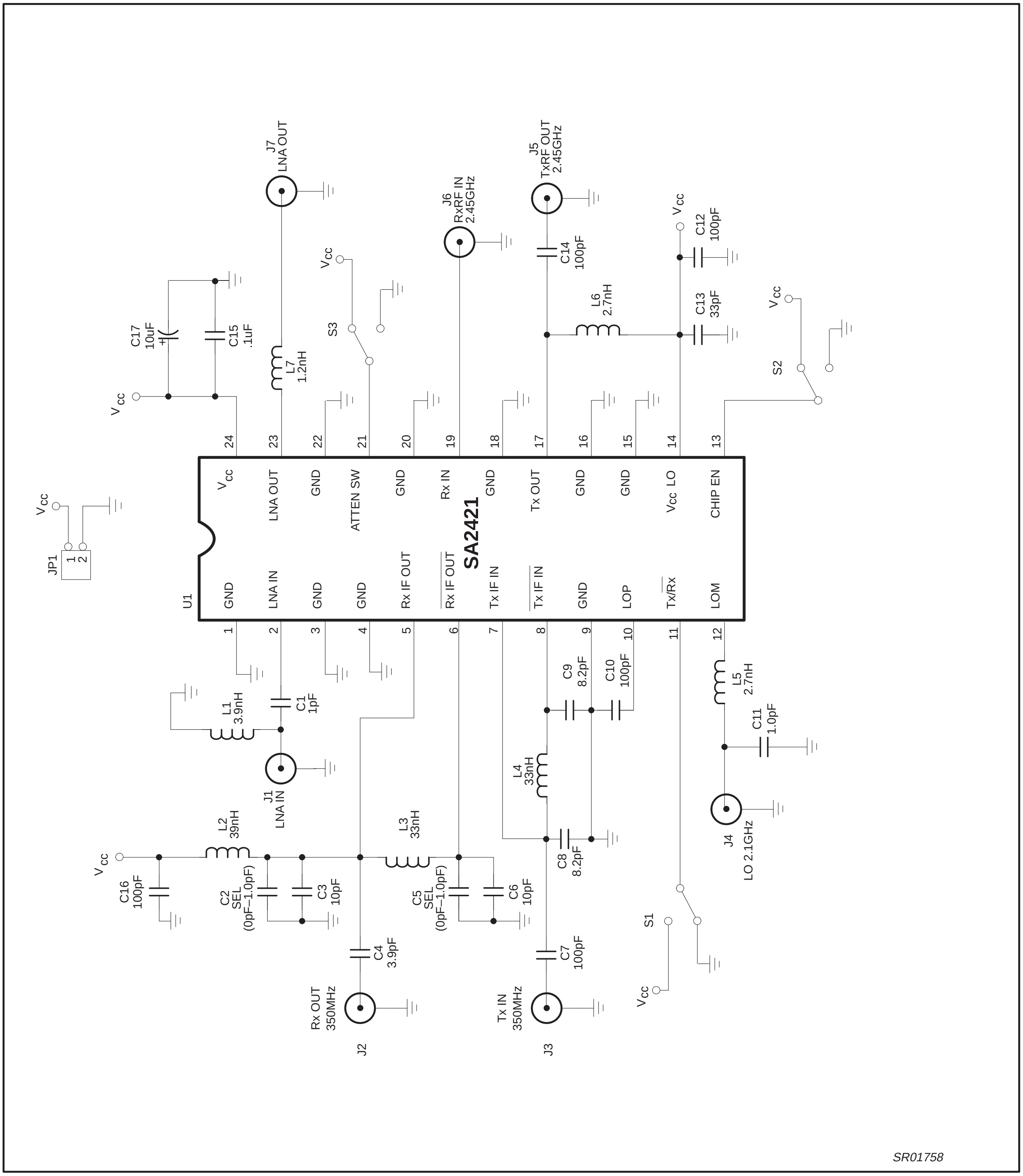
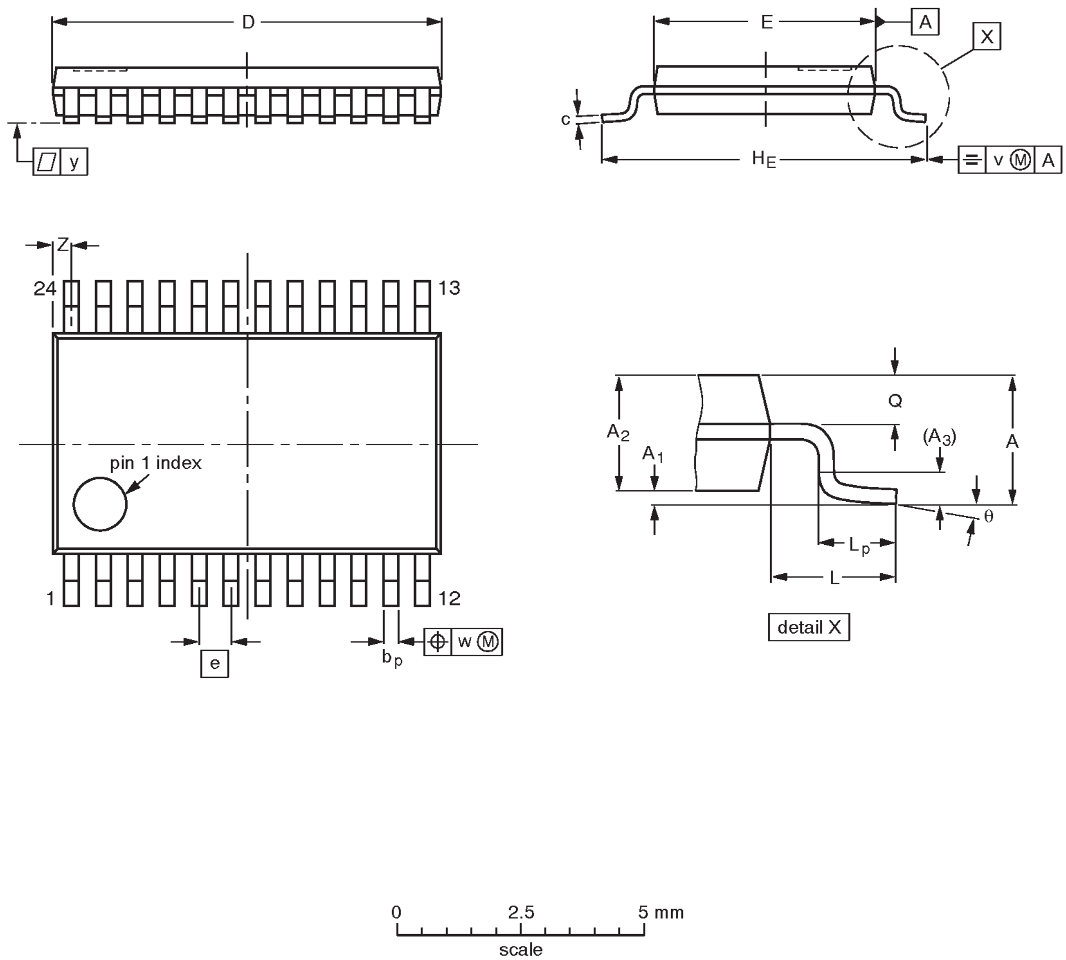

SA2421
U1
GND
LNA IN
GND
GND
Rx IF OUT
Rx IF OUT
Tx IF IN
Tx IF IN
GND
LOP
Tx/Rx
LOM
VCC
LNA OUT
GND
ATTEN SW
GND
Rx IN
GND
Tx OUT
GND
GND
VCC LO
CHIP EN
J7
LNA OUT
J6
RxRF IN
2.45GHz
J5
TxRF OUT
2.45GHz
J1
LNA IN
J2
Rx OUT
350MHz
J3
Tx IN
350MHz
J4
LO 2.1GHz
JP1
S1
S2
S3
C17
10uF
C15
.1uF
L7
1.2nH
C14
100pF
L6
2.7nH
C12
100pF
C13
33pF
C1
1pF
L1
3.9nH
L2
39nH
L3
33nH
C16
100pF
C2
SEL
(0pF–1.0pF)
C3
10pF
C5
SEL
(0pF–1.0pF)
C6
10pF
C4
3.9pF
C9
8.2pF
C10
100pF
L4
33nH
C8
8.2pF
C7
100pF
L5
2.7nH
C11
1.0pF
VCC
SR01758

Figure 19.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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