DATA SHEET

HTRC110
Hitag Reader Chip

Product Specification (Rev. 1.1)

December 1997

Philips
Semiconductors

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CONTENTS

1 FEATURES

Combines all analogue RFID reader hardware in a single chip

· Optimized for HITAG transponder family

· Robust antenna coil power driver stage with modulator

· High performance adaptive sampling time AM/PM demodulator (patent pending)

· Read and write function

· On-chip clock oscillator

· Antenna rupture and short circuit detection

· Low power consumption

· Very low power stand-by mode

· Low external component count

· Small package (SO14)

2 GENERAL DESCRIPTION

The Hitag Reader Chip HTRC110 is intended for use with transponders which are based on the HITAG silicon (HT1ICS30 02x or HT2ICS20 02x). (E.g. the HITAG 2 stick HT2DC20 S20 may be operated with the use of the Reader Chip). In addition the IC supports other 125kHz transponder types using amplitude modulation for the write operation and AM/PM for the read operation. The receiver parameters (gain factors, filter cutoff frequencies) can be optimized to system and transponder requirements. The HTRC110 is designed for easy integration into RF-identification readers. State-of-the-art technology allows almost complete integration of the necessary building blocks. A powerful antenna driver/modulator together with a low-noise adaptive sampling time demodulator, programmable filters/amplifier and digitizer build the complete transceiver unit, required to design high-performance readers. A three-pin microcontroller interface is employed for programming the HTRC110 as well as for the bidirectional communication with the transponders. The three-wire interface can be changed into a two-wire interface by connecting the data input and the data output.

Tolerance dependent zero amplitude modulation caused severe problems in envelope detector systems, resulting in the need of very low tolerance reader antennas. These problems are solved by the new Adaptive Sampling Time technique (AST).

3 ORDERING INFORMATION

TYPE NAME	DESCRIPTION	ORDERING NUMBER
HTRC110 01T/02EE	Hitag Reader IC, Tube	9352 600 91112
HTRC110 01T/03EE	Hitag Reader IC, Reel	9352 600 92118

4 BLOCK DIAGRAM

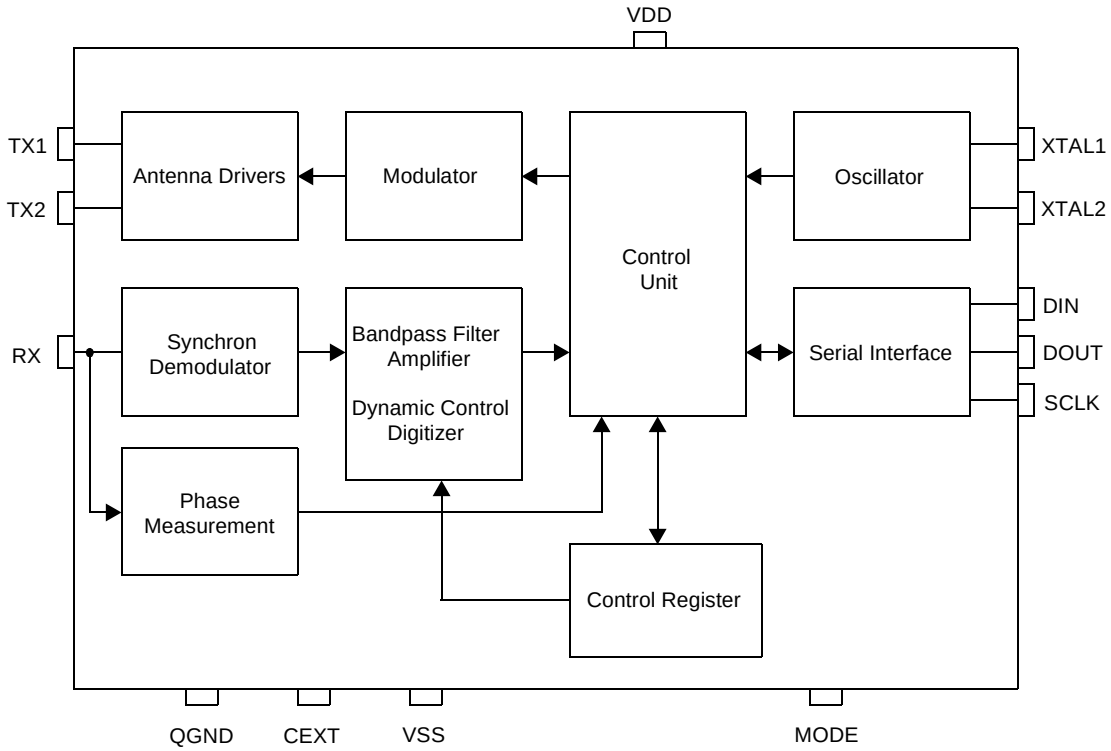


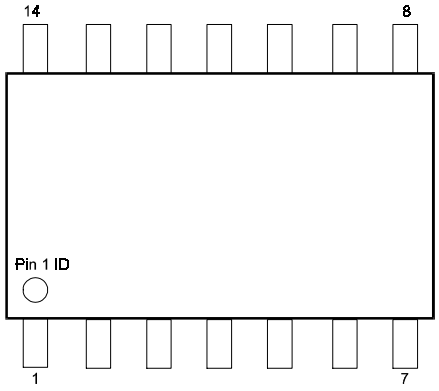
Fig.1 Block diagram Hitag Reader Chip HTRC110

5 KEY DATA

Supply VDD	5 V ±10%
Clock/Osc. frequency	4,8,12,16 MHz programmable
	(antenna carrier frequency 125 kHz)
Antenna driver current	200 mA_p continuous
Serial interface	CMOS compatible
Package	SO14
Operation temperature range	-40°C to +85°C

6 PINNING INFORMATION

6.1 Pinning Diagram



6.2 Pin Description

Number	Symbol	Description
1	VSS	GND, negative supply input
2	TX2	Coil driver output
3	VDD	Stabilized 5 V supply input
4	TX1	Coil driver output
5	MODE	To enable filtering of SCLK and DIN (for active antenna applications)
6	XTAL1	Oscillator interface, input
7	XTAL2	Oscillator interface, output
8	SCLK	Microcontroller interface: serial clock input
9	DIN	Microcontroller interface: serial data in
10	DOUT	Microcontroller interface: serial data out
11	n.c.	Not connected
12	CEXT	High pass filter coupling
13	QGND	Analog ground bias
14	RX	Demodulator input

7 MINIMUM APPLICATION CIRCUITRY

The following figure shows a minimal application circuitry for the HTRC110. The reader coil L_a together with the capacitor C_a forms a series resonant LC circuit (f = 125 kHz). The high voltages in the LC circuit are divided to safe operating levels by R_v and the chip internal resistor R_{dem_in} behind the RX-pin. The two capacitors connected to XTAL1 and XTAL2 shall be the recommended values and types from the crystal's data sheet. Alternatively to a crystal a ceramic resonator can be used or an external clock source can be connected to XTAL1.

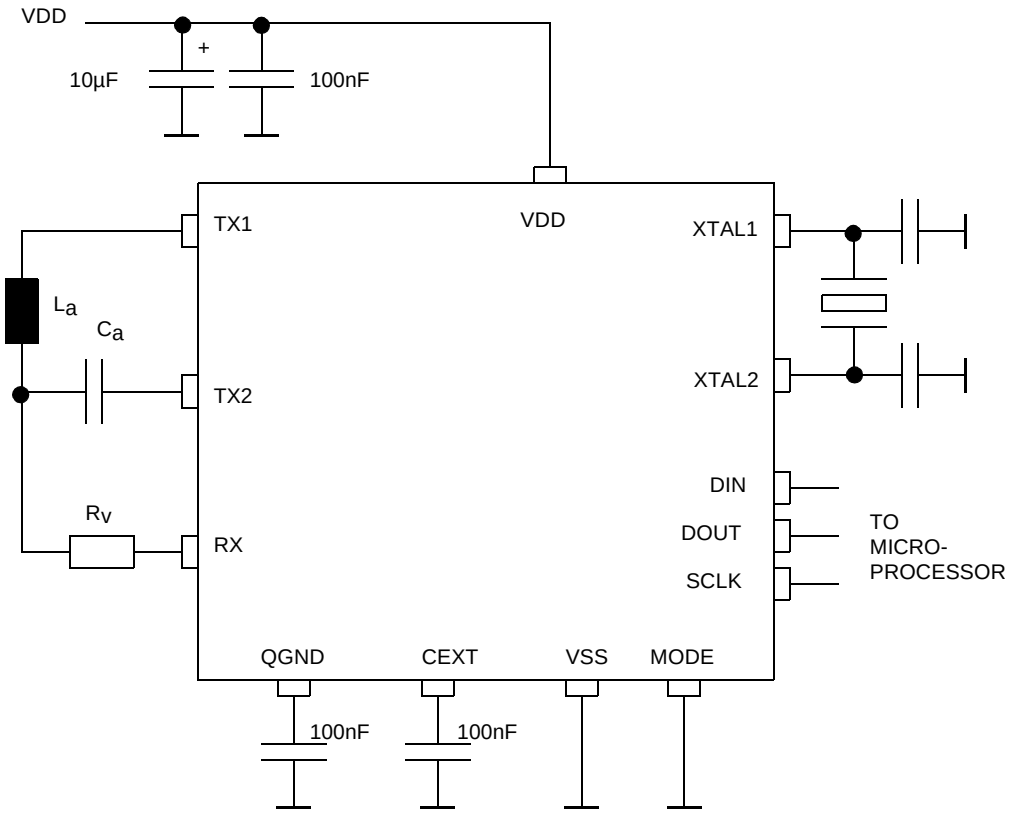


Fig.2 Minimum application circuitry

8 FUNCTIONAL DESCRIPTION

8.1 Power Supply

The HTRC110 works with an external 5V±10% power supply at VDD. The maximum DC-current is 10mA+$\hat{I}_{ant}$*2/π = 137mA. For optimum performance, the power supply connection should be bypassed to ground with a 100nF capacitor close to the IC.

8.2 Antenna Drivers, Data Input

The drivers deliver a square shaped voltage to the series resonant antenna circuit. Due to the full bridge configuration of the drivers this voltage U_{drvpp} is approximately 10V (peak-peak) corresponding to $\hat{U}_{drv}$=5V. The current flowing through the antenna is sine shaped. It´s amplitude is approximately:

$$\hat{I}_{ant} = \frac{4}{\pi}\frac{\hat{U}_{drv}}{R_{ant}} \quad \Leftrightarrow \quad I_{ant_{rms}} = \frac{\hat{I}_{ant}}{\sqrt{2}}$$

8.3 Diagnosis

In order to detect an antenna short or open condition the antenna tap voltage is monitored. An antenna fail condition is reported in the status bit ANTFAIL (see Table 14), if the antenna tap voltage does not go more negative than the diagnosis level DLEV (see Table 16). This condition is checked for every coil driver cycle.

8.4 Oscillator / Programmable Divider / Clock

The crystal oscillator at XTAL1/2 works with either crystal or ceramic resonators. It delivers the input clock frequency of 4,8,12 or 16 MHz. The oscillator frequency is divided by a programmable divider to obtain the carrier frequency of 125 kHz (see Table 10).

Alternatively, an external clock signal (CMOS compatible) may be fed into the IC via XTAL1. For example, this signal can be derived from the microcontroller clock.

8.5 Adaptive Sampling Time Demodulator

The demodulator senses the absorption modulation applied by a transponder when inserted into the field. The signal is picked up at the antenna tap point between L_a and C_a. It is divided by R_v and the internal resistor R_{dem_in} to a level below 8V (peak) with respect to QGND at the RX-pin (see Fig.2). Internally the signal is filtered with a second order low pass filter.

The antenna current and therefore the tap voltage is modulated by the transponder in amplitude and/or phase. This signal is fed into a synchronous demodulator recovering the baseband signal. The amplification and the bandpass filter edge frequencies of the demodulator can be adapted to different transponders via settings in the configuration pages.

The phase between the driver excitation signal and the antenna tap voltage depends on the antenna tuning. With optimum tuning, the phase of the antenna tap voltage is 90 degrees off the antenna driver signal. Detuning of the antenna resonant circuit results in a change of this phase relationship.

The HTRC110's built-in phase measurement unit allows the measurement of this phase relationship with a resolution of 360^o/64=5.625^o. This can be used to compute a sampling time that compensates the mistuning of the reader antenna. The phase measurement procedure can be carried out

- either once before the first communication starts, if the position of the transponder does not change with the respect to the reader antenna
- or during the communication (after sending the write pulses and before receiving the answer of the transponder), if the tag is moving.

Before the system is switched into WRITE_TAG-mode, the demodulator has to be frozen. This is internally done by clamping the input of the amplifier/filter unit to QGND. Doing so avoids large transients in the amplifier and the digitizer, which could affect settling times. In addition to the clamping, there exist other means in the HTRC110 which allow further reduction of the settling times. All the parts of the circuitry, which are associated with these functions, are controlled by the FREEZE0, FREEZE1 and THRESET bits, which are located in configuration page 2.

For more details concerning WRITE Timing, Demodulator Setting, Power Up Sequence, etc. please refer to the HTRC110 application note.

8.6 Idle and Power-down Mode

The HTRC110 can be switched into idle mode via setting the PD-bit and resetting the PD_MODE-bit. In this idle mode, only the oscillator and a few other system components are active.

It is also possible to switch the IC completely off. This is achieved by the power-down mode (PD=1, PD_MODE=1). Within this mode also the clock oscillator is switched off. This reduces the supply current of the HTRC110 to less than 20µA.

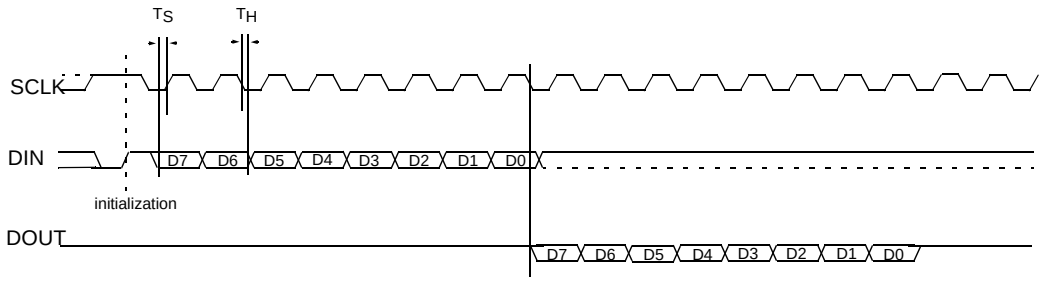
8.7 Serial Interface

The communication between the HTRC110 and the microcontroller is done via a three wire digital interface. The interface is operated by the following signals:

SCLK	Clock
DIN	Data Input
DOUT	Data Output

SCLK and DIN are realized as Schmitt-Trigger inputs. DOUT is an open drain output with internal pullup resistor.

Every communication between HTRC110 and microcontroller begins with an initialization of the serial interface. The interface initialization condition is a low-to-high transition of the signal DIN while SCLK is high.



All commands are transmitted to the HTRC110 serial interface starting with Most Significant Bit (MSB). DIN and DOUT are valid when SCLK is high.

8.7.1 Glitch Filter for Increased Noise/Interference Immunity

Connecting Pin 5 (MODE) to VDD enables digital filtering of the SCLK and the DIN input signals. This mode offers improved immunity against glitches on these interface signals. It is intended to be used in the so called “Active Antenna Applications” where the microcontroller and the reader communicate via long signal lines (e.g. 1 meter).

In other applications Pin 5 (MODE) has to be connected to GND.

Please refer to the HTRC110 application note for a detailed description of this feature.

9 COMMANDS

Table 1 depicts the HTRC110 command set summary.

Table 1:

Bit No. / Command Name	7 MSB	6	5	4	3	2	1	0 LSB	Remark
GET_SAMPLING_TIME	0	0	0	0	0	0	1	0	8 bit resp. (0 0 D5-D0)
GET_CONFIG_PAGE	0	0	0	0	0	1	P1	P0	8 bit resp. (X3-X0 D3-D0)
READ_PHASE	0	0	0	0	1	0	0	0	8 bit resp. (0 0 D5 - D0)
READ_TAG	1	1	1	-	-	-	-	-	READ_TAG-mode
WRITE_TAG_N	0	0	0	1	N3	N2	N1	N0	WRITE_TAG-mode with pulse width programming
WRITE_TAG	1	1	0	-	-	-	-	-	WRITE_TAG-mode
SET_CONFIG_PAGE	0	1	P1	P0	D3	D2	D1	D0	4*4 config bits available
SET_SAMPLING_TIME	1	0	D5	D4	D3	D2	D1	D0	

9.1 READ_TAG

This command is used to read the demodulated bit stream from a transponder: After the assertion of the three command bits the HTRC110 instantaneously switches to READ_TAG-mode and transmits the demodulated, filtered and digitized data from the transponder. Data comes out and should be decoded by the microcontroller. READ_TAG-mode is terminated by a low to high transition at SCLK.

Table 2:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	1	1	-	-	-	-	-	received data available at DOUT

9.2 WRITE_TAG_N

This command is used to write data to a transponder.

If N3-N0 are set to zero, the signal from DIN is transparently switched to the drivers. A high level at DIN corresponds to antenna drivers switched off, a low level corresponds to antenna drivers switched on.

If any binary number between 1 and 1111 is loaded into N3-N0 the drivers are switched off at the next positive transition of DIN. This state is held for a time interval equal to N * T_0 (T_0=8µs). This method relaxes the timing resolution requirements to the microcontroller and to the software implementation while providing an exact, selectable write pulse timing. WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK.

Table 3:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	1	N3	N2	N1	N0	no response

9.3 WRITE_TAG

This is the 3 bit short form of the previously described command WRITE_TAG_N. It allows to switch into WRITE_TAG-mode with a minimum communication time.

The behaviour of the WRITE_TAG command is identical to WRITE_TAG_N with two exceptions:

WRITE_TAG-mode is entered after assertion of the 3rd command bit.
No N parameter is specified with this command; instead the N value which was programmed with the most recent WRITE_TAG_N command is used. If no WRITE_TAG_N was issued so far, a default N=0 (transparent mode) will be assumed.

Table 4:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	1	0	-	-	-	-	-	no response

9.4 READ_PHASE

This command is used to read the antenna´s phase, which is measured at every carrier cycle.
The phase is coded binary in D5-D0.

Table 5:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	1	0	0	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.5 SET_SAMPLING_TIME

This command specifies the demodulator sampling time t_s. The sampling time is coded binary in D5-D0.

Table 6:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	1	0	D5	D4	D3	D2	D1	D0	no response

9.6 GET_SAMPLING_TIME

This command is used to read back the sampling time t_s set with SET_SAMPLING_TIME. The sampling time is coded binary in D5-D0.

Table 7:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	0	1	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.7 SET_CONFIG_PAGE

This command is used to set the amplifier and filter parameters (cutoff frequencies, gain factors) and the different operation modes. P1 and P0 select one of four configuration pages.

Table 8:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	1	P1	P0	D3	D2	D1	D0	no response

Table 9:

Bit No. / Command/Page No.	P1	P0	D3	D2	D1	D0
SET_CONFIG_PAGE 0	0	0	GAIN1	GAIN0	FILTERH	FILTERL
SET_CONFIG_PAGE 1	0	1	PD_MODE	PD	HYSTERESIS	TXDIS
SET_CONFIG_PAGE 2	1	0	THRESET	ACQAMP	FREEZE1	FREEZE0
SET_CONFIG_PAGE 3	1	1	DISLP1	DISSMART-COMP	FSEL1	FSEL0

Table 10:

Bit name	Description	Initial condition	
FILTERL	main low pass cutoff frequency	0	0: fL = 3 kHz 1: fL = 6 kHz
FILTERH	main high pass cutoff frequency	0	0: fH = 40 Hz 1: fH = 160 Hz
GAIN0	amplifier_0 gain factor	0	0: $gain_0$ = 16; 1: $gain_0$ = 32
GAIN1	amplifier_1 gain factor	1	0: $gain_1$ = 6.22; 1: $gain_1$ = 31.5
TXDIS	disable coil driver	0	0: coil driver active 1: coil driver inactive
HYSTERESIS	data comparator hysteresis	0	0: hysteresis OFF 1: hysteresis ON
PD	power down mode enable	0	0: device active 1: device power down
PD_MODE	select power down mode	0	0: idle mode 1: power down
FREEZE0	facility to achieve fast settling times	0	see table 11
FREEZE1	facility to achieve fast settling times	0	see table 11
ACQAMP	store signal amplitude as reference for later amplitude comparison	0	see status bit AMPCOMP
THRESET	reset threshold generation of digitizer	0	
FSEL0 FSEL1	clock frequency select LSB clock frequency select MSB	0 0	00: 4MHz, 01: 8MHz 10: 12MHz, 11: 16MHz
DISSMARTCOMP	disable smart comparator	0	0: smart comparator = ON 1: smart comparator = OFF
DISLP1	disable low pass 1	0	0: low pass = ON 1: low pass = OFF

Table 11: Freeze Bit Description

FREEZE1	FREEZE0	Meaning
0	0	normal operation
0	1	main low pass is frozen; main high pass is precharged to QGND
1	0	main low pass is frozen; time constant of main high pass is reduced by a factor of 16 for FILTERH=0 and by a factor of 8 for FILTERH=1
1	1	time constant for main high pass is reduced by a factor of 16 for FILTERH=0 and by a factor of 8 for FILTERH=1; second high pass is precharged

9.8 GET_CONFIG_PAGE

This command has three functions:

1. Reading back the configuration parameters set by SET_CONFIG_PAGE command
2. Reading back the transmit pulse width programmed with WRITE_TAG_N
3. Reading the system status information

P1 and P0 select one of four configuration pages. The response (X3 X2 X1 X0 D3 D2 D1 D0) contains the contents of the selected configuration page in its lower nibble. For P=0 or P=1 the higher nibble reflects the current setting of N (the transmit pulse width). For P=2 or P=3 the system status information is returned in the higher nibble.

Table 12:

Bit No.	7	6	5	4	3	2	1	0	Remark
Command	0	0	0	0	0	1	P1	P0	
Response	X3	X2	X1	X0	D3	D2	D1	D0	

Table 13:

Bit No. / Command/Page No.	7	6	5	4	3	2	1	0
GET_CONFIG_PAGE 0	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 1	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 2	0 (RFU)	0 (RFU)	AMPCOMP	ANTFAIL	D3	D2	D1	D0
GET_CONFIG_PAGE 3	0 (RFU)	0 (RFU)	AMPCOMP	ANTFAIL	D3	D2	D1	D0

Table 14: Status Bit Description

Bit name	Meaning	
ANTFAIL	antenna failure	0: antenna ok 1: antenna failure
AMPCOMP	amplitude comparison result	When ACQAMP is set, the actual amplitude of the data signal is stored as reference. After resetting ACQAMP status bit AMP-COMP is set when the actual data signal amplitude is higher than the stored reference.

10 ABSOLUTE MAXIMUM RATINGS

Table 15 lists the limiting values. Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Table 15:

Parameter	Symbol	Min.	Max.	Unit
Voltage at any pin except RX		-0.3	+6.5	V
Voltage at any pin except RX		-0.3	VDD+0.3	V
Voltage at RX pin		-10	+12	V
Maximum junction temperature	T_j		140	°C
Storage temperature range	T_{store}	-65	+125	°C

11 DC CHARACTERISTICS

Table 16 lists the DC characteristics. All voltages are measured to V_{ss}, T_{amb} = -40°C to +85°C.

Table 16:

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply						
Supply voltage		VDD	4.5	5.0	5.5	V
Operating supply current	VDD=5.5V, I_{TX1}=I_{TX2}=0	I_{On}		4	10	mA
Idle current(1)	VDD=5.5V	I_{id}		0.2	0.4	mA
Power down current	VDD=5.5V	I_{pd}		7	20	µA
Drivers (TX1, TX2)						
Output peak-current	permanent	I_{ant}			200	mA_p
Output peak-current	1:4 On/off-ratio t_{on} < 400 ms	$I_{antPulse}$			400	mA_p
Output resistance	both drivers together			2.5	7	Ω
Demodulator Input						
Voltage range	U_{RX} with respect to QGND		-8		8	V
QGND Potential			0.35 VDD	0.42 VDD	0.5 VDD	V
Impedance		R_{dem_in}	17	25	33	kΩ
Diagnosis Level (DLEV)						
	U_{RX} with respect to QGND, VDD=5V	DLEV	-1.5	-1.15	-0.8	V
Digital Inputs						
Data input high voltage		V_{IH}	0.7 VDD		VDD+0.3 V	V
Data input low voltage		V_{IL}	- 0.3 V		0.3 VDD	V
Digital Outputs						
Output low	$I_{OL\ max}$ = +1mA	V_{OL}			0.4	V
Output drive capability	$V_{OL} \leq 0.4V$		1			mA

1. Power consumption of external quartz or any other external component is not included

12 AC CHARACTERISTICS

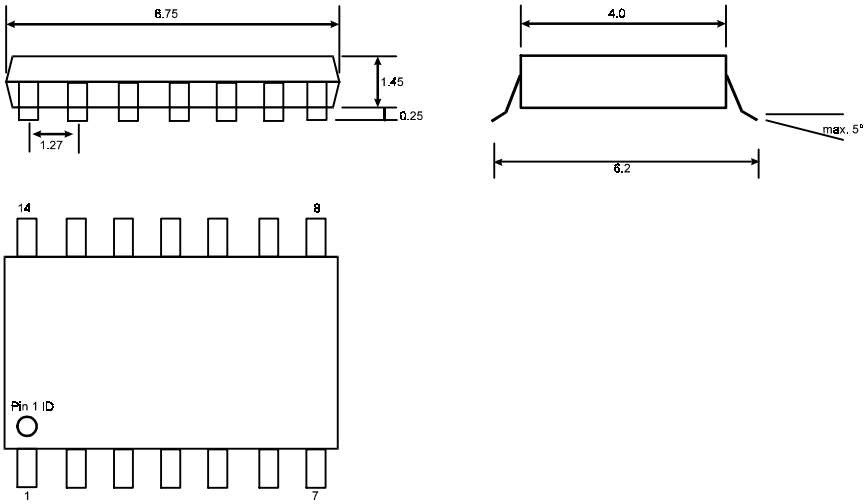
Table 17 lists the AC characteristics. T_{amb} = -40°C to +85°C.

Table 17:

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
XTAL Oscillator (XTAL1/XTAL2)						
Frequency range	depending on FSEL	f_{osc}	4		16	MHz
Start-up time				4	10	ms
Input capacitance	XTAL1			5		pF
Input resistance	XTAL1 to XTAL 2		0.9	1.3	3.0	MΩ
External Clock (XTAL1)						
Frequency range	depending on FSEL		4		16	MHz
Duty cycle			40		60	%
Serial Interface						
Setup time	MODE pin at V_{ss}	T_S	50			ns
Hold time	MODE pin at V_{ss}	T_H	50			ns
Receiver						
Sensitivity	at RX input	U_{RX}	2	1		mV_{pp}
Receiver delay	FILTERL=0	T_{RCV0}	290	310	340	µs
Receiver delay	FILTERL=1	T_{RCV1}	160	175	190	µs
Recovery from Clock Stable to Demodulator Valid						
Recovery time demodulator(1)		T_{RPD}			5	ms
Recovery from WRITE-pulse						
Recovery of demodulator(1)		T_{RWD}			500	µs
Recovery from AST-step						
Recovery of demodulator		T_{RAST}		0.7	1.5	ms
Phase measurement error					±5.7	deg

1. These short times require special command sequences. Please refer to the application note *AN97070 Read/Write Devices based on the HITAG Read/Write IC HTRC110.*

13 PACKAGE



14 DEFINITIONS

Amplitudes of sine shaped signals: $\hat{U}$, $\hat{I}$

Peak-to-peak of arbitrary shaped signals: U_{pp}, I_{pp}

Zero-to peak of arbitrary shaped signals: U_p, I_p

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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