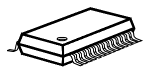
SIEMENS

GSM Receiver Circuit PMB 2402

Preliminary Data **Bipolar IC**

Features

- Heterodyne receiver with demodulator
- Down mixing from 900 MHz receiver band to the base band
- Demodulation and generation of I/Q-baseband components
- Low mixer noise 10 dB (SSB)
- Input high intercept point + 2 dB
- Integrated 0˚ and 90˚ phase shifter
- 82 dB AGC-range
- On-chip second LO-oscillator with external tuning circuit
- Two differential operational amplifiers
- Low power consumption due to highly flexible power-down capability
- Wide input frequency range up to 1 GHz
- Wide IF-range from 35 MHz to 100 MHz
- Wide output frequency range up to 13.5 MHz
- P-DSO-28-4 shrink package
- Temperature range – 25 ˚C to 85 ˚C



P-DSO-28-4

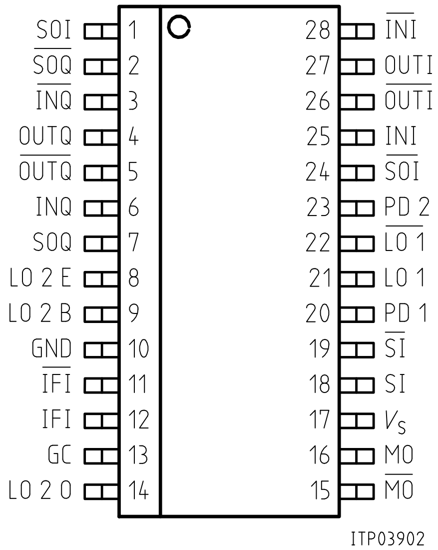
Applications

- Digital mobile cellular systems as GSM, DAMPS, JDC
- Various demodulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK
- Space and power saving optimizations of existing discrete demodulator circuits

Type	Version	Ordering Code	Package
PMB 2402S	V 2.1	Q67000-A6072	P-DSO-28-4 (Shrink, SMD))
PMB 2402S	V 2.1	Q67006-A6072	P-DSO-28-4 (Shrink, SMD, Tape + Reel)

Functional Description

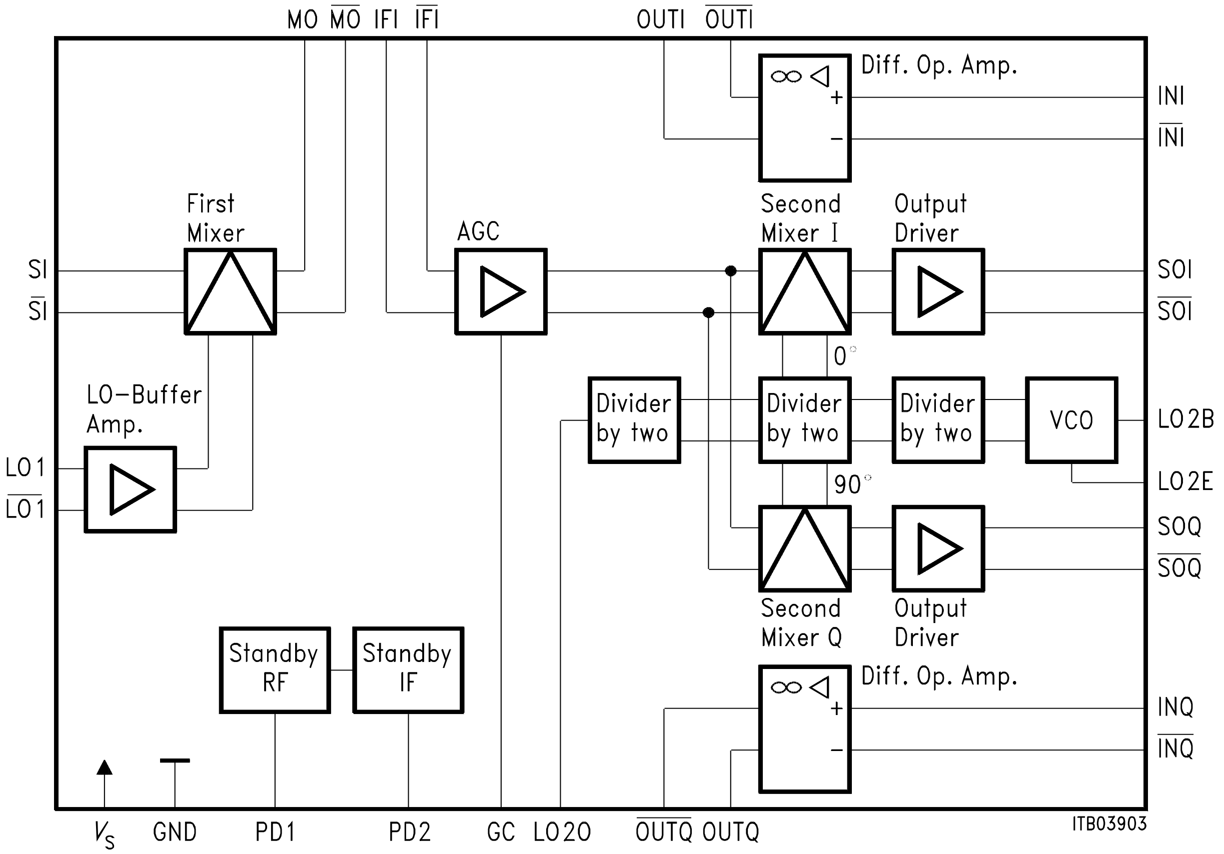
The PMB 2402 is a single-chip single-conversion heterodyn PM-receiver with phase shifting circuitry for the I/Q-phase baseband demodulation on chip. It also includes the second local oscillator, a gain controlled second IF-amplifier, two differential operational amplifiers for baseband filtering purposes and power down circuitry.
The PMB 2402 is designed for digital mobile telephones according to the GSM-standard and other digital systems.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	SOI	Non-inverting in-phase signal output
2	SOQ	Non-inverting quadratur signal output
3	$\overline{\text{INQ}}$	Inverting op. amp. signal output (Q)
4	OUTQ	Non-inverting op. amp. signal output (Q)
5	$\overline{\text{OUTQ}}$	Inverting op. amp. signal output (Q)
6	INQ	Non-inverting op. amp. signal intput (Q)
7	$\overline{\text{SOQ}}$	Inverting quadratur signal output
8	LO2E	External capacitors for oscillator
9	LO2B	VCO-tuning circuit
10	GND	Ground
11	$\overline{\text{IFI}}$	Inverting IF input
12	IFI	Non-inverting IF input
13	GC	Gain control input
14	LO2O	VCO-signal output
15	$\overline{\text{MO}}$	Inverted output of first mixer
16	MO	Non-inverted output of first mixer
17	V_S	Supply voltage
18	SI	Non-inverted signal input of first mixer
19	$\overline{\text{SI}}$	Inverted signal input of first mixer
20	PD1	Power-down input 1
21	LO1	Non-inverting input for first local oscillator
22	$\overline{\text{LO1}}$	Inverting input for first local oscillator
23	PD2	Power-down input 2
24	$\overline{\text{SOI}}$	Inverting in-phase signal output
25	INI	Non-inverting op. amp. signal input (I)
26	$\overline{\text{OUTI}}$	Inverting op. amp. signal output (I)
27	OUTI	Non-inverting op. amp. signal output (I)
28	$\overline{\text{INI}}$	Inverting op. amp. signal input (I)



Block Diagram

Circuit Description

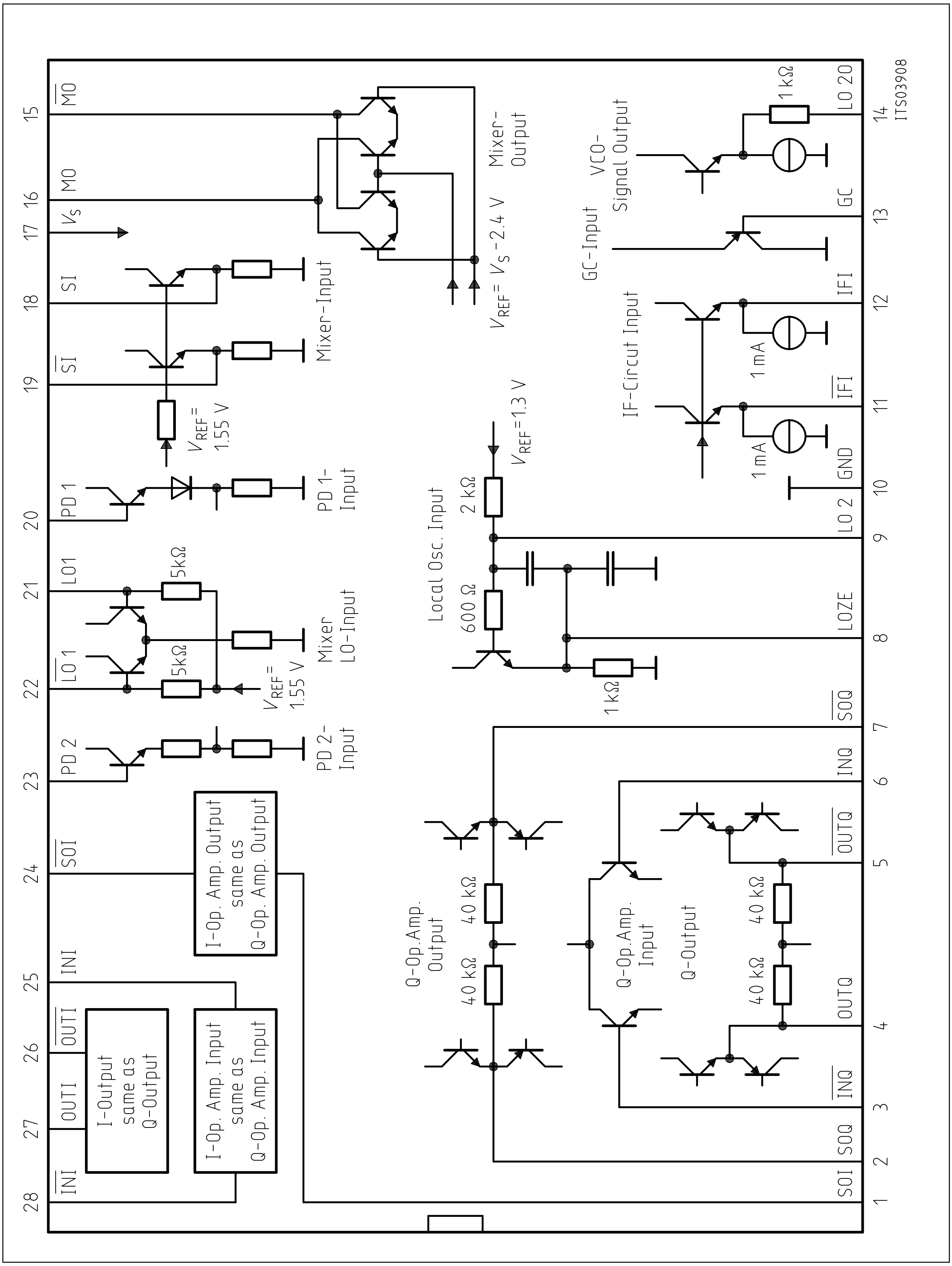
The input signal SI/$\overline{\text{SI}}$ and the amplified first local oscillator signal LO1/$\overline{\text{LO1}}$ are mixed down to an intermediate frequency (IF). The open collector output of the mixer generates a differential current at pins MO/$\overline{\text{MO}}$ which is filtered by an external resonant circuit. The resulting voltage drives an external SAW-filter.

The second local oscillator signal LO2 is generated in an on chip VCO and is fed to two dividers, which generate orthogonal signals at a quarter of VCO-frequency. The internal LO-signal is fed to an additionally divider, whose output signal LO2O is fed to the RF-signal of PLL-synthesizer. The filtered IF-signal reenters the chip at the IFI/$\overline{\text{IFI}}$ input, where it is amplified and demodulated to the final baseband output frequency with each of the orthogonal signals. The resulting in-phase and quadrature signals pass through differential output drivers and appear at SOI/$\overline{\text{SOI}}$ and SOQ/$\overline{\text{SOQ}}$ outputs, respectively. The amplification of the IF-signal before the second mixer stage is performed by a gain-controlled amplifier, the gain being determined by the voltage at the gain control input GC.

Two differential operational amplifiers with the input signals INI/$\overline{\text{INI}}$ (INQ/$\overline{\text{INQ}}$) and the output signals OUTI/$\overline{\text{OUTI}}$ (OUTQ/$\overline{\text{OUTQ}}$) can be used as active filters.

Differential signals and symmetrical circuitry are used throughout, except at the signal output. Bias drivers generate internal temperature- and supply voltage-compensated reference voltages required by various circuit blocks. Switching the power down inputs PD1 and PD2 from high to low (**see table**) sets the circuit from its normal operating mode into a mode with reduced supply current.

PD1	PD2	RF-Part	IF-Part	VCO/Divders
L	L	OFF	OFF	ON
L	H	OFF	ON	ON
H	L	ON	OFF	ON
H	H	ON	ON	ON



Internal Input / Output Circuits

Electrical Characteristics

Absolute Maximum Ratings

The maximum ratings may noy be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

T_A = – 25 ˚C to 85 ˚C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.5	7	V	
Input/output voltage (any except open collector)	V_{IO}	– 0.5 – 0.5	V_S + 0.5 7.5	V V	$V_S \leq 7$ V $V_S \leq 7$ V
Open collector output voltage (MO/$\overline{MO}$)	V_{OC}	– 0.5 – 0.5	V_S + 2.5 7.5	V V	$V_S \geq 5$ V $V_S \geq 5$ V
Differential input voltage (any differential input)	V_I	– 3	3	V	
Junction temperature	T_j		125	˚C	
Storage temperature	T_{stg}	– 55	125	˚C	
Thermal resistence (junction to ambient)	$R_{th\ JA}$		55	K/W K/W	PDSO-28 P-DSO-28-S

Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC-characteristics limits are not guaranteed.

V_S = 4.5 V to 5.5 V; T_A = – 25 °C to 85 °C; refer to test circuit 1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
SI/$\overline{\text{SI}}$ input level	P_{SI}		– 11	dBm	
SI/$\overline{\text{SI}}$ input frequency	f_{SI}		1000	MHz	
LO1/$\overline{\text{LO1}}$ input level	P_{LO1}	– 11	3	dBm	
LO1/$\overline{\text{LO1}}$ input frequency	f_{LO1}		1100	MHz	
Intermediate frequency	f_{IF}	35	100	MHz	
IFI/$\overline{\text{IFI}}$ input level	P_{IFI}		– 24	dBm	
IFI/$\overline{\text{IFI}}$ input frequency	f_{IFI}	35	100	MHz	
LO2 input level	P_{LO2}	– 20	0	dBm	VCO external
LO2 input frequency	f_{LO2}	140	400	MHz	
VCO frequency range	f_{VCO}	120	250	MHz	with ext. capacitors
LO2O output level	P_{LO2O}	120	180	mVpp	
LO2O output frequency	f_{LO2O}	15	50	MHz	
SOI/$\overline{\text{SOI}}$, SOQ/$\overline{\text{SOQ}}$ output Bandwidth	B_{SO}	0	13.5	MHz	– 3 dB roll off
GC input voltage	V_{GC}	0	2	V	
L-PD1/PD2 voltage	V_{PDL}	0	1	V	
H-PD1/PD2 voltage	V_{PDH}	4	V_S	V	

Note: Power levels are referred to resistance of 50 Ω

AC/DC Characteristics

AC/DC-characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

V_S = 4.75 to 5.25 V; T_A = 25 °C;

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current	I_S	3.1 12 11.5 20	5.5 15.5 15 24.5	6.8 19 18.5 30	mA mA mA mA	PD1 = L PD2 = L PD1 = L PD2 = H PD1 = H PD2 = L PD1 = H PD2 = L	1
First Mixer Signal Input SI/$\overline{\text{SI}}$							
Input resistance	R_{SI}	17	25	33	Ω		2a
Input inductance	L_{SI}	3.5	5	6.5	nH	In series to R_{SI}	2a
Max. input level	P_{SI}	– 13	– 11		dBm	1 dB compr. at MO/$\overline{\text{MO}}$	1
Input intercept Point	P_{IPI}	0	2	3	dBm	G_{MO} = 14 dB	1
Blocking level	P_B	– 16	– 14	– 12	dBm	3 dB attenuation of wanted Signal at MO	1
Input interference level at $f = f_{int}$	P_{int}	– 38			dBm	– 98 dBm interference at $f = (f_{int}$ +/– $f_{LO1})$ X2 at MO	3
Input frequency	f_{SI}			960	MHz		1
Noise figure	N_{SI} N_{SI}	7.5 9.5	8 10	9.5 11.5	dB dB	DSB-noise, f_C = 900 MHz SSB-noise, f_C = 900 MHz including optimum noise matching	1
Output of First Mixer MO/$\overline{\text{MO}}$ (open collector)							
Output resistance	R_{MO} R_{MO}	11.2 7	16 10	20.8 13	kΩ kΩ	f_{MO} = 45 MHz f_{MO} = 71 MHz	2c 2c
Output capacitance	C_{MO}	0.7	1	1.3	pF	parallel to R_{MO}	2c
Total output current	$I_{MO+\overline{MO}}$	3.5	5	6.5	mA		1
Power gain from Signal input	G_{MO}		13	14	dB		1
Intermediate frequency	f_{IF}	35		100	MHz		1

AC/DC-Characteristics (cont'd)

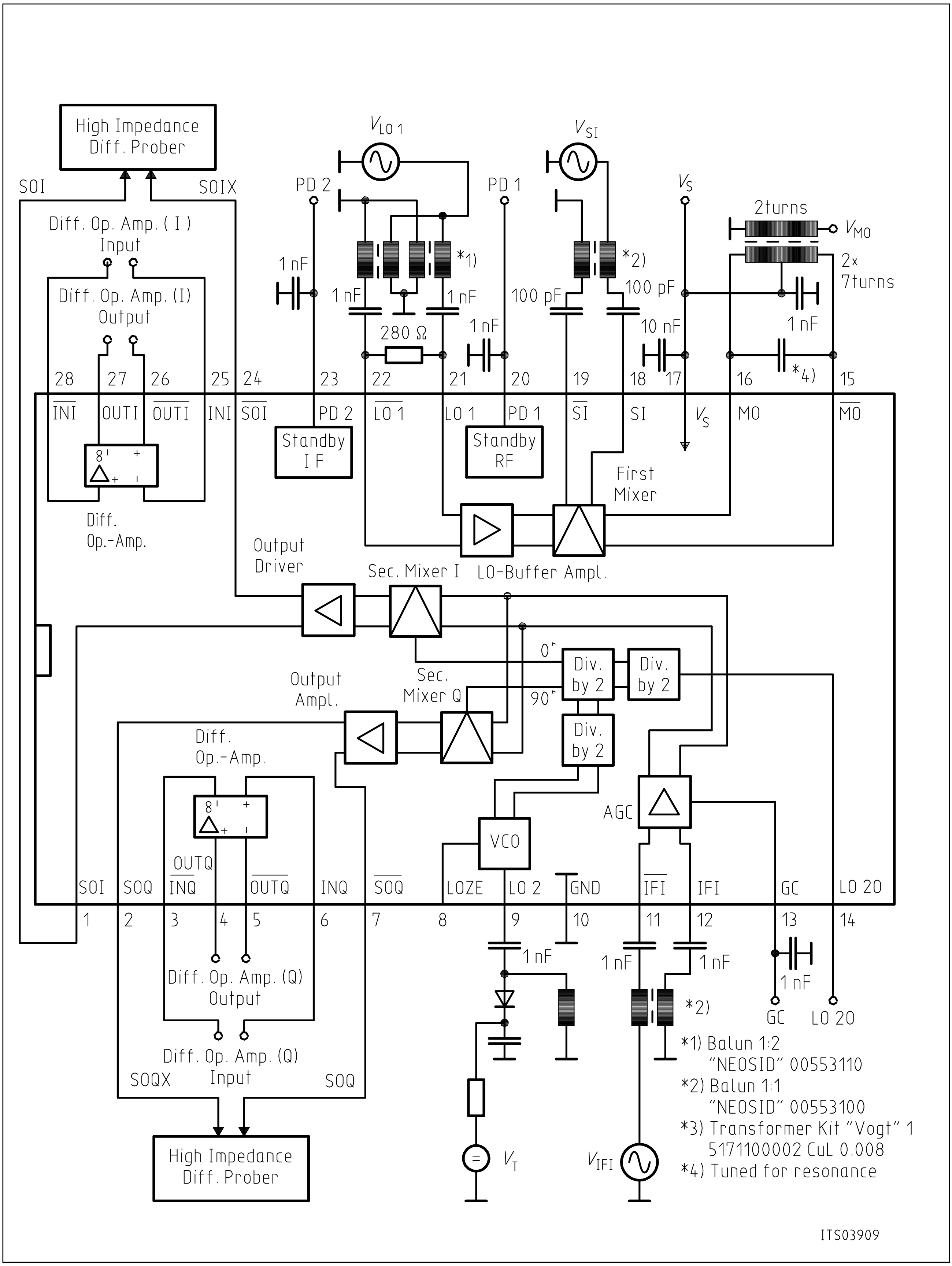
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input of First Mixer Local Oscillator LO1/$\overline{\text{LO1}}$							
Input resistance	R_{LO1}	490	700	910	Ω	f_{LO1} = 900 MHz	2a
Input capacitance	C_{LO1}	0.7	1	1.3	pF	parallel to R_{LO1}	2a
Input level	P_{LO1} V_{LO1}	– 11 178		3 890	dBm mVpp	**see diagram 1**	1 1
Input frequency	f_{LO1}			1100	MHz		1
Isolation of First Mixer							
From SI to MO	A_{SI-MO}	30			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
SI to LO1	A_{SI-LO1}	60			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
LO1 to MO	A_{LO1-MO}	50			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
LO1 to SI	A_{LO1-SI}	60			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
MO to Si	A_{MO-SI}	50			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
MO to LO1	A_{MO-LO1}	65			dB	f_{SI} = 945 MHz; f_{LO1} = 900 MHz	1
IF Input IFI/$\overline{\text{IFI}}$							
Input resistance	R_{IFI}	63	90	117	Ω		2a
Input capacitance	C_{IFI}	0.35	0.5	0.65	pF	parallel to R_{IFI}	2a
Max. input level	P_{IFI} V_{IFI}		– 17 89		dBm mVpp	V_{GC} = 2 V, 1 dB compr. at SO; **see diagram 4**	1 1
Input intercept point	P_{IPI}	**see diagram 5**					1
Input frequency	f_{SI}	35		100	MHz		1
Noise figure	N_{SI}	10	11	14	dB	SSB-noise	1
Input for Second Local Oscillator LO2 (VCO external)							
Input resistance	R_{LO2}	1.9 1.3	2.4 1.8	3.1 2.3	kΩ kΩ	f_{LO2} = 180 MHz f_{LO2} = 360 MHz	2b 2b

AC/DC-Characteristics (cont'd)

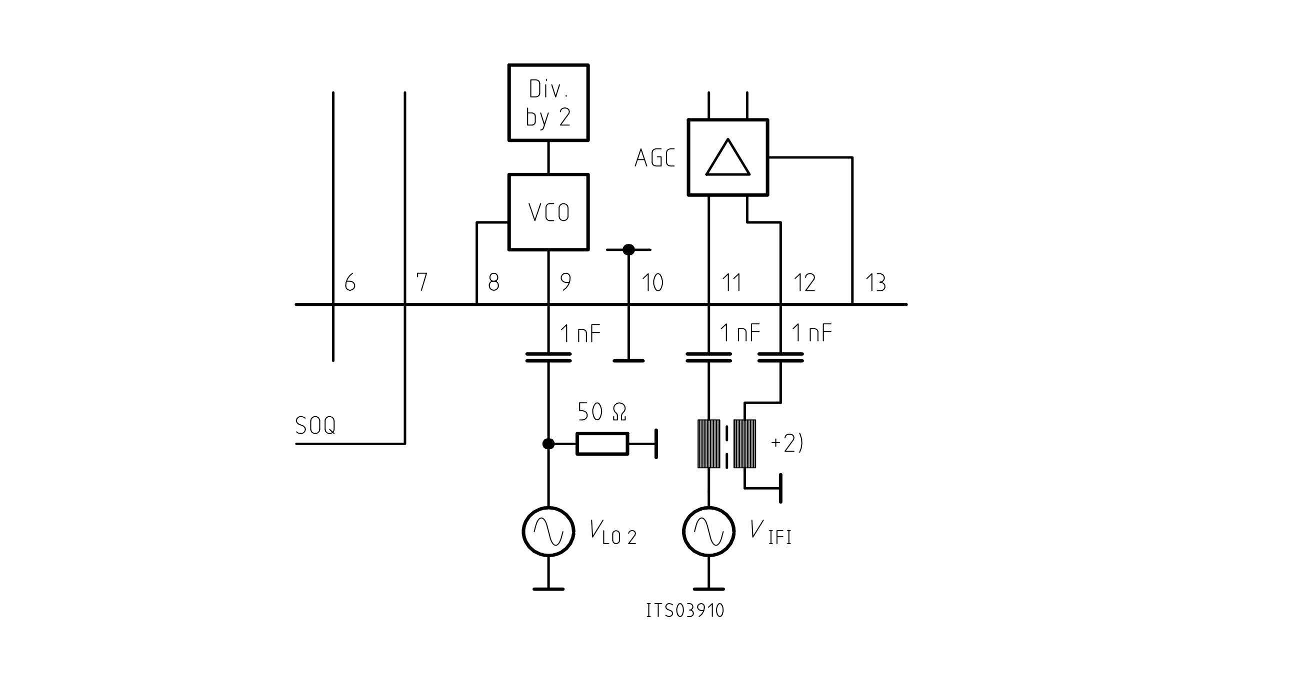
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input capacitance	C_{LO2}	0.7	1	1.3	pF		2b
Input level	P_{LO2} V_{LO2}	– 20 63		0 630	dBm mVpp	into 50 Ω	1.1 1.1
Input frequency	f_{LO2}	140		400	MHz		1.1
Voltage Controlled Oscillator VCO (LO2)							
VCO-frequency	f_{VCO}	120		250	MHz	with ext. capacitors	1.2
VCO Output LO2O							
Output resistance	R_{LO2O}	0.9	1.2	1.5	kΩ		
Output capacitance	C_{LO2O}	0.7	1	1.3	pF		
Output level	V_{LO2O}	150 120	160 140		mVpp mVpp	IF ≤ 75 MHz IF ≥ 75 MHz	1 1
Output frequency	f_{LO2O}	15		50	MHz		1
Signal Outputs SOI/$\overline{\text{SOI}}$, SOQ/$\overline{\text{SOQ}}$							
Output resistance	R_{SO}	175	250	325	Ω		
Output capacitance	C_{SO}	0.7	1	1.3	pF		
SO frequency roll off	f_{SO}		13.5		MHz	**see diagram 6**	
DC output level	V_{SO}	2.0		2.5	V		1
Diff. output offset voltage	$V_{SO/\overline{SO}}$			28	mV	between $I/\overline{I}$ or Q/$\overline{\text{Q}}$	1
Voltage gain from IF to I/Q-output	G_{SO}	57 – 25	61 – 21	65 – 17	dB dB	V_{GC} = 0 V **see dia-** V_{GC} = 2 V **gram 2 + 3**	1
Gain Control Input GC							
GC-input voltage	V_{GC}	0		2	V		1
GC-input current	$-I_{GC}$			1	µA	0 V ≤ V_{GC} ≤ 2 V	1
Gain control factor	F_{GC}		40		dB/V	$F_{GC} = dG_{SO}/dV_{GC}$ **see diagram 3**	1

AC/DC-Characteristics (cont'd)

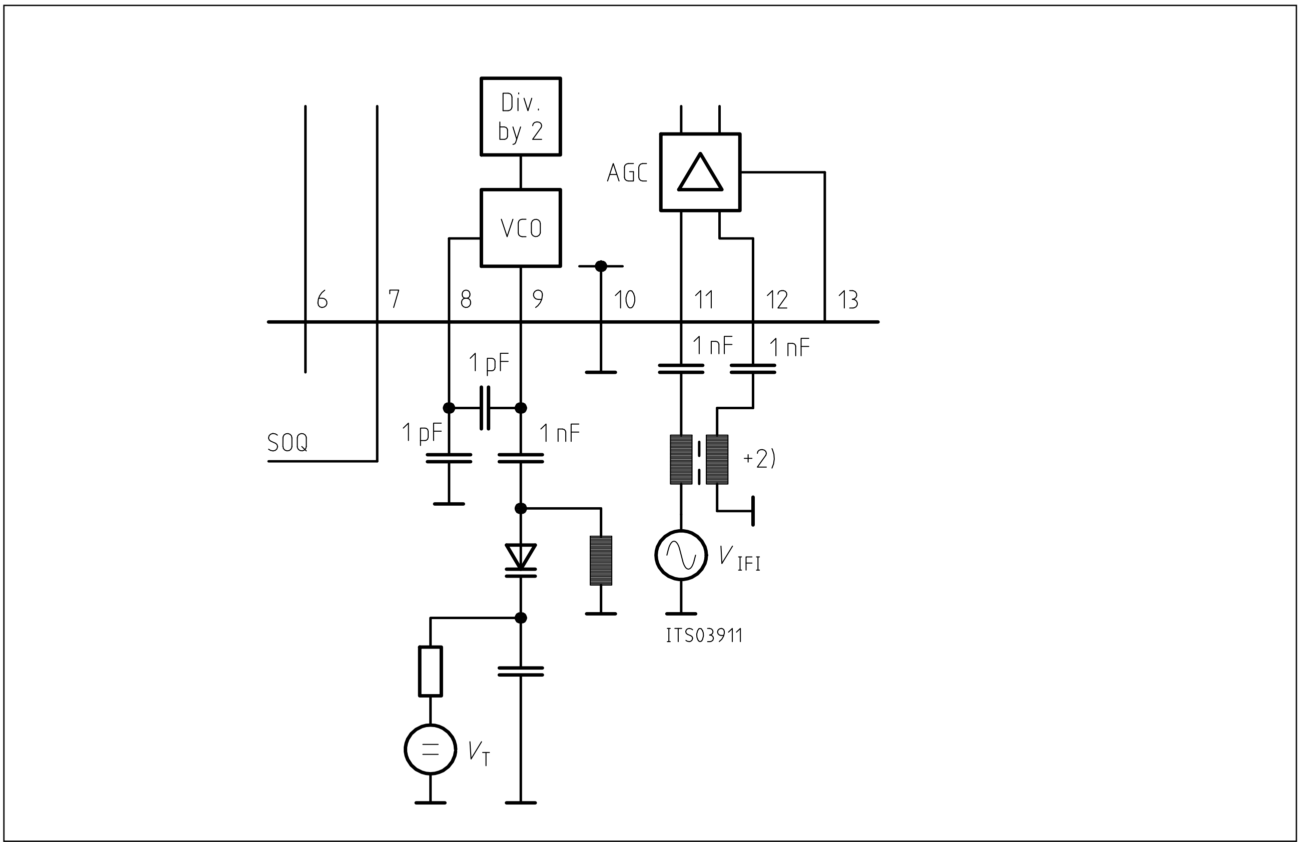
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Power-Down Inputs PD1, PD2							
L-PD input voltage	V_{PDL}	0		1	V		1
L-PD input current	I_{PD1L} I_{PD2L}			0.1 0.2	µA µA	$0 \leq V_{PD1, 2L} \leq 1$ V	1
H-PD input voltage	V_{PDH}	4		V_S	V		1
H-PD input current	I_{PDH}			10	µA	$4 \leq V_{PD1, 2L} \leq V_S$	1
Differential Operational Amplifier (open loop)							
Slew rate	SR		4.6		V/µs		1
Gain Bandwith Prod.	GBW		12		MHz		1
Voltage gain	A_{Vo}		55		dB		1
Phase margin	φ_R		60		degr.		1
Gain margin	A_R		14		dB		1
Common mode Rejection Ratio	$CMRR$		58		dB		1
Offset voltage	V_{OFF}		1		mV		1
Output voltage	V_{OUT}	0.8		V_S –1	V		1



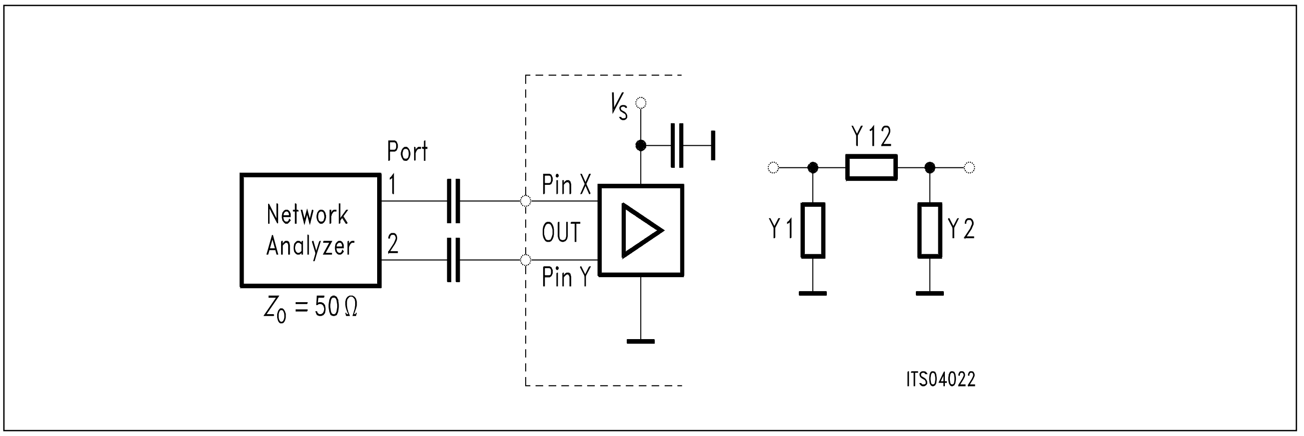
Test Circuit 1



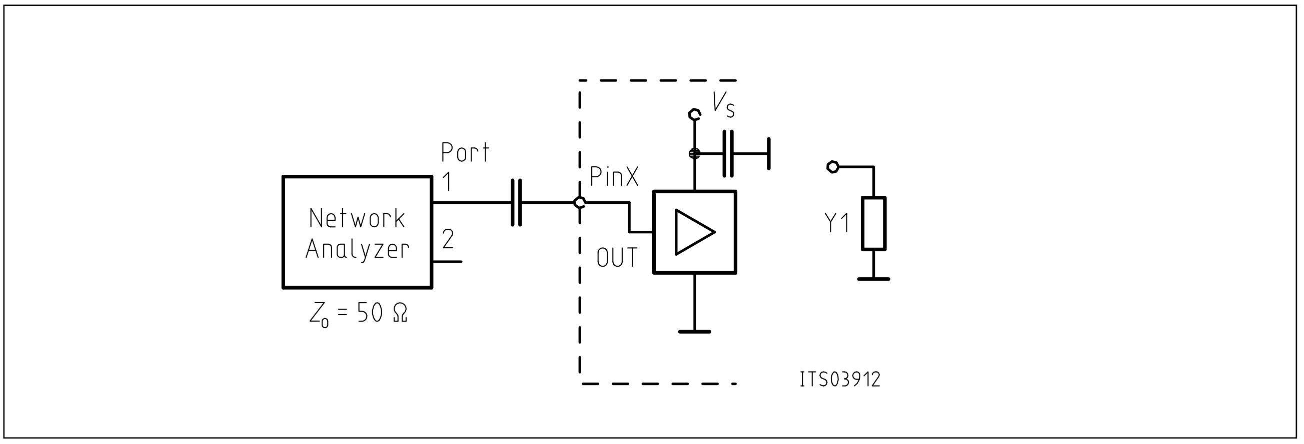
Test Circuit 1.1



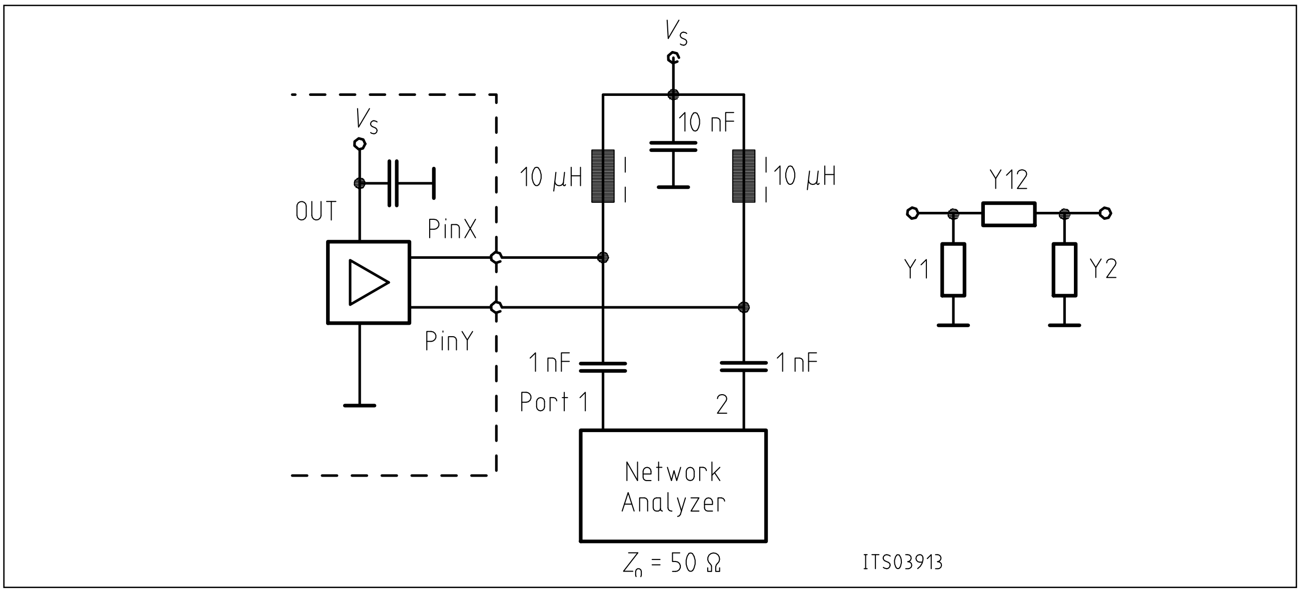
Test Circuit 1.2



Test Circuit 2a



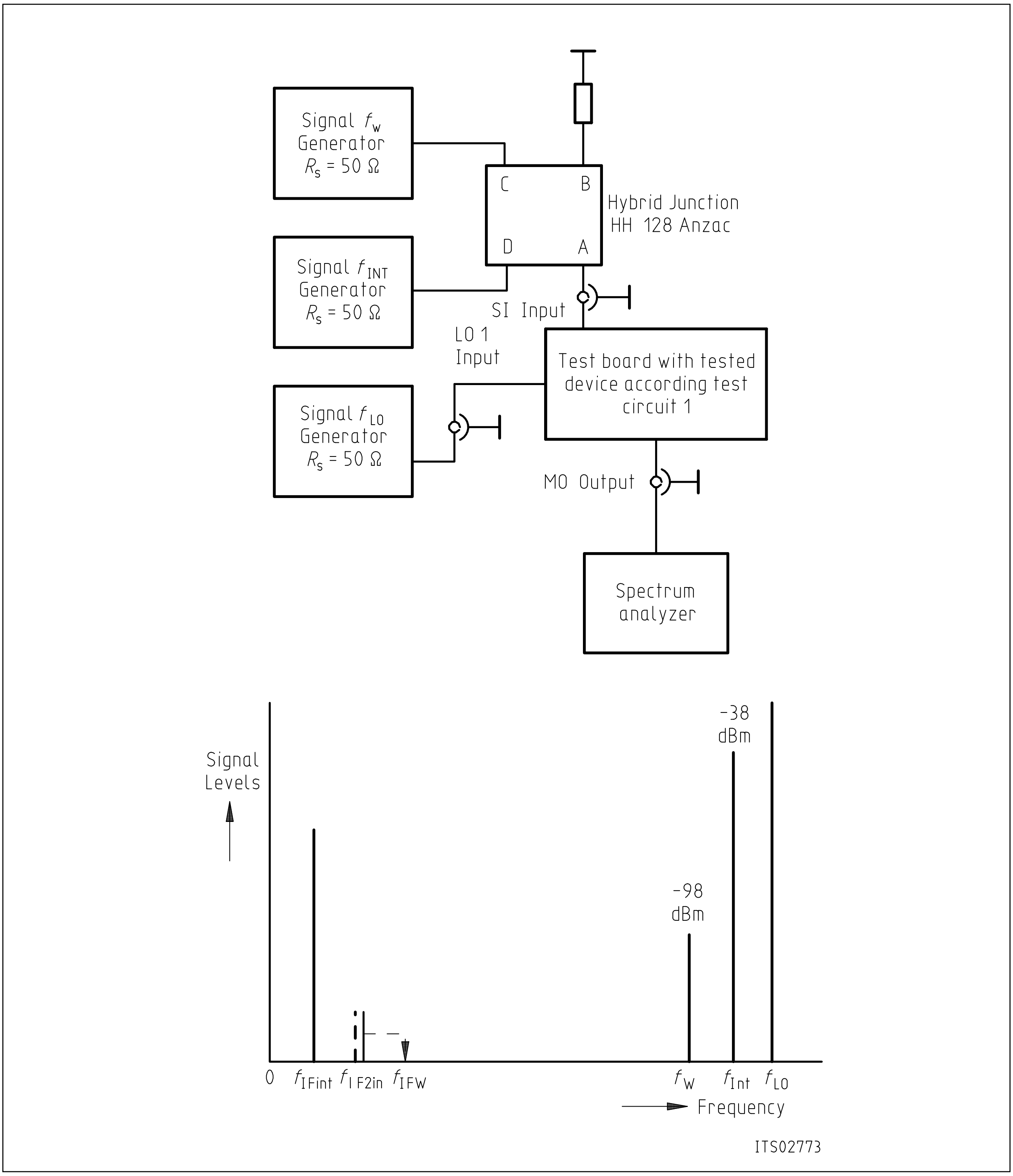
Test Circuit 2b



Test Circuit 2c

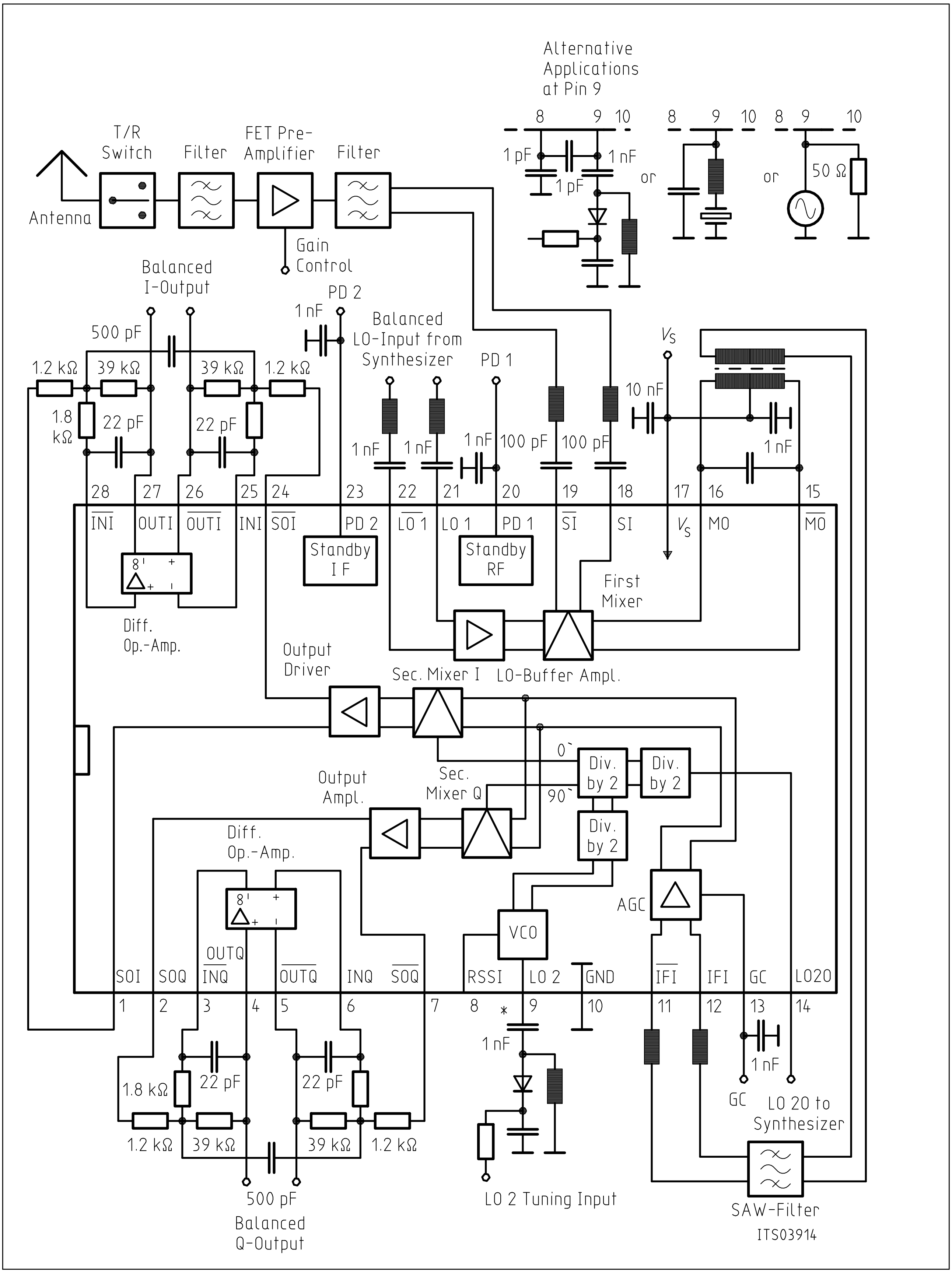
The S-parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base.

Test Point	Test Circuit	Test Frequency / MHz	Pin x	Pin y
LO1-input impedance	2a	900	21	22
SI-input impedance	2a	900	18	19
IFI-input impedance	2a	45 … 90	11	12
LO2-input impedance	2b	180, 360	9	–
MO-output impedance	2c	45, 71	15	16



Test Circuit 3

f_W = wanted input signal from received channel
f_{int} = unwanted interfering signal within band : $f_{int} = f_{LO} - f_{IF} / 2$
f_{LO} = local oscillator signal
f_{IFW} = wanted IF signal from received channel = $f_{LO} - f_W$
$f_{IFi t}$ = unwanted IF / 2 signal from interfering channel: $f_{IFint} = f_{LO} - f_{int}$
f_{IF2in} = unwanted harmonic signal of f_{IF2in} : $f_{IF2in} = 2 \times f_{IFint}$



Application Circuit

Diagram 1
First Mixer Gain versus LO-Level P_{LO1}
P_{SI} = – 40 dBm, f_{MO} = 45 MHz

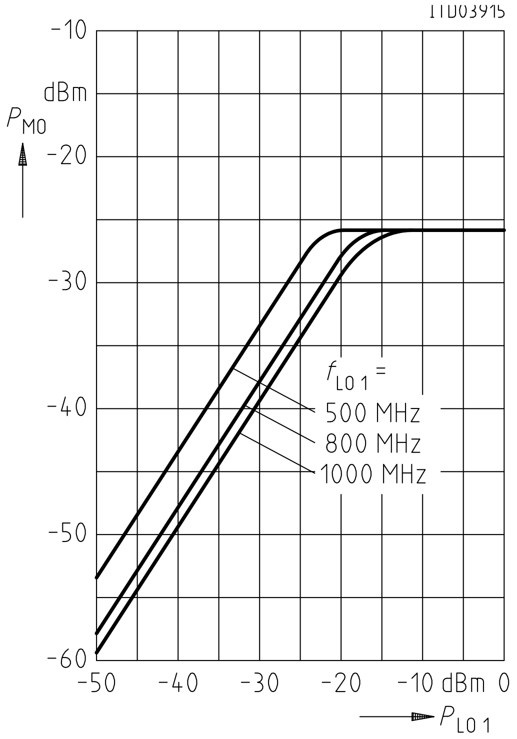


Diagram 2
Gain Control Characteristic Output Level P_{SO} versus input Level P_{IFI}

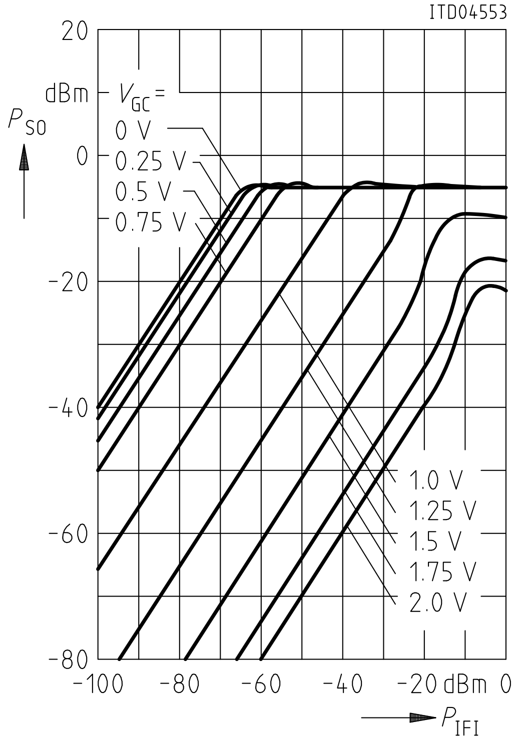


Diagram 3
Gain Control Characteristic Voltage Gain G_{SO} versus GC-Voltage V_{GC}

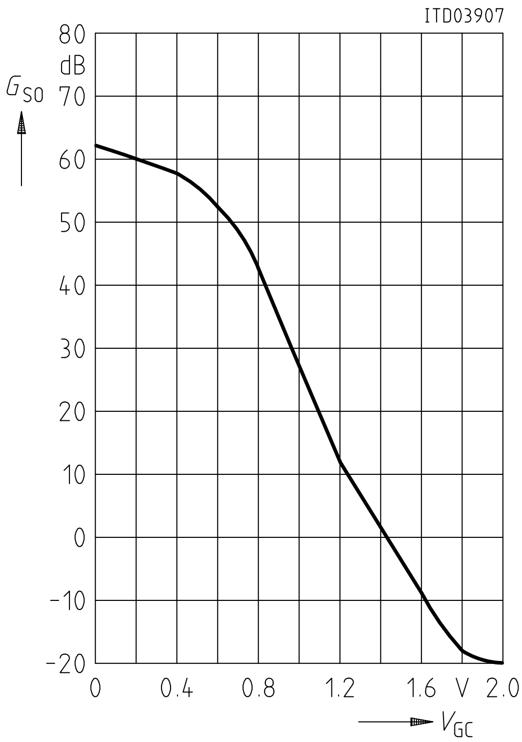


Diagram 4
Gain Control Characteristic
Max. Input Level P_{IFI} versus GC-Voltage V_{GC}:
(1 dB Compresion at SO)

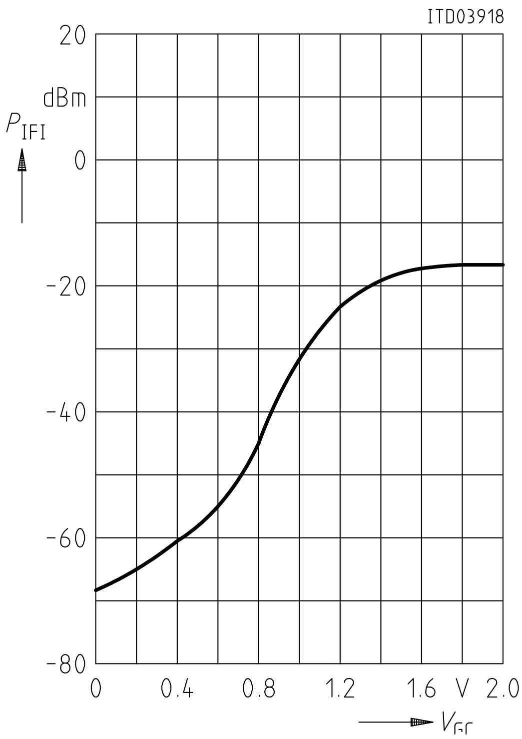


Diagram 5
Gain–Control Characteristic Input Intercept Point P_{IPI} versus GC-Voltage V_{GC}

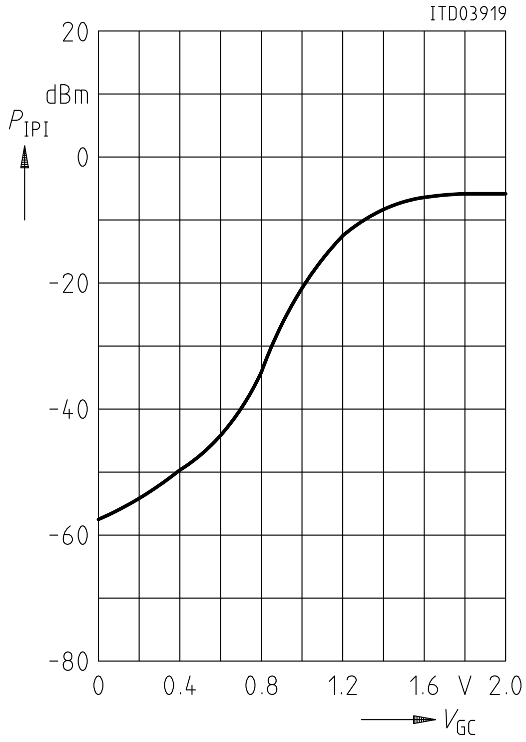
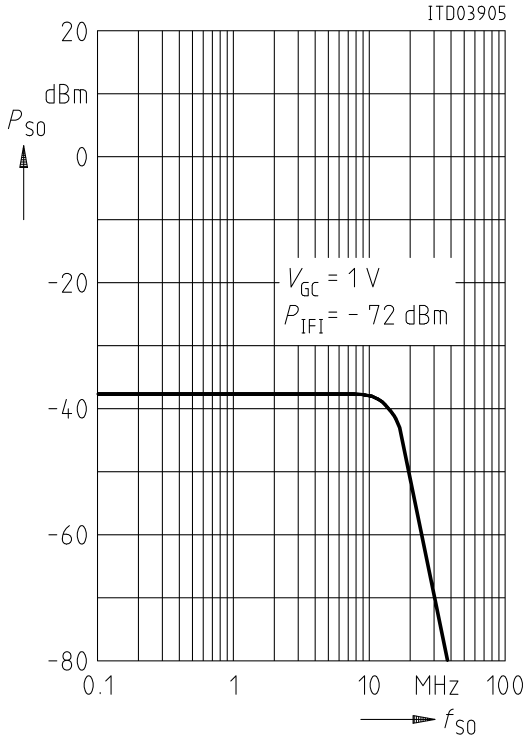
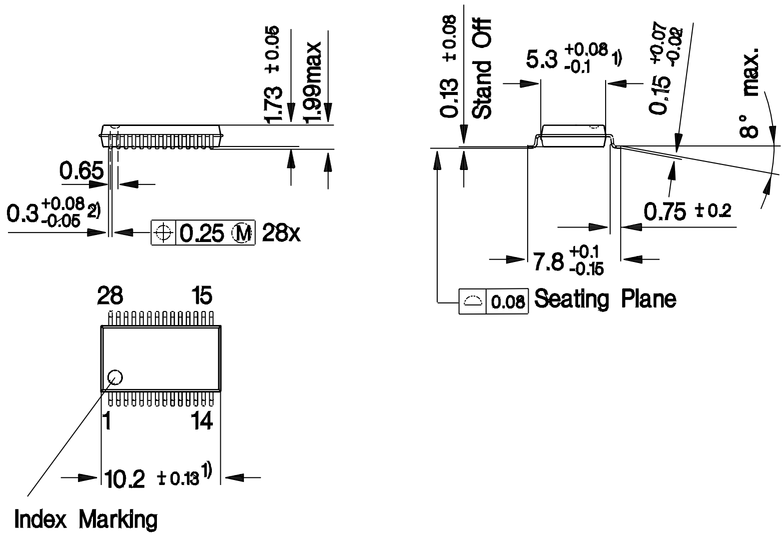


Diagram 6
Frequency Transfer Characteristic of Outputs SOI / SOQ



Package Outlines

Plastic-Package, P-DSO-28-4 (Shrink) (SMD)
(Dual-Small-Outlines)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Sorts of Packing
Package outlines for tubes, trays ect. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm