SIEMENS

PMB 2220

Version 2.2

1 Overview

Combined with a PLL (i.e. PMB 2306 or PMB 2307) and a power amplifier, the PMB 2220 device performs a complete DECT transmitter. Additionally, the phase locked loop can be switched to receive mode and be used as a local oscillator for the receive mixer.

P-SSOP-20-1

1.1 Features

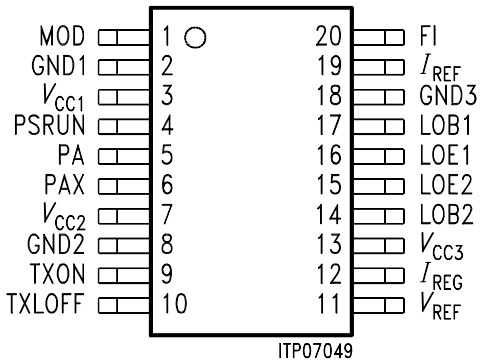
- Either **single VCO operation** (for receive and transmit) or **dual VCO operation** (VCO1 for receive and VCO2 for transmit) possible
- 64/65- prescaler on chip
- Frequency doubler for receive and transmit mode with balanced driver outputs
- Supply voltage regulator (with external pnp-transistor) for the two VCOs
- Power down for the inactive VCO
- Current reference output for PLL charge pump to get constant lock-in time
- Wide power supply range 3.0 ... 5.5 V, for 3 cell supply without external regulator

Type	Ordering Code	Package
PMB 2220	Q67000-A6079	P-SSOP-20-1

1.2 Pin Configuration

(top view)

P-SSOP-20-1



1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	MOD	Prescaler modulus control input (divider ratio 1:64 or 1:65)
2	GND1	
3	V_{CC1}	Supply voltage 1 (prescaler)
4	PSRUN	Test input for prescaler
5	PA	Frequency doubler signal output
6	PAX	Inverted frequency doubler signal output
7	V_{CC2}	Supply voltage 2 (bandgap and frequency doubler)
8	GND2	
9	TXON	Control input for VCO power down
10	TXLOFF	System power down control input
11	V_{REF}	Reference voltage for I_{REF}-current generation with external resistor to ground
12	I_{REG}	Base current for external supply voltage regulating pnp-transistor
13	V_{CC3}	Supply voltage 3 (regulated for VCO1 and VCO2)
14	LOB2	Base input of oscillator 2
15	LOE2	Emitter input of oscillator 2
16	LOE1	Emitter input of oscillator 1
17	LOB1	Base input of oscillator 1
18	GND3	
19	I_{REF}	Reference current for PLL charge pump
20	FI	Prescaler output

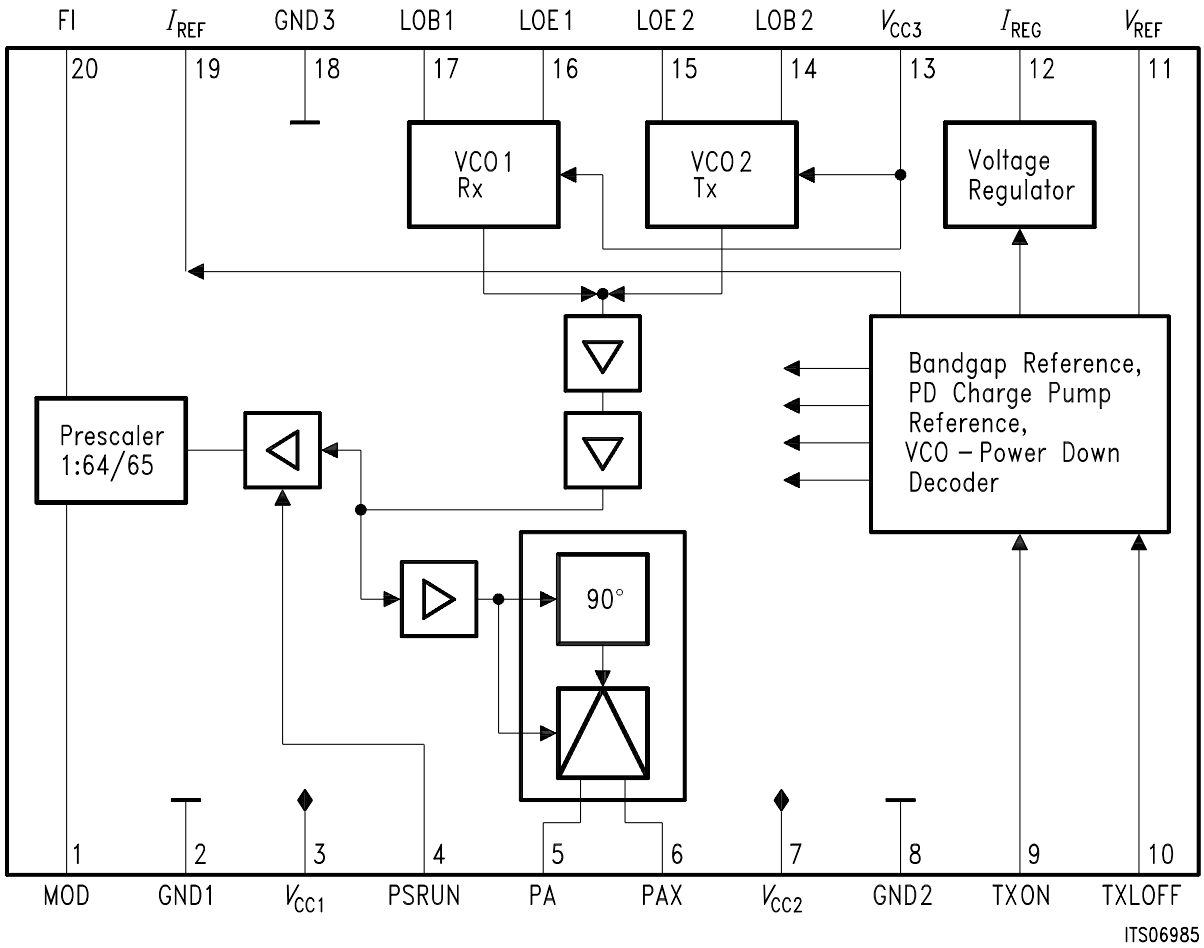


Figure 1
Block Diagram

2 Circuit Description

VCO1, VCO2

The signal TXON determines which one of the VCOs is active: Receive mode VCO1 with TXON logic LOW, transmit mode VCO2 with TXON logic HIGH. The other VCO is powered down.

Both VCOs are emitter coupled configurations (pins LOB1, LOE1 and LOB2, LOE2) with an external dielectric resonator connected to ground and a tuning diode in parallel. During the transmit timeslots the modulation can be done at the anode, the PLL loop being open.

The VCOs generate differential signals. Those of the active VCO are coupled to the prescaler and the doubler via an isolation amplifier.

Supply Voltage Regulator for the VCOs

With an external pnp-transistor the supply voltage of both VCOs is stabilized to 2.7 V in the specified general supply voltage range. This allows for a minimal frequency drift in spite of a ripple on the chip supply voltage. The emitter of the external transistor must be connected to V_{CC2}.

Phase Shifter, Frequency Doubler

Frequency doubling of the active differential VCO signal is performed by multiplying the signal with its quadrature component.

PD Charge Pump Reference

Pin I_{REF} functions as a current source for use in the charge pump of the PLL. The current is set by connecting pin V_{REF} (reference voltage) by a resistor to ground. This external resistor allows for a much smaller tolerance than would be feasible with an on-chip resistor.

Prescaler

The prescaler divides the signal frequency of the active VCO by a ratio of 1:64 (MOD high) or 1:65 (MOD low) and outputs it on pin FI.

The MOD input is TTL/CMOS compatible. The output is compatible to the CMOS frequency synthesizer family PMB 2306 / PMB 2307, with a minimum logic swing of 0.5 Vpp.

The supply V_{CC1} is used to feed the prescaler. Due to the internal interface V_{CC1} must be connected to V_{CC2}.

Summary of Function Modes

Power Down Operation

The following table shows the relation between the logic level of the inputs TXLOFF and TXON and the status of the different function blocks.

The “power down code” lists the logic levels of the inputs in the order TXLOFF, TXON.

L = logic LOW, H = logic HIGH
off: function block in power down mode or stand by
on: function block in normal operation

Function Blocks	Power Down Code (TXLOFF, TXON)		
	L, x	**H, L**	**H, H**
Bandgap ref., power down dec., charge pump ref., voltage regulator	off	on	on
Prescaler	off	on	on
VCO1 (Rx)	off	on	off
VCO2 (Tx)	off	off	on
Delay, doubler	off	on	on

Prescaler Divider Ratio

The table shows the relation between the logic level of the input MOD and the prescaler divider ratio.

Logic Level of MOD	Prescaler Divide Ratio
HIGH	1:64
LOW	1:65

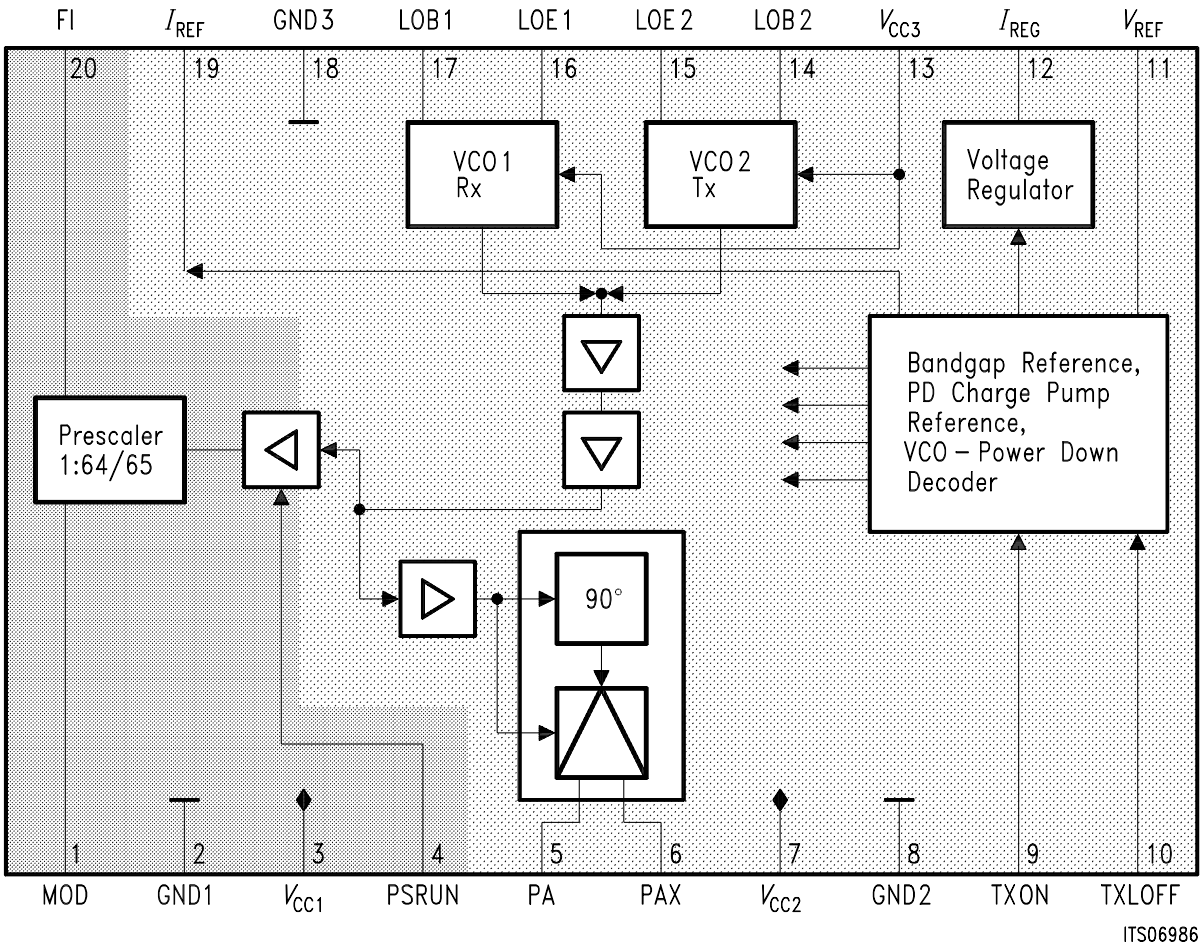


Figure 2
Supply Voltage Partitioning

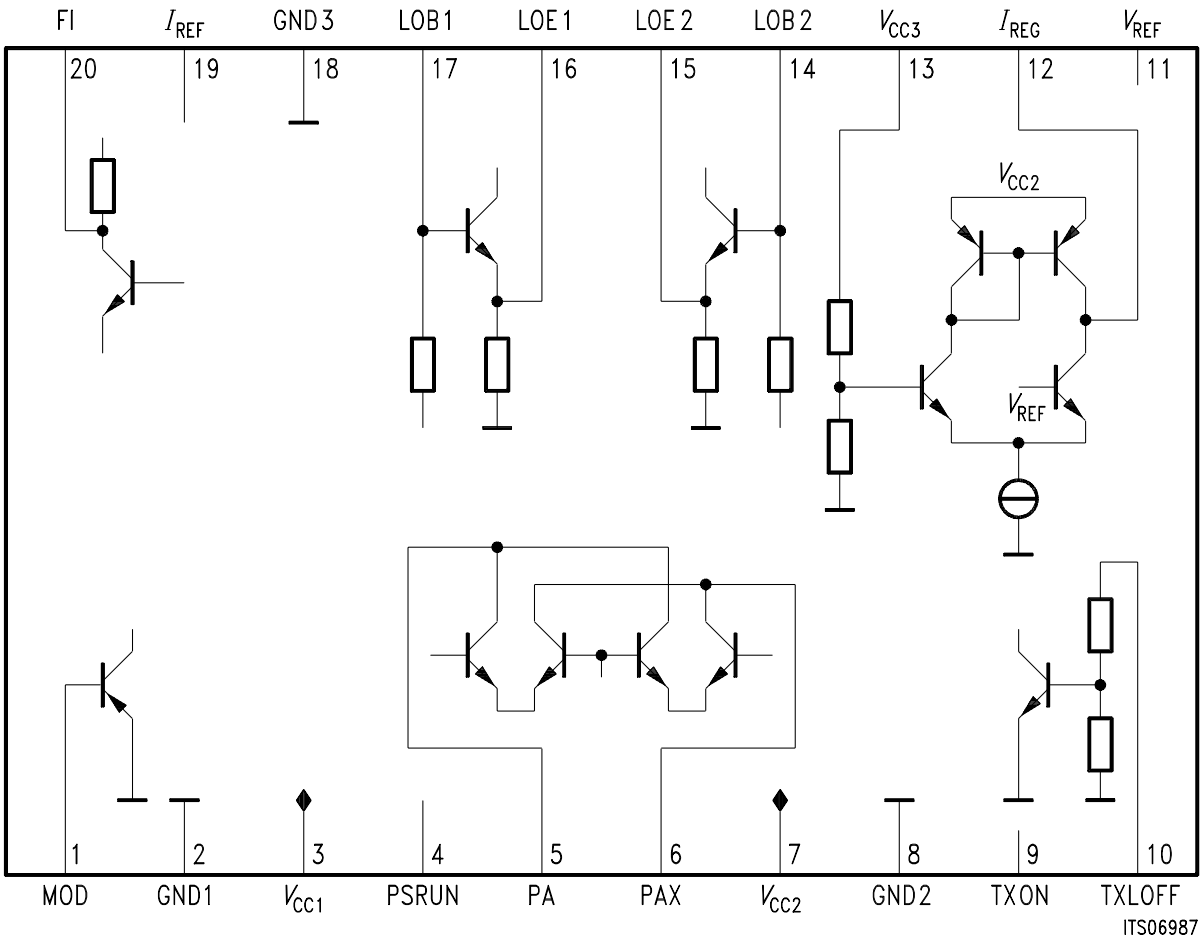


Figure 3
Input/Output Circuits Part 1

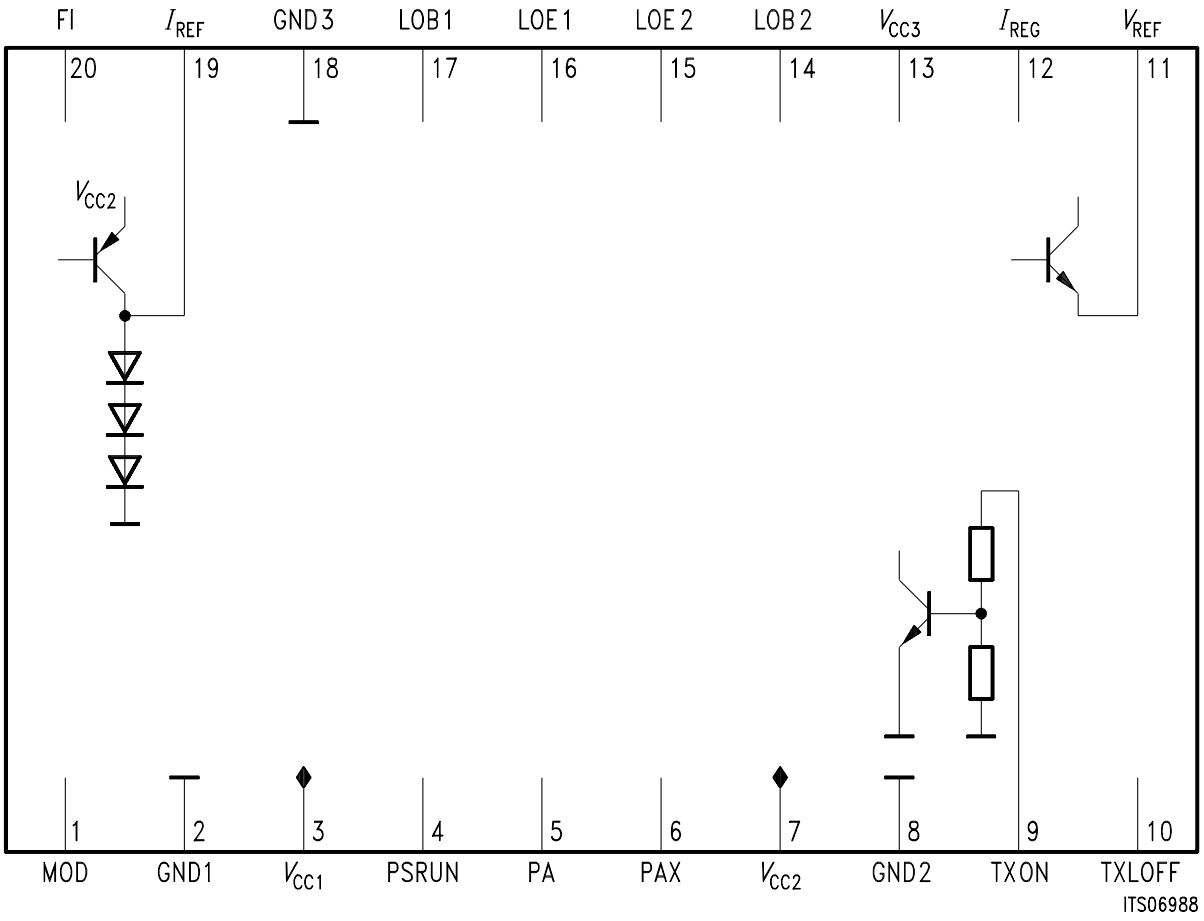


Figure 4
Input/Output Circuits Part 2

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

T_A = – 10 °C to + 55 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_{CC1,2,(3)}$	– 0.5	+ 7	V	
Differential input voltage (pins LOB1 to LOE1 and LOB2 to LOE2)	V_{diff}	– 1	+ 1	V	
Resistance between pin V_{REF} and GND	R_{VREF}	1.3		kΩ	note [1]
Junction temperature	T_j		+ 125	°C	note [2]
Storage temperature	T_S	– 65	+ 150	°C	

[1] Corresponds to a current I_{REF} of about 700 µA.

[2] The thermal resistance R_{th} (junction to ambient) of the P-SSOP-20 package is about xxxx K/W.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Operational Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	3.0	5.5	V	V_{CC} = V_{CC1} = V_{CC2}
Resistance between pin V_{REF} and GND	R_{VREF}	2.6		kΩ	note [1]
Voltage at pin I_{REF}	V_{IREF}	GND	V_{CC} – 1.5	V	V_{CC} = V_{CC1} = V_{CC2}
Input-/Oscillation frequency	f_{VCO}	800	1000	MHz	

[1] Corresponds to a current I_{REF} of about 360 µA.

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 AC / DC Characteristics

Supply voltage V_{CC} = 3.0 … 5.5 V
Ambient temperature T_A = – 10 … + 55 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit	Test Conditions
		min.	typ.	max.			
Supply Currents							
Supply current during standby (TXLOFF = LOW)	I_{VCC1}			50	µA	1	T_A = 25 °C; V_{CC1} = 3.0 V
	I_{VCC2}			50	µA	1	V_{CC2} = 3.0 V
	I_{VCC3}			70	µA	1	
	$I_{PA/PAX}$			50	µA	1	
Supply current (TXLOFF = HIGH)	I_{VCC1}		2.7	3.6	mA	1	T_A = 25 °C; V_{CC1} = 3.0 V
	I_{VCC2}		13.8	17	mA	1	V_{CC2} = 3.0 V
	I_{VCC3}		7.7	10	mA	1	V_{CC3} = 3.0 V
	$I_{PA/PAX}$	3.5	4.5	5.5	mA	1	
Supply current (TXLOFF = HIGH)	I_{VCC1}		3.0	4	mA	1	T_A = 25 °C; V_{CC1} = 5.5 V
	I_{VCC2}		14.9	18	mA	1	V_{CC2} = 5.5 V
	I_{VCC3}		8.4	11	mA	1	V_{CC3} = 5.5 V
	$I_{PA/PAX}$	3.5	4.9	6	mA		
Control Inputs TXLOFF, MD, TXON							
TXLOFF voltage HIGH	$V_{TXLOFFH}$	2.0		5.5	V	1	
TXLOFF voltage LOW	$V_{TXLOFFL}$	GND		0.4	V	1	
TXLOFF input current HIGH	$I_{TXLOFFH}$			200	µA	1	
TXLOFF input current LOW	$I_{TXLOFFL}$			20	µA	1	
TXON voltage HIGH	V_{TXONH}	2.0		5.5	V	1	
TXON voltage LOW	V_{TXONL}	GND		0.8	V	1	
TXON input current HIGH	I_{TXONH}	– 20			µA	1	
TXON input current LOW	I_{TXONL}	– 100			µA	1	

3.3 AC / DC Characteristics (cont'd)

Supply voltage V_{CC} = 3.0 … 5.5 V
Ambient temperature T_A = – 10 … + 55 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit	Test Conditions
		min.	typ.	max.			
Current Source V_{REF}, I_{REF}							
Current I_{REF}	I_{IREF0}		100		µA	1	R_{VREF} = 8.7 kΩ, pin I_{REF} and GND
Tolerance due to Production		– 10		+ 10	%	1	
Tolerance due to Temperature		– 5		– 5	%	1	
Sensitivity of I_{REF} with respect to supply	m		2.5	4	µA/V	1	
VCO (with Fixed Resonator and External Circuitry see Test Circuit 2)							
Oscillator frequency tuning range	f_{VCO}					2	V_T = 0.5 … 2.5 V with fixed resonator
Rx-lower limit	$f_{VCO-Rxmin}$			879	MHz	2	
Rx-upper limit	$f_{VCO-Rxmax}$	901			MHz	2	
Tx-lower limit	$f_{VCO-Txmin}$			934	MHz	2	
Tx-upper limit	$f_{VCO-Txmax}$	956			MHz	2	
Power supply ripple rejection	A_r		– 45	– 35	dB	2	note [1]
Supply voltage dependence of oscillator frequency note [2]	$\Delta f_{VCO}/\Delta V_{CC3}$			300	kHz/V	2	1
Supply voltage dependence of oscillator frequency note [2]	$\Delta f_{VCO}/\Delta V_{CC2}$			20	kHz/V	2	1

Note: $V_{CC} = V_{CC1}$ or V_{CC2}

[1] Trapezoidal ripple with 200 mV amplitude, 10 µs rise/fall time, 900 µs cycle time, 50 % duty cycle.

[2] Assuming 200 mV ripple on V_{CC2} the overall frequency deviation should be less than 10 kHz.
$\Delta f_{VCO} \leq$ 10 kHz (typ)

3.3 AC / DC Characteristics (cont'd)

Supply voltage V_{CC} = 3.0 … 5.5 V
Ambient temperature T_A = – 10 … + 55 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit	Test Conditions
		min.	typ.	max.			
Sideband noise after frequency doubling measured at PA/PAX			– 80 – 110 – 125 – 135	– 75 – 105 – 115 – 131	dBc/Hz dBc/Hz dBc/Hz dBc/Hz	2 2 2 2	at 50 kHz offset at 1.2 MHz offset at 3.0 MHz offset at 4.7 MHz offset
Signal Output PA / PAX							
Output resistance	$R_{PA/X}$		150		Ω		differential output ($f_{PA/X}$ = 1900 MHz)
Output capacitance	$C_{PA/X}$		640		f_F		in parallel to $R_{PA/X}$ ($f_{PA/X}$ = 1900 MHz)
Output level	$P_{PA/X}$	– 7	– 5	– 3	dBm	1	R_Q = 200 Ω T_A = 25 °C; V_{CC2} = 3.0 V
Supply voltage dependence of output level	$\Delta P_{PA/X}/\Delta V_{CC2}$		+ 0.2		dBm/V	1	R_Q = 200 Ω
Temperature dependence of output level	$\Delta P_{PA/X}/\Delta T_A$		– 0.02		dBm/K	1	R_Q = 200 Ω
Suppression of fundamental	A_f		– 25	– 15	dB	1	

3.3 AC / DC Characteristics (cont'd)

Supply voltage V_{CC} = 3.0 … 5.5 V
Ambient temperature T_A = – 10 … + 55 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit	Test Conditions
		min.	typ.	max.			
Output FI and Input MOD							
Output logic swing	V_{FI}	0.5			Vpp	1	$C_L \leq 8$ pF
MOD voltage High	V_{MODH}	2.0		5.5	V	1	
MOD voltage Low	V_{MODL}	GND		0.8	V	1	
MOD input current High	I_{MODH}			50	µA	1	
MOD input current Low	I_{MODL}	– 100			µA	1	
MOD setup time (diagram 1)	t_{set}			29	ns	1	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

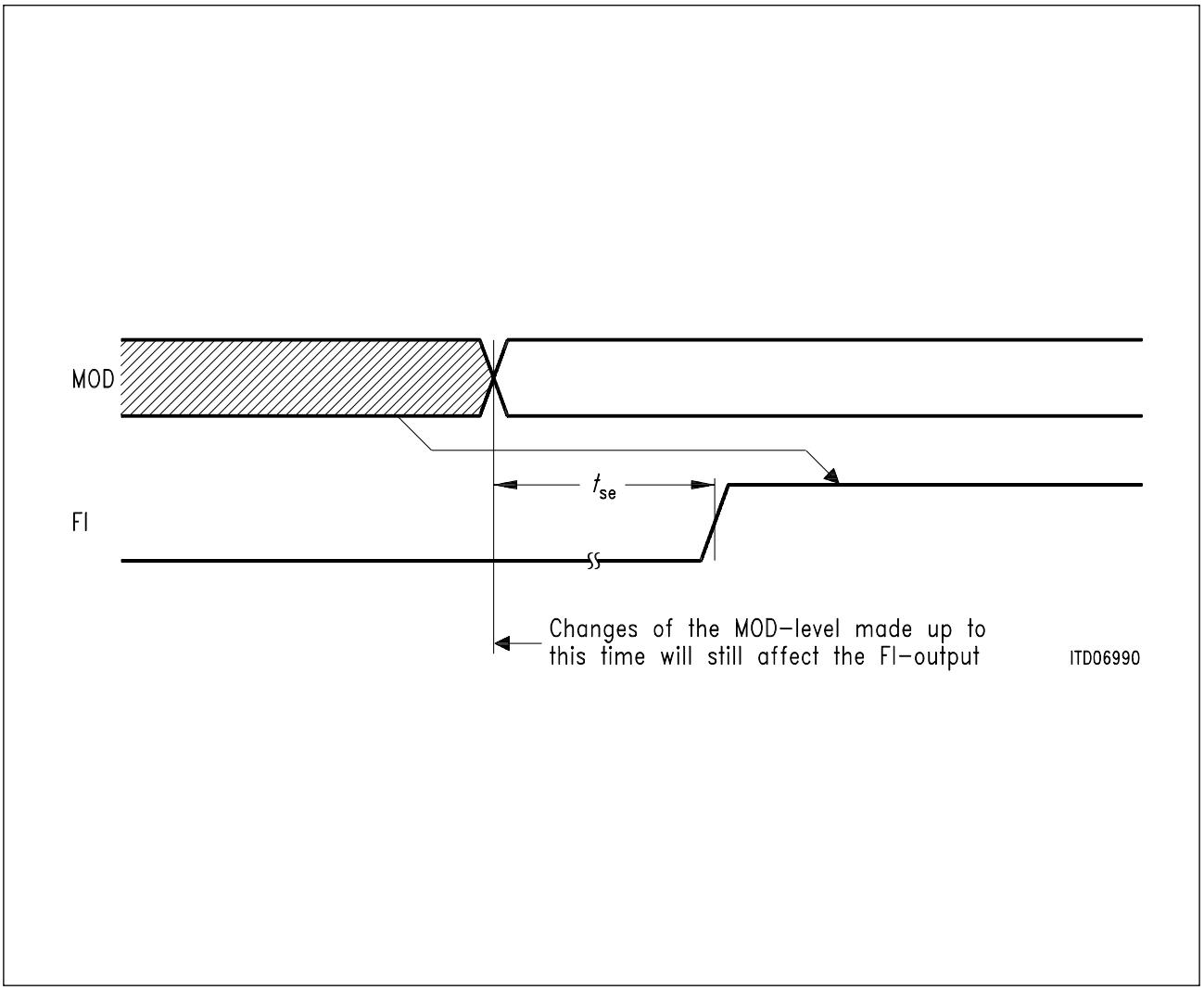
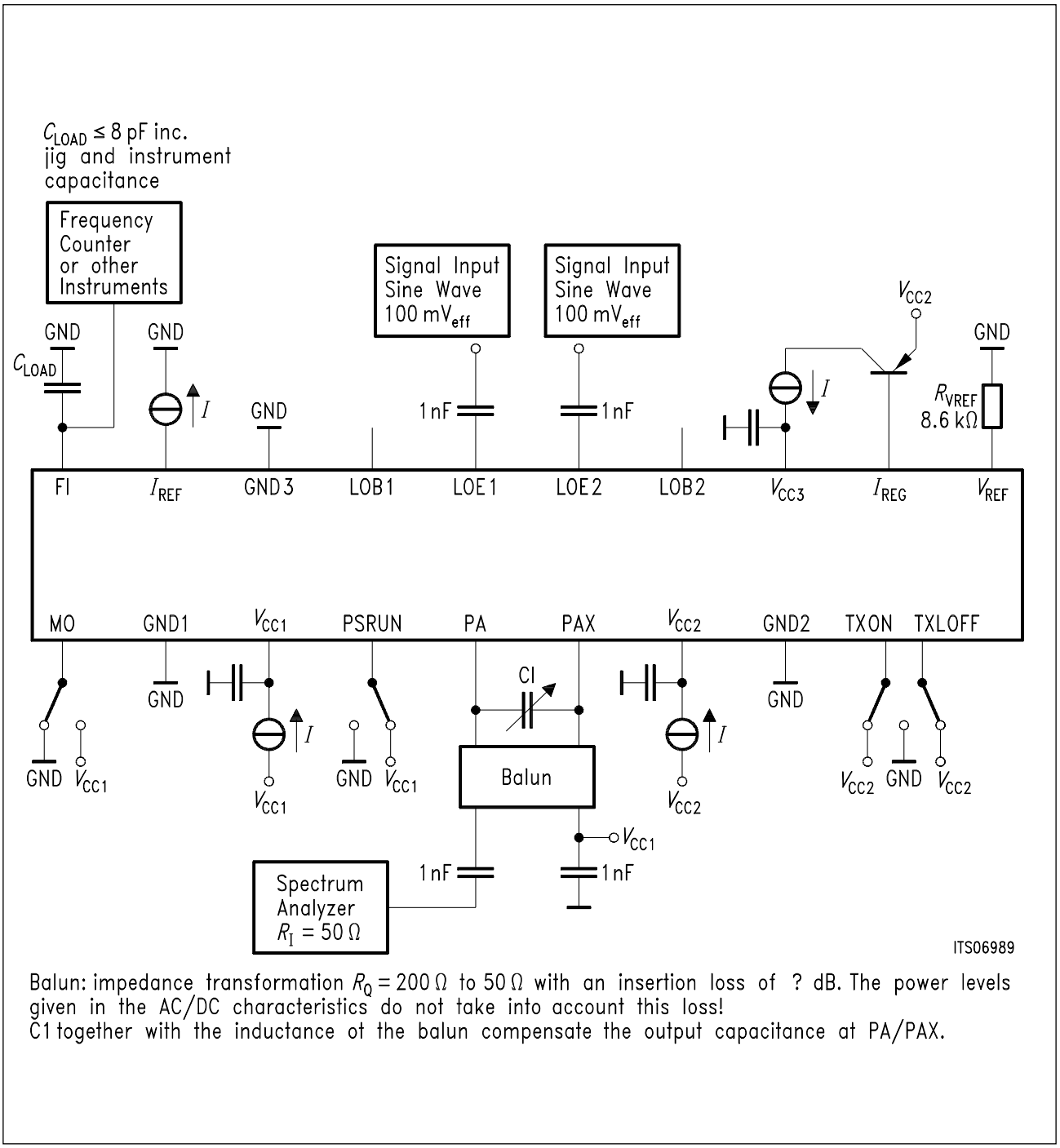


Figure 5
Diagram 1



Balun: impedance transformation R_Q = 200 Ω to 50 Ω with an insertion loss of ? dB. The power levels given in the AC/DC characteristics do not take into account this loss!
C1 together with the inductance ot the balun compensate the output capacitance at PA/PAX.

Figure 6
Test Circuit 1

Test Circuit 2

The test circuit 2 given in this section is used to verify the system performance of the synthesizer consisting of the PMB 2220 and the PMB 2306 or PMB 2307. The aim is to give a common test circuit as well as its layout as a reference for the DECT related system performance measurements.

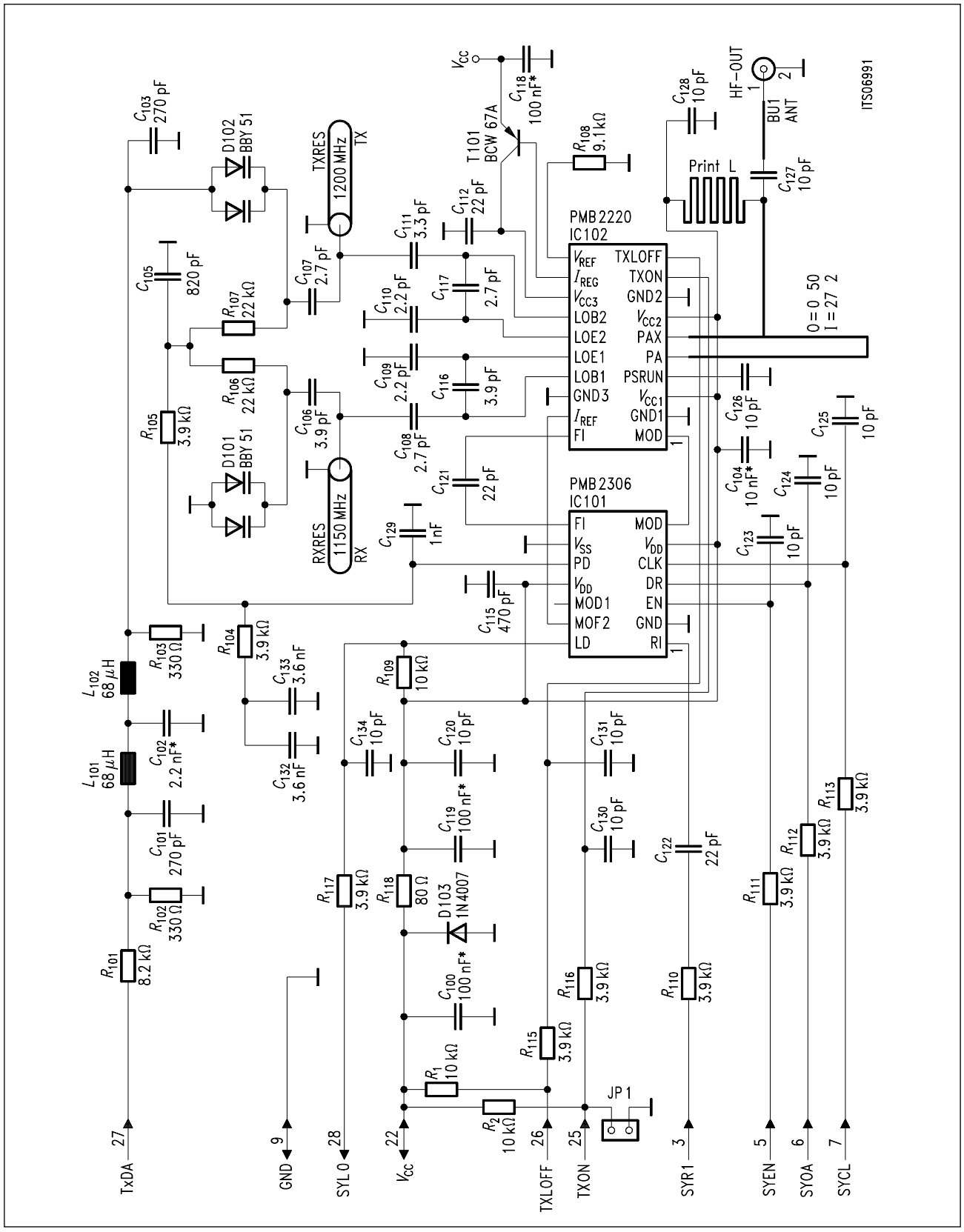


Figure 7
Test Circuit 2: Circuit Diagram

Bill of Materials

Project Name: SCH\PMB_2220 Time & date: 16:49 Sep. 27, 1994

#	Device	Value	Package Type	Refdes
1	C	2.2 nF*	0603RC	C102
2	C	2.2 pF	0603RC	C109, C110
3	C	2.7 pF	0603RC	C107, C108, C117
1	C	3.3 pF	0603RC	C111
2	C	3.9 pF	0603RC	C106, C116
1	C	10 nF*	0603RC	C104
10	C	10 pF	0603RC	C120, C123, C124, C125, C126, C127 C128, C130, C131, C134
3	C	22 pF	0603RC	C112, C121, C122
2	C	270 pF	0603RC	C101, C103
1	C	470 pF	0603RC	C115
1	C	1 nF	0805RC	C129
2	C	100 nF*	0805RC	C118, C119
1	C	820 pF	0805RC	C105
1	C	100 nF*	1206RC	C100
2	C	5.6 nF	1210RC	C132, C133
1	RES	1150 MHz	CER-RES	RXRES
1	RES	1200 MHz	CER-RES	TXRES
2	COIL	68 µH	1210RC	L101, L102
1	DIODE	1N4007	MELF	D103
2	DIODE	BBY 51	SOT-23	D101, D102
1	CON	ANT SMA-WBU		BU1
1	IC	PMB 2306	SO-14	IC101
1	IC	PMB 2220	SSOP-20	IC102
1	JUMPER HEADER 2			JP1
2	R	22 k	0603RC	R106, R107
2	R	330	0603RC	R102, R103
9	R	3.9 k	0603RC	R104, R105, R110, R111, R112, R113, R115, R116, R117
1	R	8.2 k	0603RC	R101
1	R	9.1 K	0603RC	R108
2	R	10 k	0805RC	R1, R2
1	R	0 Ω	1206RC	R118
1	R	10 k	1206RC	R109
1	BJT	BCW 67A	SOT-23	T101

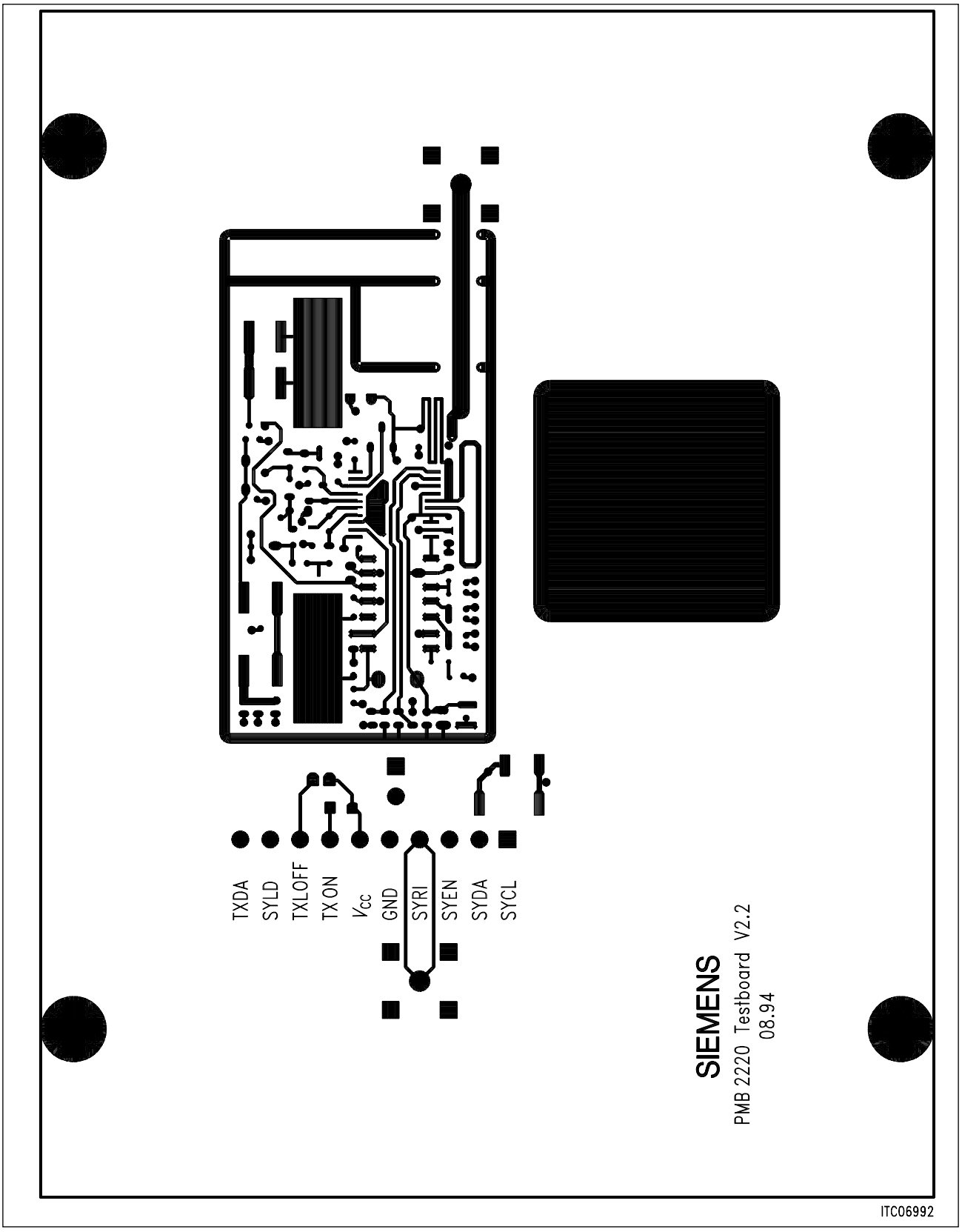


Figure 8
Test Circuit 2: Top Layer

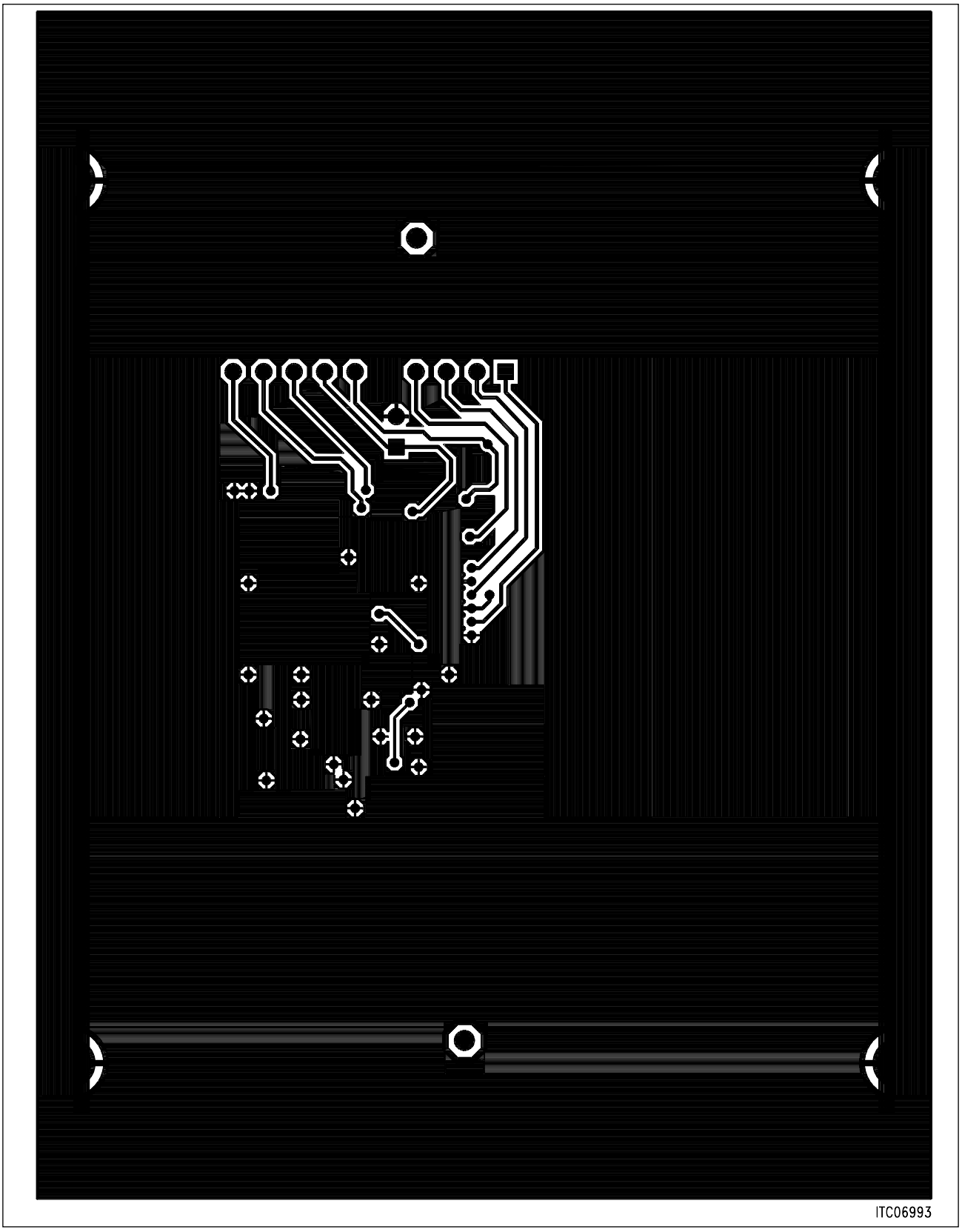


Figure 9
Test Circuit 2: Bottom Layer

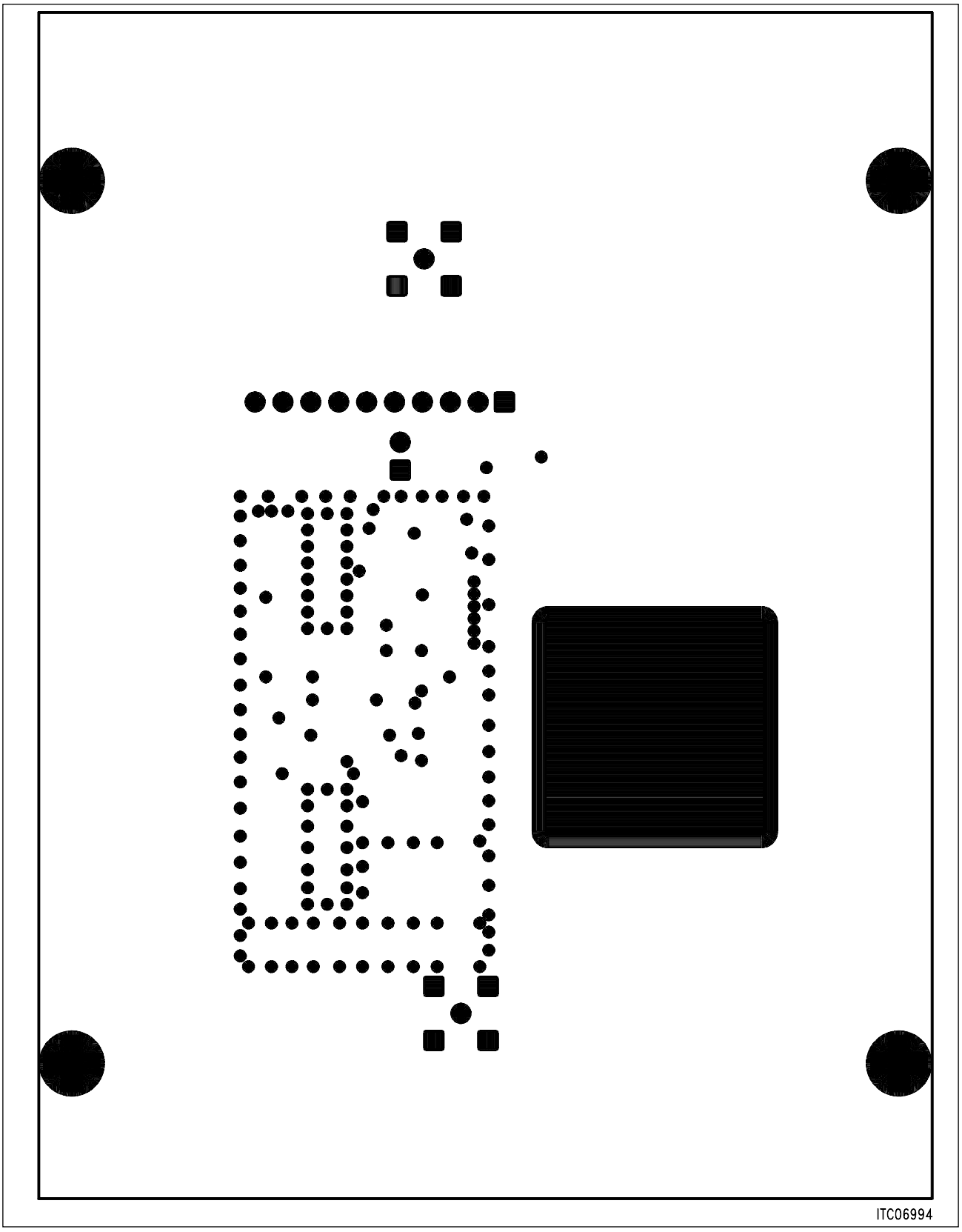


Figure 10
Test Circuit 2: Drill Layer

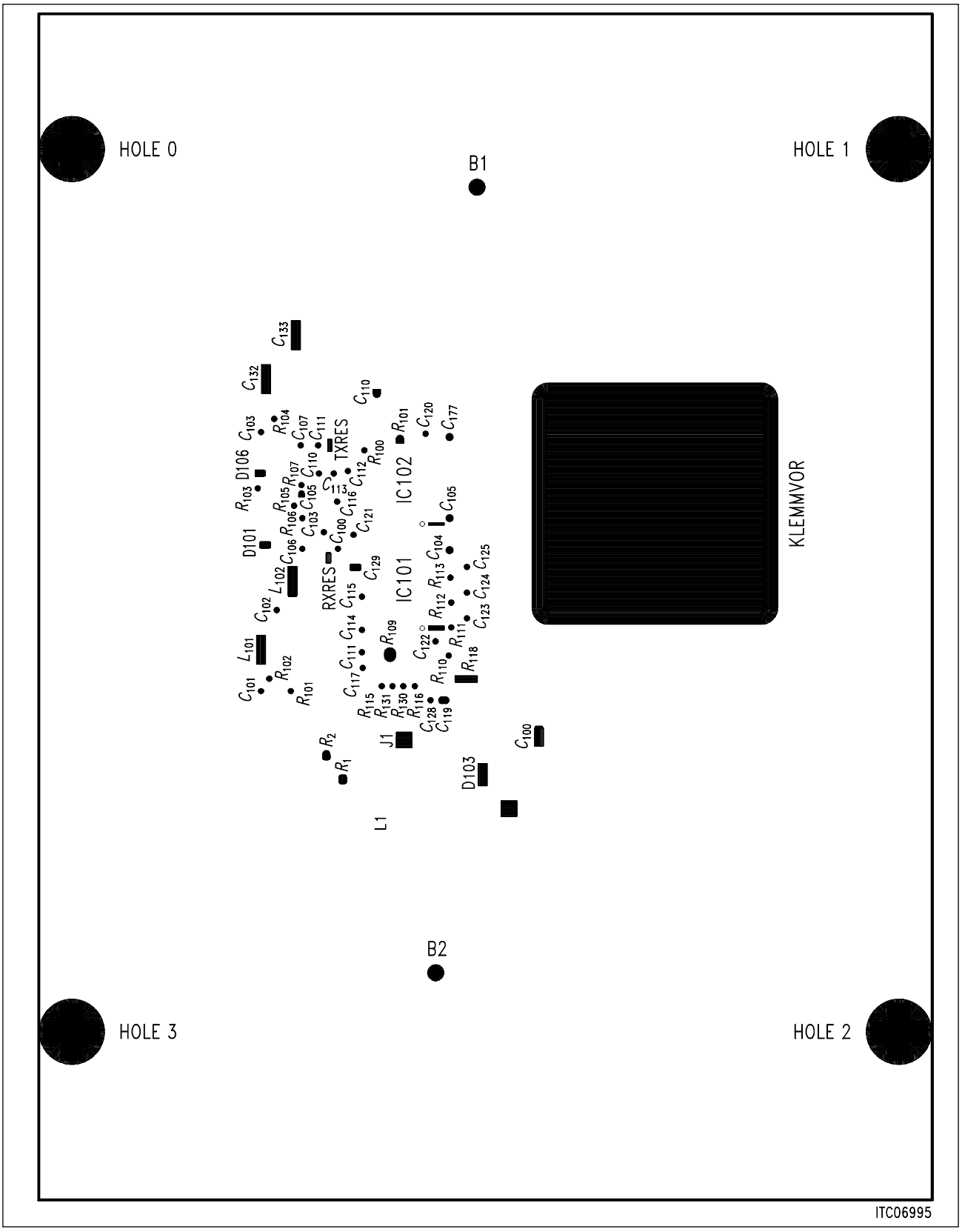
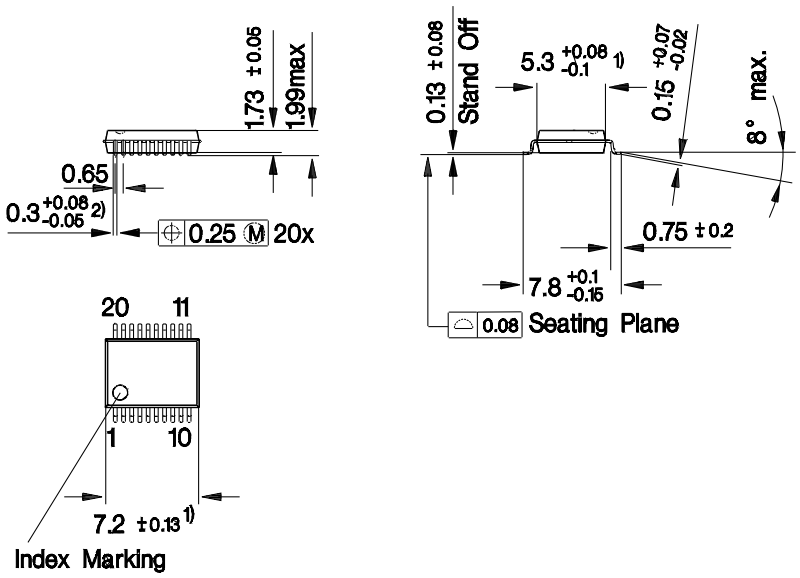


Figure 11
Test Circuit 2: Assembly Diagram

4 Package Outlines

P-SSOP-20-1
(Plastic Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPS05387

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm