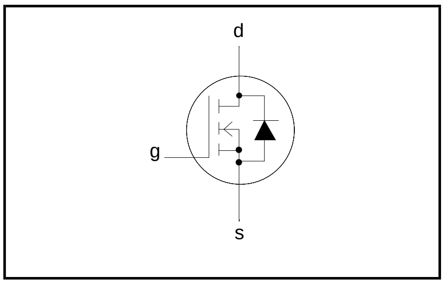
PowerMOS transistors FREDFET, Avalanche energy rated

PHX6ND50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Isolated package
- Fast reverse recovery diode

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 3.1 A

$R_{DS(ON)} \leq 1.5\ \Omega$

t_{rr} = 180 ns

GENERAL DESCRIPTION

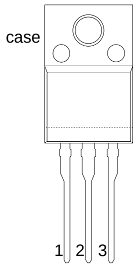
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHX6ND50E is supplied in the SOT186A full pack, isolated package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{hs} = 25 ˚C; V_{GS} = 10 V	-	3.1	A
		T_{hs} = 100 ˚C; V_{GS} = 10 V	-	2	A
I_{DM}	Pulsed drain current[1]	T_{hs} = 25 ˚C	-	24	A
P_D	Total dissipation	T_{hs} = 25 ˚C	-	35	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	˚C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 4 A; t_p = 0.17 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq 50$ V; $R_{GS} = 50\ \Omega$; V_{GS} = 10 V; refer to fig:17	-	280	mJ
E_{AR}	Repetitive avalanche energy[1]	I_{AR} = 5.9 A; t_p = 1 µs; T_j prior to avalanche = 25˚C; $R_{GS} = 50\ \Omega$; V_{GS} = 10 V; refer to fig:18	-	10	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	5.9	A

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	3.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

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[1] pulse width and repetition rate limited by T_j max.

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 6 A; V_{DD} = 400 V; V_{GS} = 10 V	-	53	64	nC
Q_{gs}	Gate-source charge		-	4	6	nC
Q_{gd}	Gate-drain (Miller) charge		-	28	34	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 39 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 12 Ω	-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{hs} = 25˚C	-	-	5.9	A
I_{SM}	Pulsed source current (body diode)	T_{hs} = 25˚C	-	-	24	A
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	180	-	ns
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125˚C	-	220	-	ns
Q_{rr}	Reverse recovery charge	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	0.65	-	µC
		I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125˚C	-	2.6	-	µC
I_{rrm}	Peak reverse recovery current	I_S = 6 A; V_{GS} = 0 V; dI/dt = 100 A/µs; 125˚C	-	15	-	A

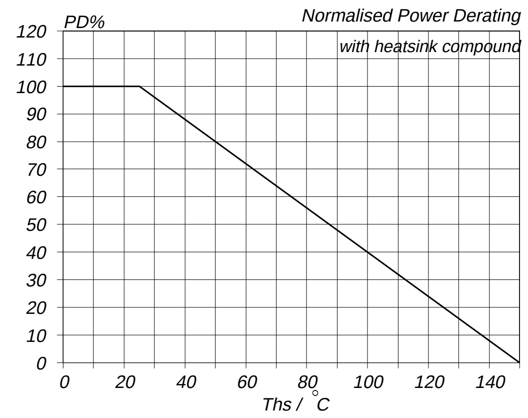

Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25\,^\circ C} = f(T_{hs})$

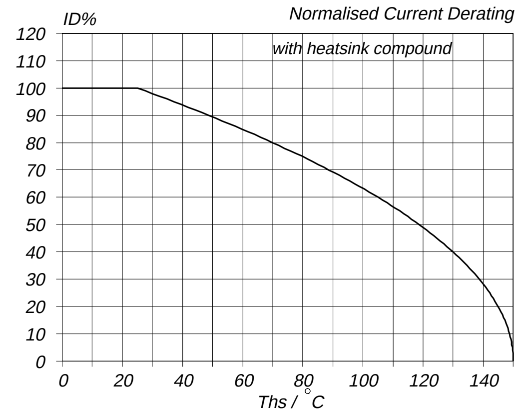

Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\,25\,^\circ C} = f(T_{hs})$; conditions: $V_{GS} \geq 10$ V

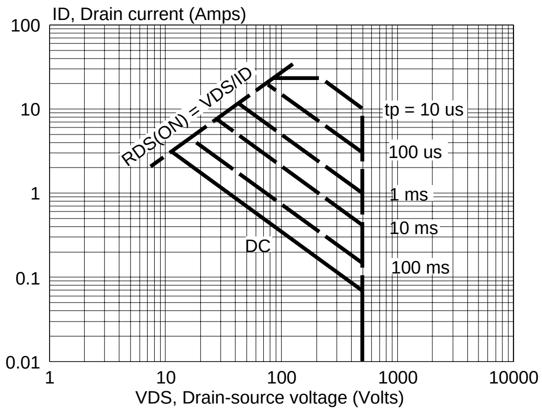

Fig.3. Safe operating area. $T_{hs} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

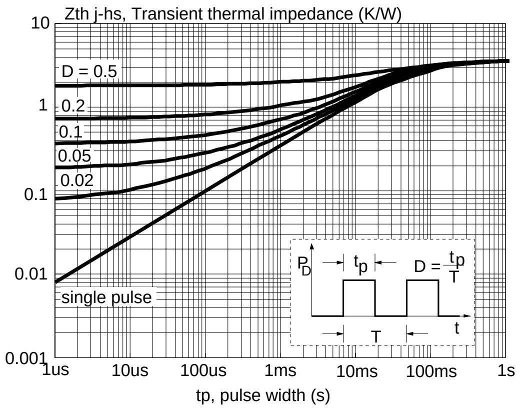

Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}hs} = f(t)$; parameter $D = t_p/T$

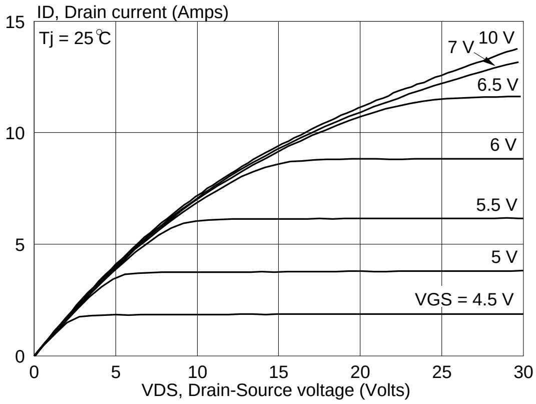

Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

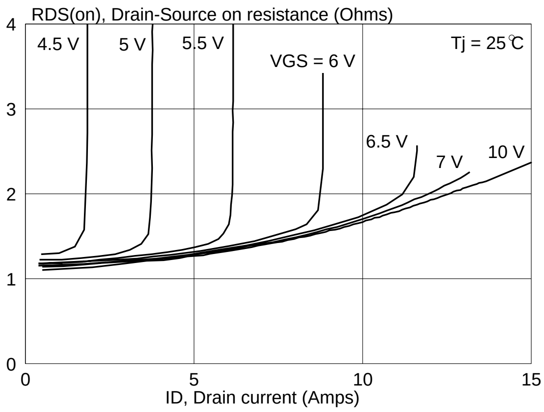

Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

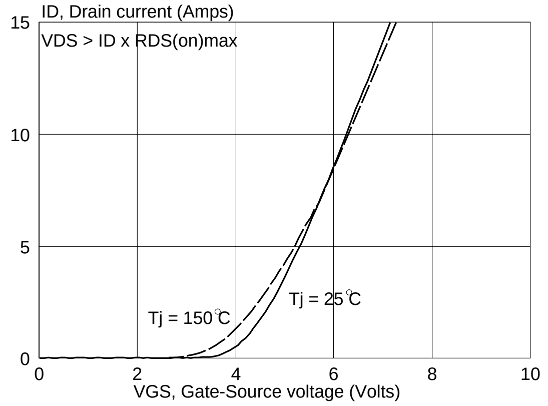

Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

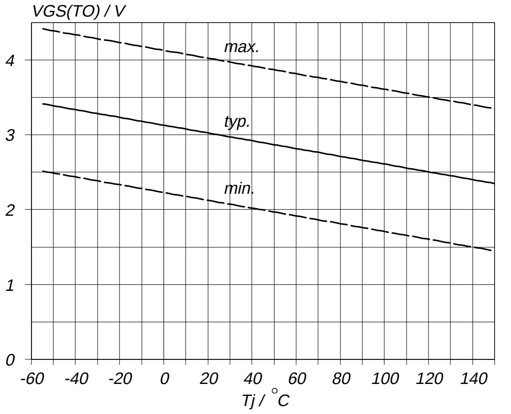

Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

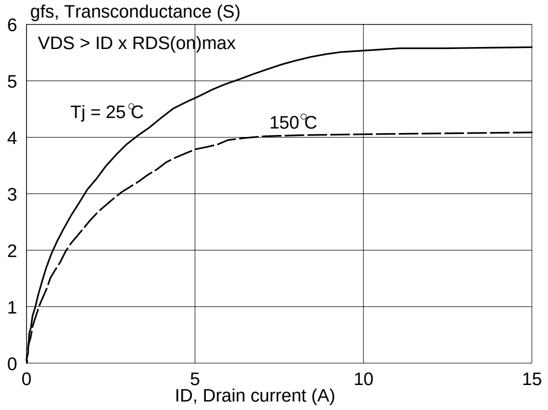

Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

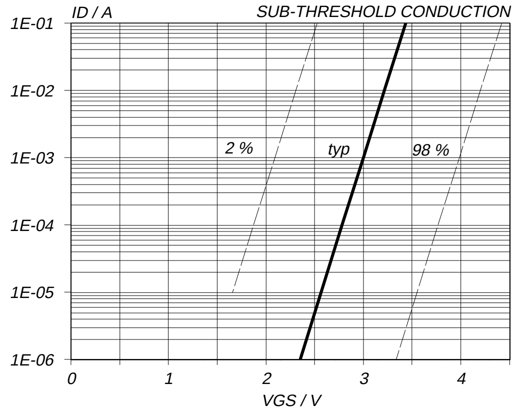

Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

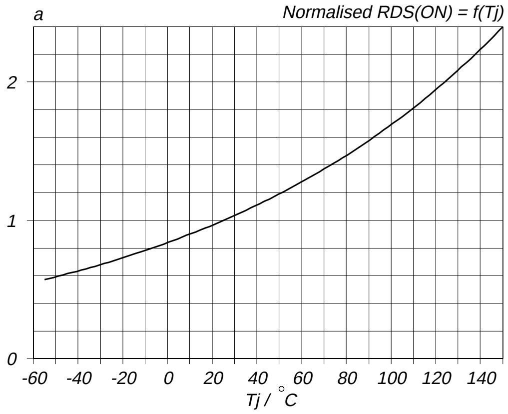

Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$; $I_D = 3$ A; $V_{GS} = 10$ V

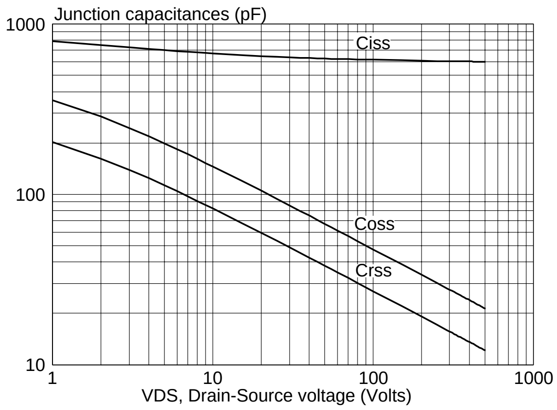

Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

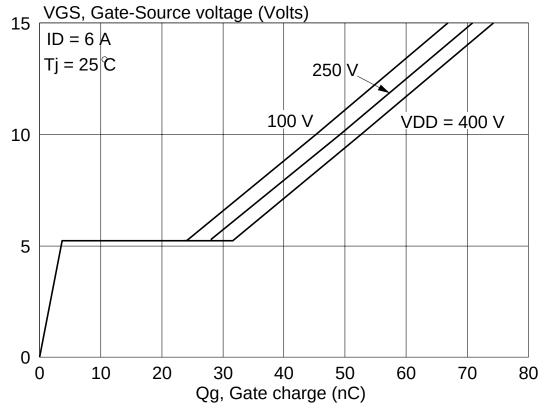

Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; *parameter* V_{DS}

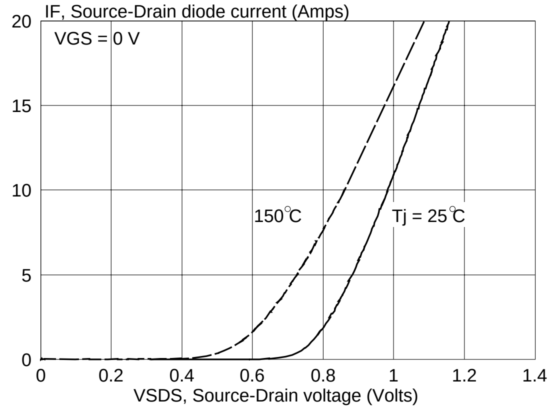

Fig.16. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; *parameter* T_j

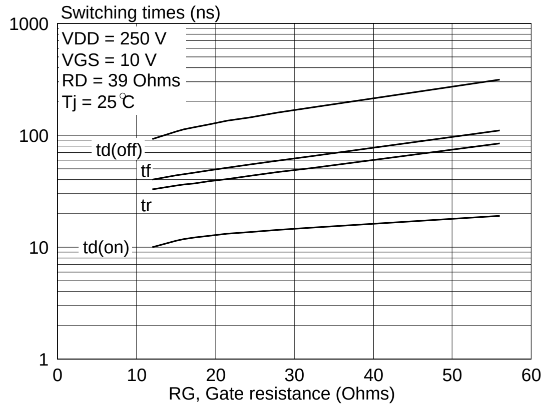

Fig.14. Typical switching times; $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

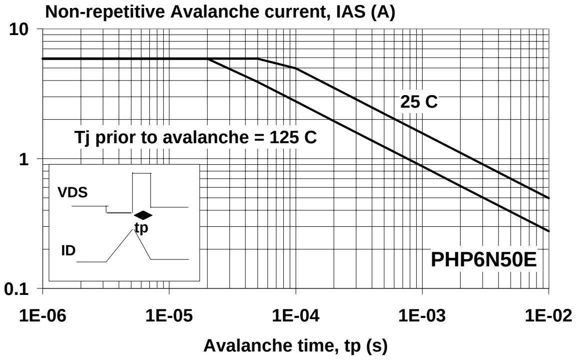

Fig.17. Maximum permissible non-repetitive avalanche current (I_{AS}) *versus avalanche time* (t_p); *unclamped inductive load*

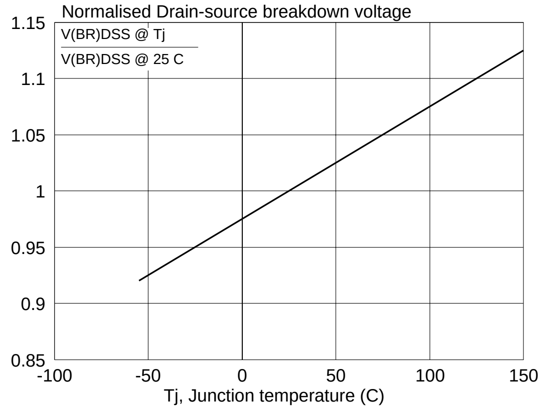

Fig.15. Normalised drain-source breakdown voltage; $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

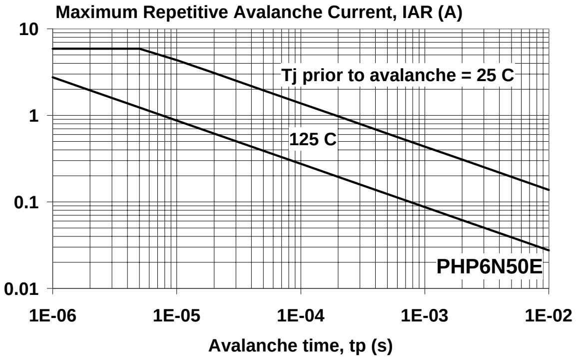

Fig.18. Maximum permissible repetitive avalanche current (I_{AR}) *versus avalanche time* (t_p)

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

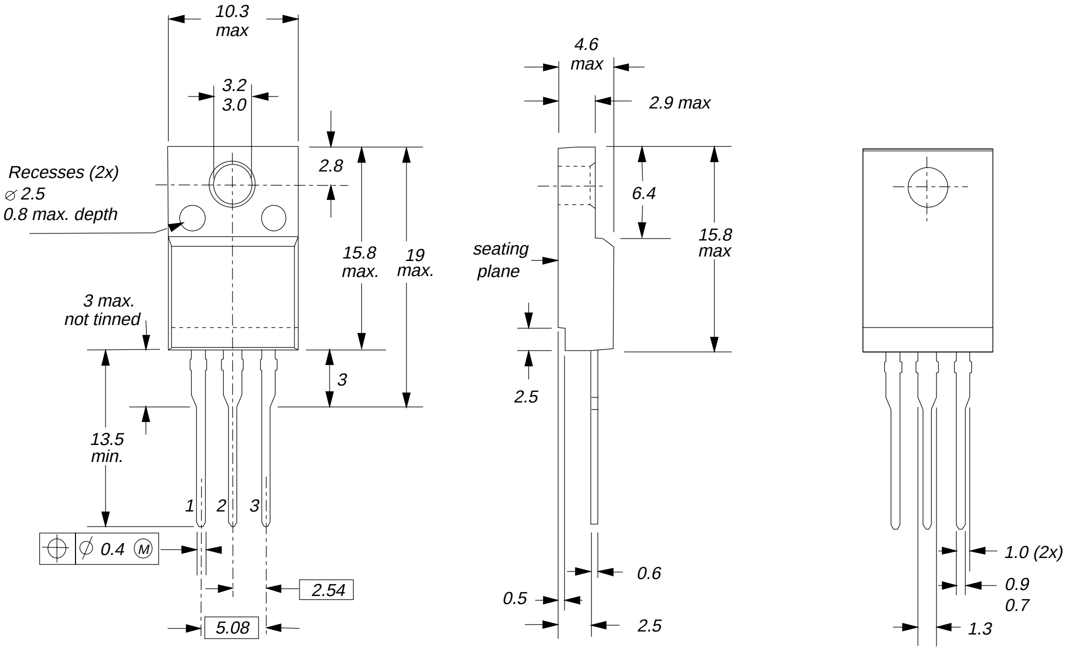

Fig.19. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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