PowerMOS transistors Avalanche energy rated

PHU2N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Extremely high dV/dt capability

QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 2 A

$R_{DS(ON)} \leq 5\ \Omega$

GENERAL DESCRIPTION

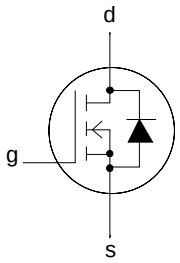
N-channel, enhancement mode field-effect power transistor, intended for use in **C**ompact **F**luorescent **L**amps (CFL) and low power ballasts. The PHU2N50E is compatible with self oscillating and IC driven circuits, including the UBA2021 ballast controller IC. Other applications include off line switched mode power supplies and D.C. to D.C. converters.

The PHU2N50E is supplied in the SOT533 (I-PAK) leaded package.

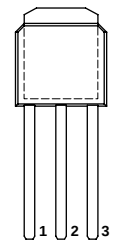
PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SYMBOL



SOT533



Top view MBK915

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 10 V	-	2	A
		T_{mb} = 100 ˚C; V_{GS} = 10 V	-	1.3	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	8	A
P_D	Total dissipation	T_{mb} = 25 ˚C	-	50	W
dV/dt	Peak Diode Recovery voltage slope. (See fig. 19)	I_{ds} 2.0 A; dI/dt = 100 A/µs; V_s = 8V; $T_j < T_{jmax}$	-	5.2	V/ns
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	˚C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 1.26 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq$ 50 V; R_{GS} = 50 Ω; V_{GS} = 10 V; refer to fig:17	-	82	mJ
E_{AR}	Repetitive avalanche energy[1]	I_{AR} = 2 A; t_p = 2.5 µs; T_j prior to avalanche = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V; refer to fig:18	-	3.3	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	In free air	-	70	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1 A	-	3.1	5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1 A	0.5	1.3	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 ˚C	-	77	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2 A; V_{DD} = 400 V; V_{GS} = 10 V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 120 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 24 Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	236	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Feedback capacitance		-	22	-	pF

1 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25˚C	-	-	2	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25˚C	-	-	8	A
V_{SD}	Diode forward voltage	I_S = 2 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 2 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	µC

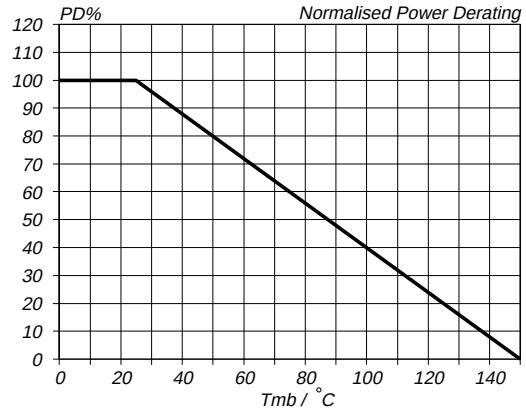


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

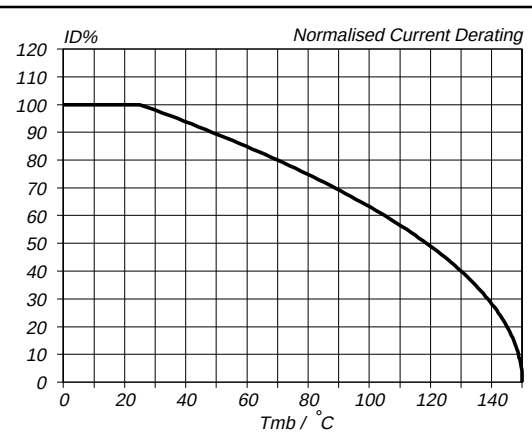


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

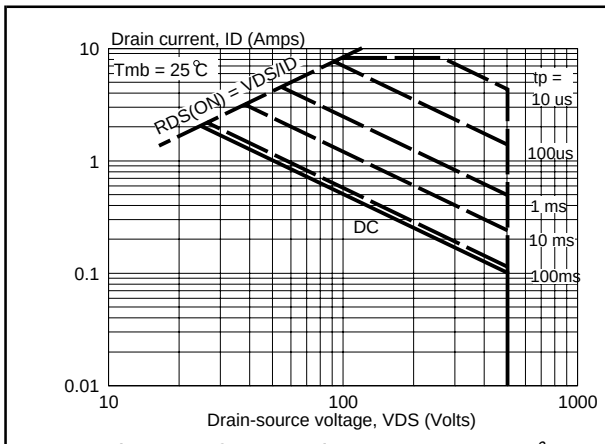


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

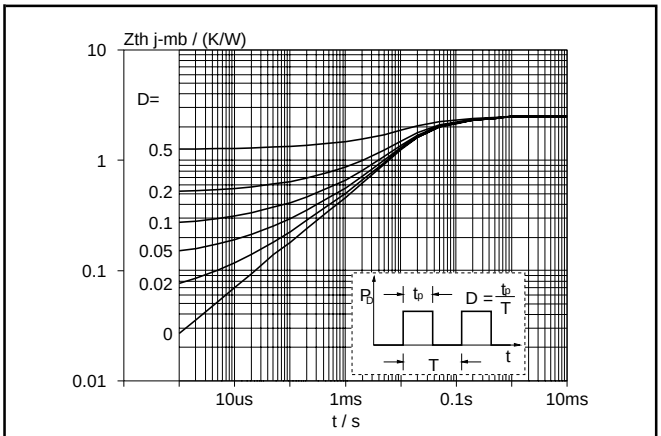


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

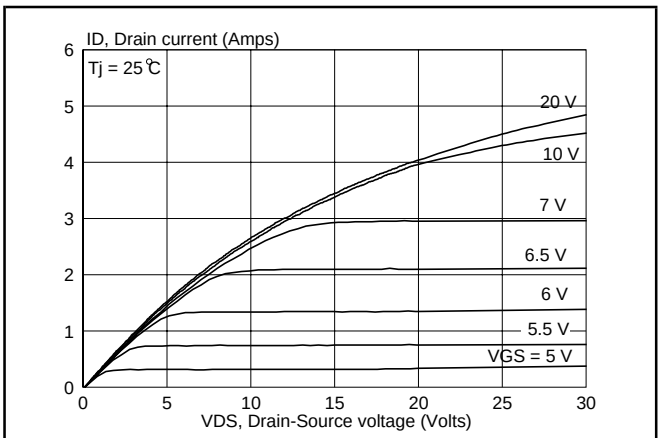


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

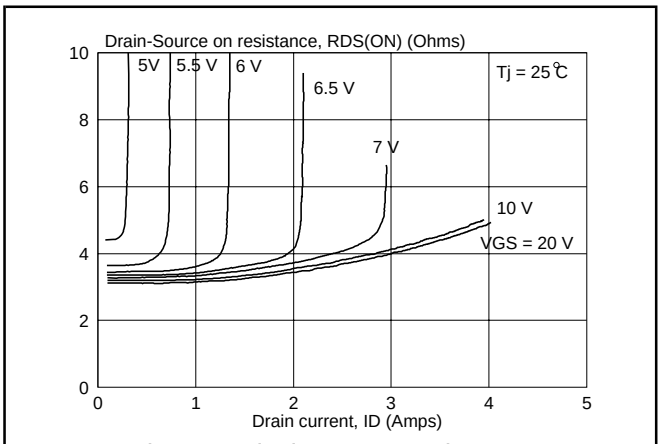


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

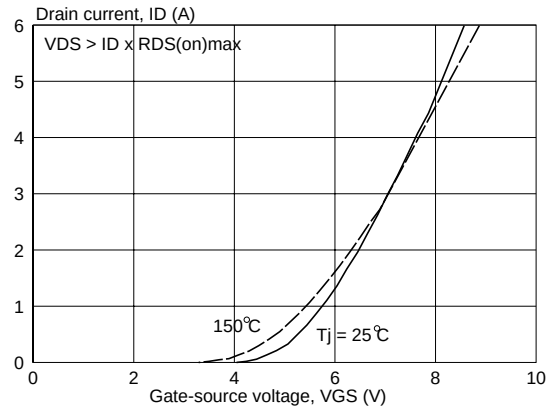


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

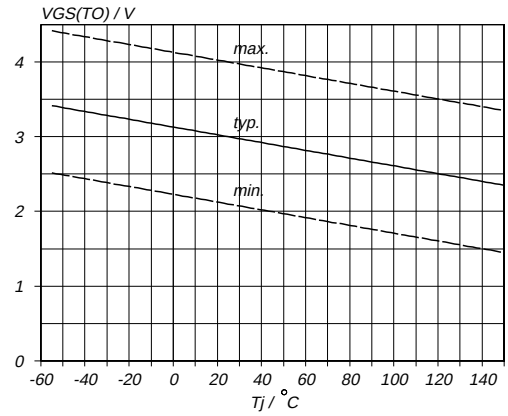


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

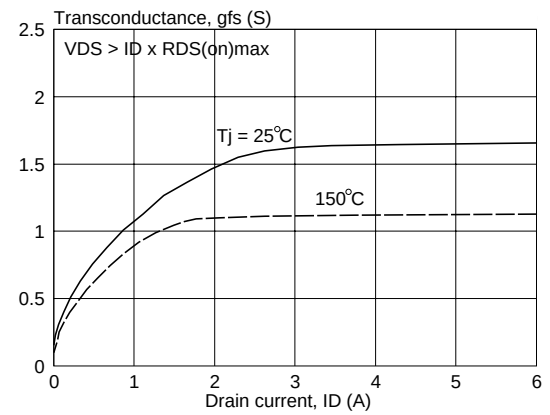


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

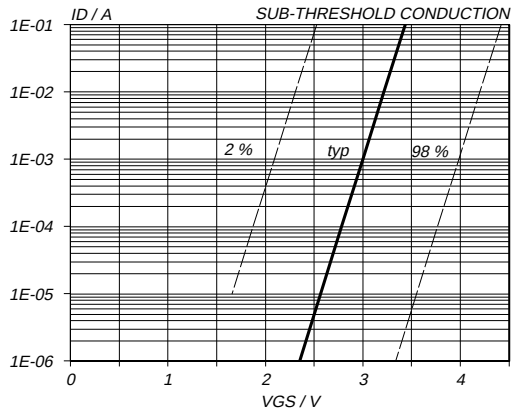


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

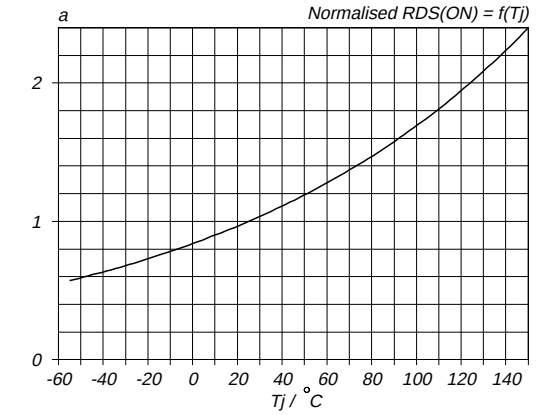


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$; I_D = 1 A; V_{GS} = 10 V

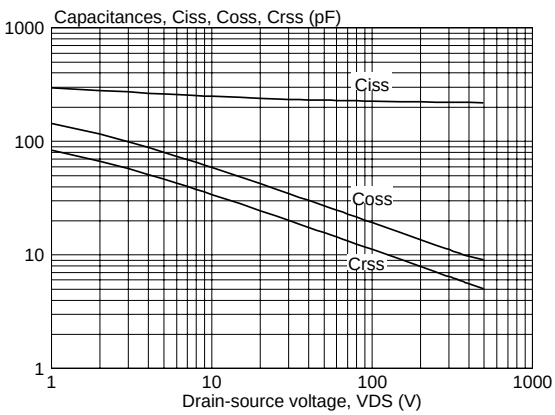


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

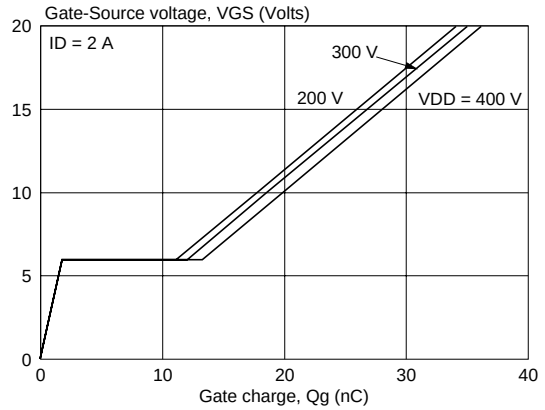


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

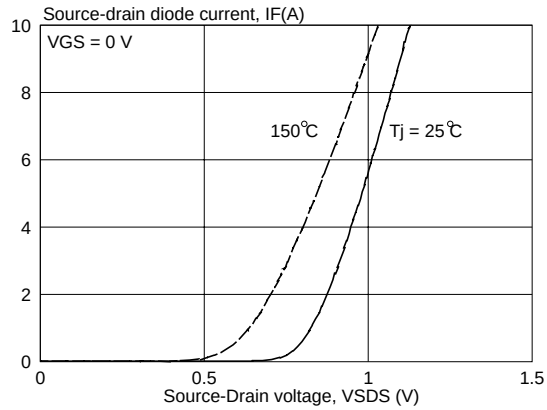


Fig.16. Source-Drain diode characteristic. $I_F = f(V_{SDS})$; parameter T_j

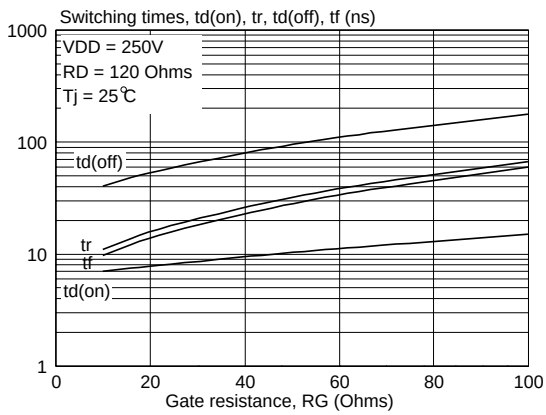


Fig.14. Typical switching times; $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

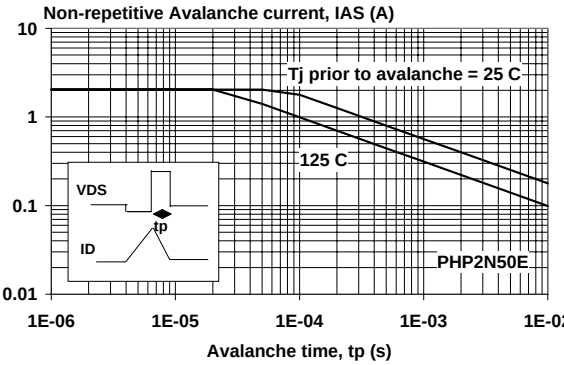


Fig.17. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

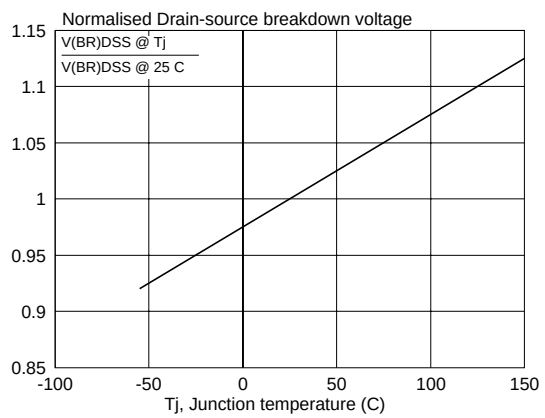


Fig.15. Normalised drain-source breakdown voltage; $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

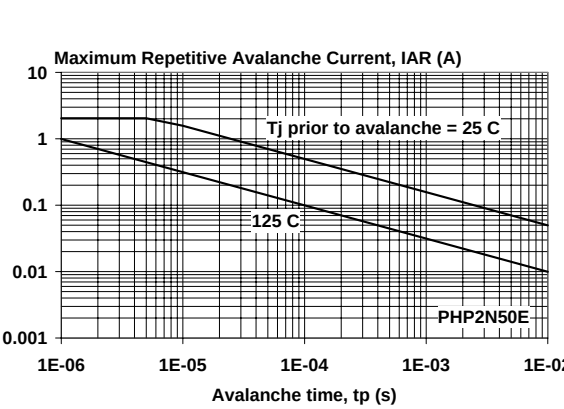
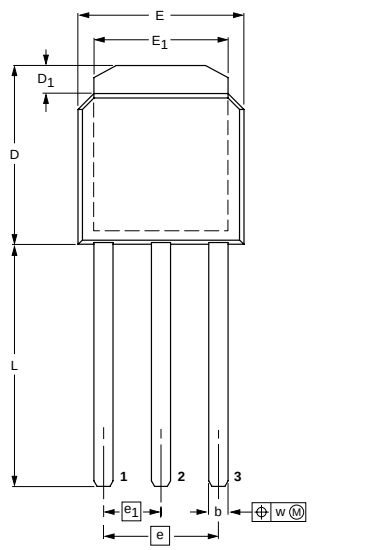


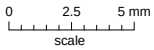
Fig.18. Maximum permissible repetitive avalanche current (I_{AR}) versus avalanche time (t_p)

Fig.19. Peak body recovery voltage dV/dt. The dV/dt = f(I_{DS}). The dI/dt is 100A/µs.

MECHANICAL DATA

Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line) **SOT533**





DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	E_1	e	e_1	L	Q
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	7.28 6.94	1.06 0.96	6.73 6.47	5.36 5.26	4.57	2.285	9.8 9.4	1.00 1.10

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT533		TO-251				99-02-18

Fig.20. SOT533 surface mounting package. Pin 2 connected to mounting base.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.