PowerMOS transistor PHT1N60R

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance. Intended for use in Compact Fluorescent Lights (CFL), electric shaver, battery charger and general purpose switching applications.

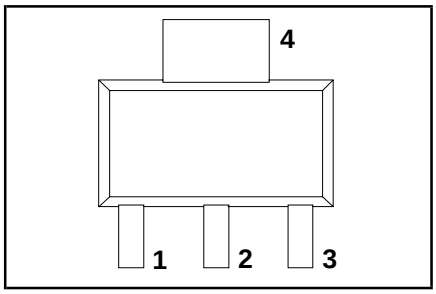
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	0.46	A
P_{tot}	Total power dissipation	1.8	W
$R_{DS(ON)}$	Drain-source on-state resistance	16.0	Ω

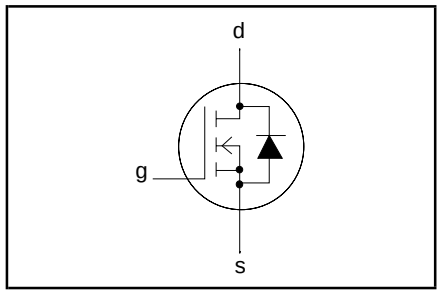
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	600	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{sp} = 25 ˚C	-	0.46	A
		T_{sp} = 100 ˚C	-	0.4	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 ˚C	-	1.84	A
I_{DR}	Source-drain diode current (DC)	T_{sp} = 25 ˚C	-	0.46	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{sp} = 25 ˚C	-	1.84	A
P_{tot}	Total power dissipation	T_{sp} = 25 ˚C	-	1.8	W
T_{stg}	Storage temperature		-55	150	˚C
T_j	Junction temperature		-	150	˚C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 0.46 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25˚C prior to surge	-	20	mJ
		T_j = 100˚C prior to surge	-	8	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 0.46 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 ˚C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point	surface mounted, FR4 board	12	15	K/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	surface mounted, FR4 board	70	-	K/W

STATIC CHARACTERISTICS

T_{sp} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	2.75	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 ˚C	-	7.5	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±35 V; V_{DS} = 0 V	-	16	80	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.23 A	-	13.6	16.0	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 0.5 A ;V_{GS} = 0 V	-	0.93	1.2	V

DYNAMIC CHARACTERISTICS

T_{sp} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 0.23 A	0.1	0.28	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	77	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Feedback capacitance		-	5	-	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 0.5 A; V_{DS} = 400 V	-	5	-	nC
Q_{gs}	Gate to source charge		-	0.5	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	3	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 0.5 A;	-	5	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	31	-	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	25	-	ns
t_f	Turn-off fall time		-	15	-	ns
t_{rr}	Source-drain diode Reverse recovery time	I_F = 0.46 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Source-drain diode Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.5	-	µC

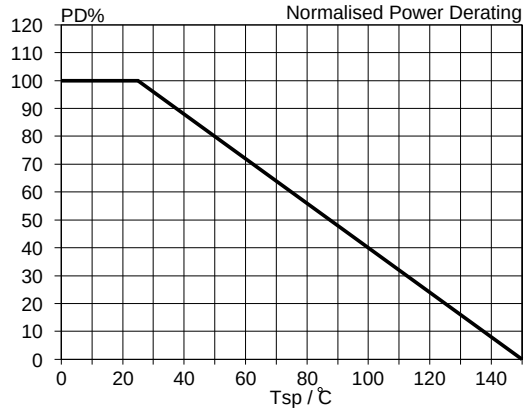


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25˚C}$ = f(T_{sp})

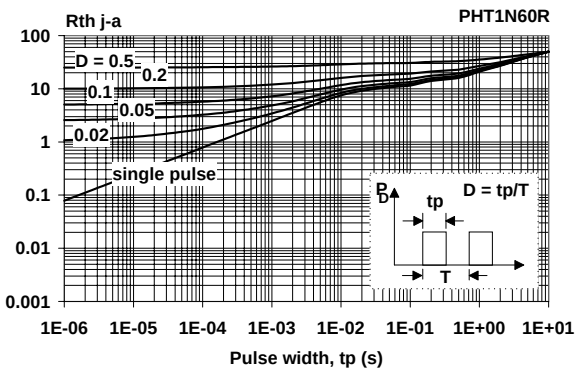


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}sp}$ = f(t); parameter D = t_p/T

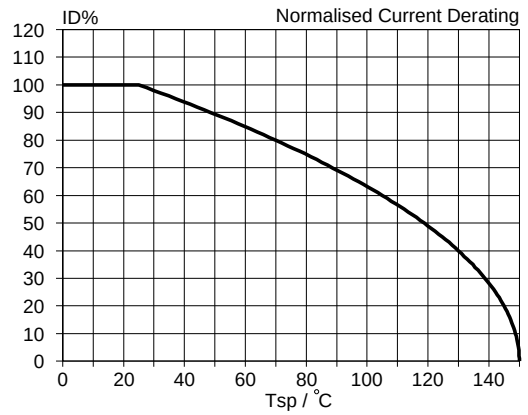


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{sp}); conditions: $V_{GS} \geq$ 10 V

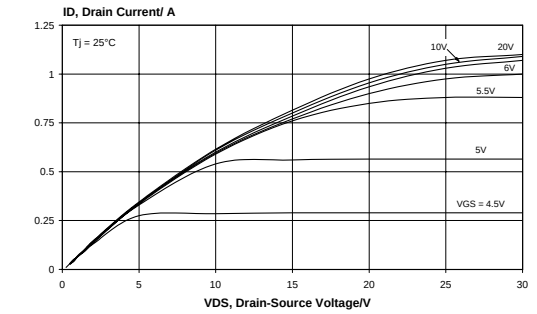


Fig.5. Typical output characteristics.
I_D = f(V_{DS}); parameter V_{GS}

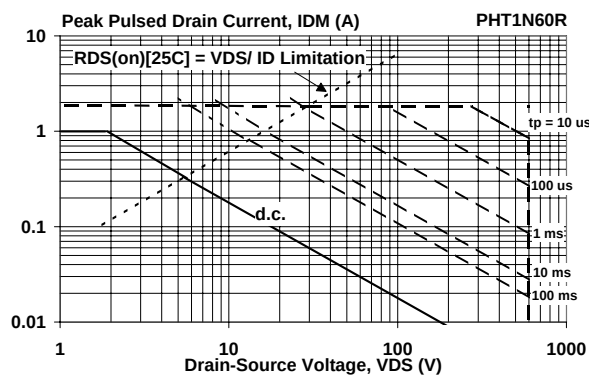


Fig.3. Safe operating area. T_{sp} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

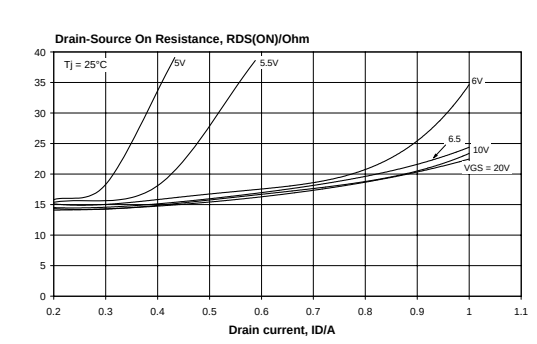


Fig.6. Typical on-state resistance.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

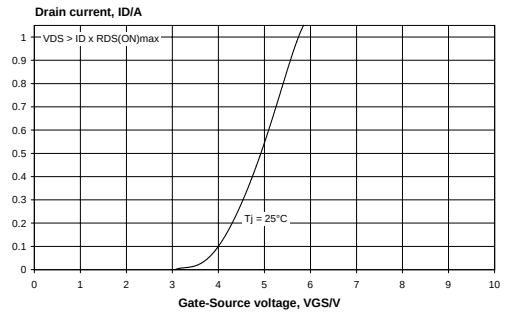


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

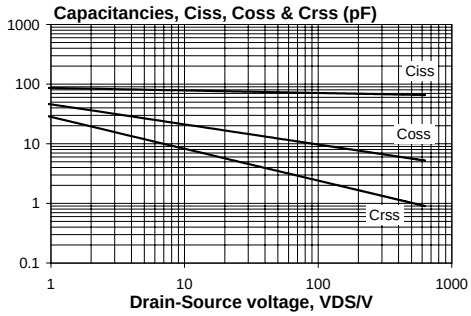


Fig.10. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

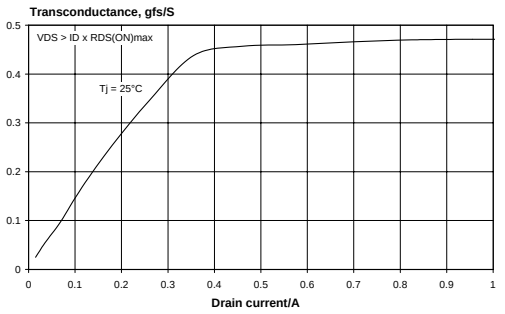


Fig.8. Typical transconductance. $g_{fs} = f(I_D)$; parameter T_j

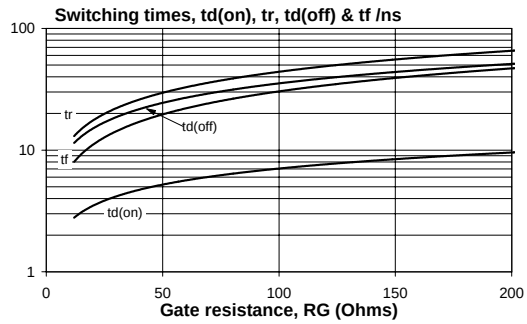


Fig.11. Typical switching times; $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

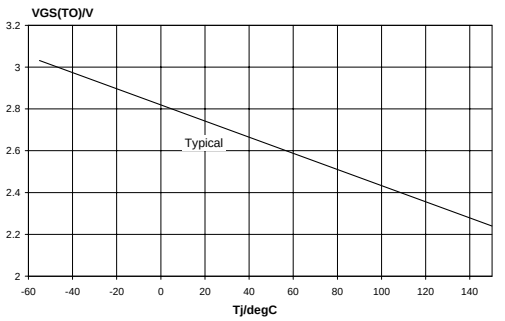


Fig.9. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

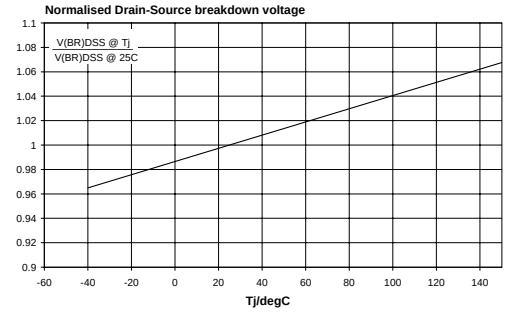
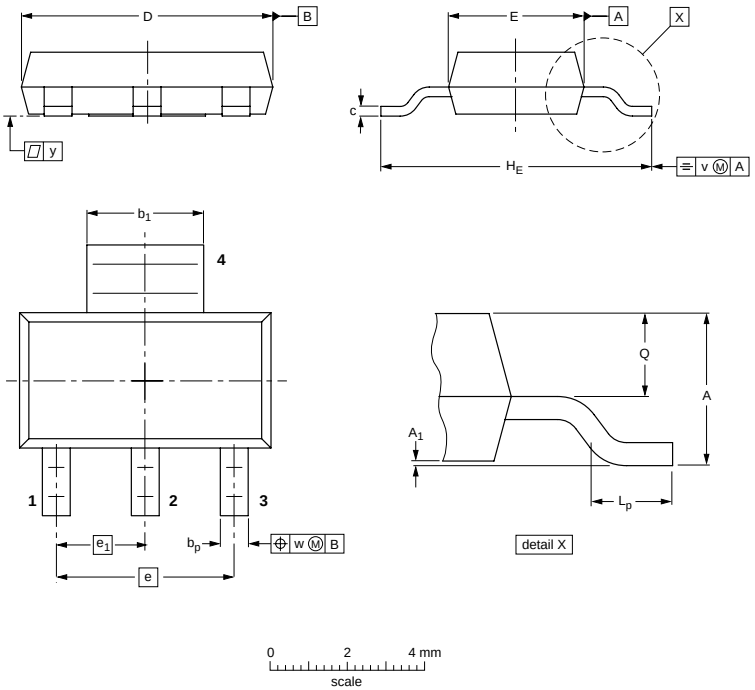


Fig.12. Normalised drain-source breakdown voltage; $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

MECHANICAL DATA

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Fig.13. SOT223 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Discrete Semiconductor Packages, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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