DATA SHEET

PHP212
Dual P-channel enhancement mode MOS transistor

Product specification
Supersedes data of 1996 Oct 23
File under Discrete Semiconductors, SC13b

1997 Jun 18

Philips Semiconductors

PHILIPS

Dual P-channel enhancement mode MOS transistor

PHP212

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

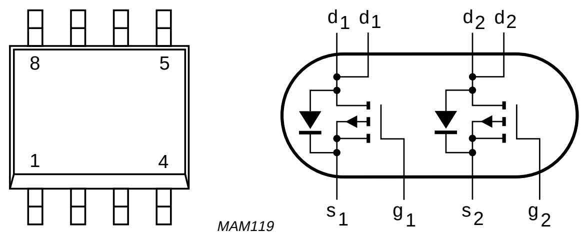


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–4	A
R_{DSon}	drain-source on-state resistance	I_D = –2 A; V_{GS} = –10 V	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–4	A
I_{DM}	peak drain current	note 2	–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.6	A
I_{SM}	peak pulsed source current	note 2	–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	20	K/W

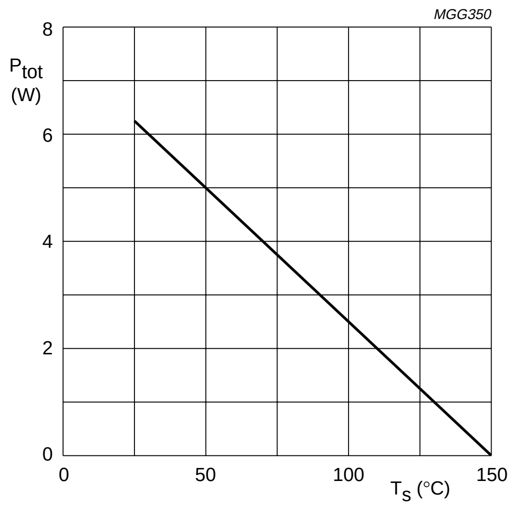
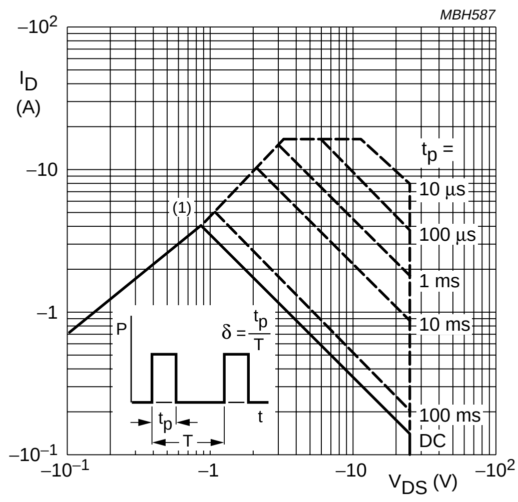


Fig.2 Power derating curve.



δ = 0.01; T_s = 80 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = –1 mA	–1	–	–2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –24 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –1 A	–	–	0.25	Ω
		V_{GS} = –10 V; I_D = –2 A	–	–	0.12	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = –10 V; V_{DD} = –15 V; I_D = –2 A	–	13	–	nC
Q_{GS}	gate-source charge	V_{GS} = –10 V; V_{DD} = –15 V; I_D = –2 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = –10 V; V_{DD} = –15 V; I_D = –2 A	–	4	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to –10 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	6	–	ns
t_r	rise time	V_{GS} = 0 to –10 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to –10 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	10	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = –10 to 0 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	29	–	ns
t_f	fall time	V_{GS} = –10 to 0 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	16	–	ns
t_{off}	turn-off switching time	V_{GS} = –10 to 0 V; V_{DD} = –15 V; I_D = –1 A; R_{gen} = 6 Ω; see Fig.4	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –1.25 A	–	–	–1.3	V
t_{rr}	reverse recovery time	I_S = –1.25 A; di/dt = 100 A/µs	–	75	–	ns

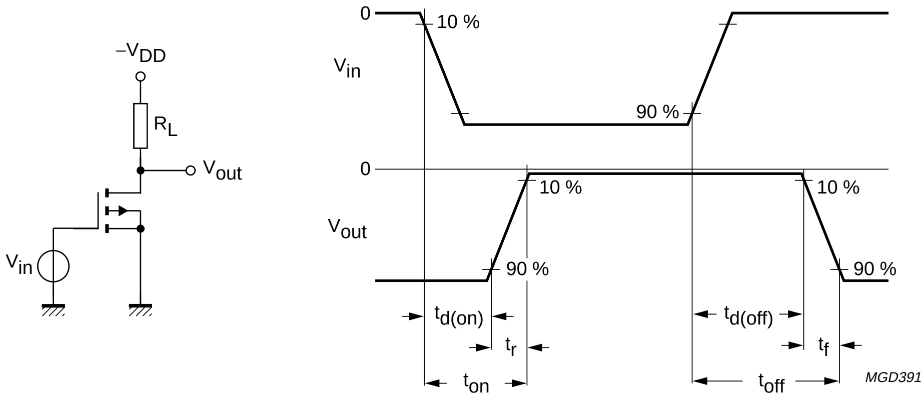
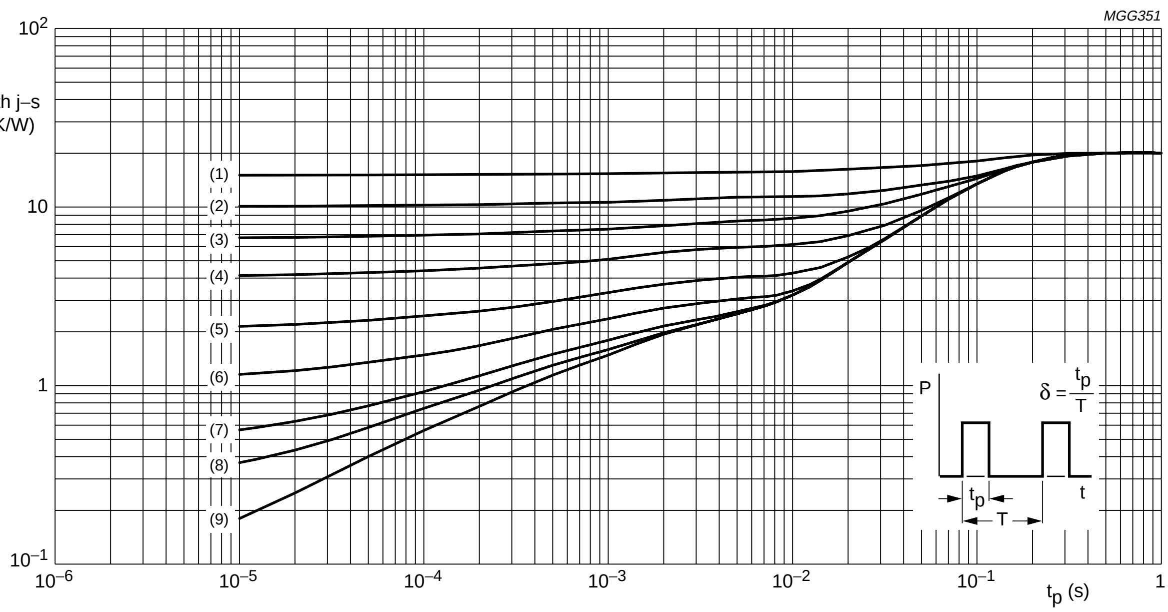


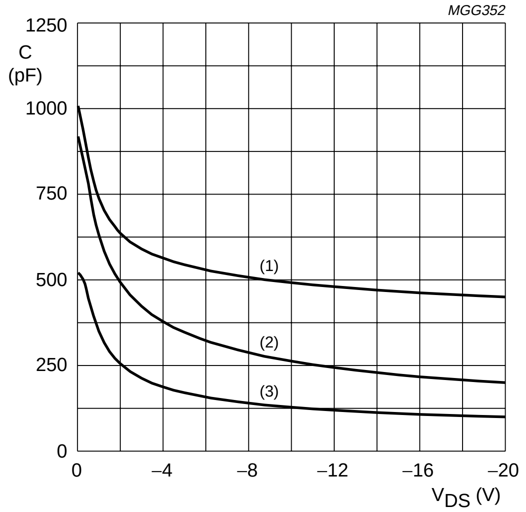
Fig.4 Switching times test circuit; input and output waveforms.



(1) $\delta = 0.75$. (2) $\delta = 0.5$. (3) $\delta = 0.33$. (4) $\delta = 0.2$.

(5) $\delta = 0.1$. (6) $\delta = 0.05$. (7) $\delta = 0.02$. (8) $\delta = 0.01$. (9) $\delta = 0$.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



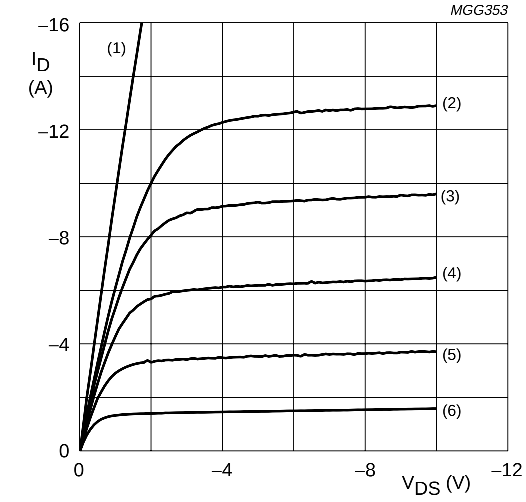
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

(1) C_{iss}.

(2) C_{oss}.

(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

(1) V_{GS} = −10 V.

(2) V_{GS} = −5 V.

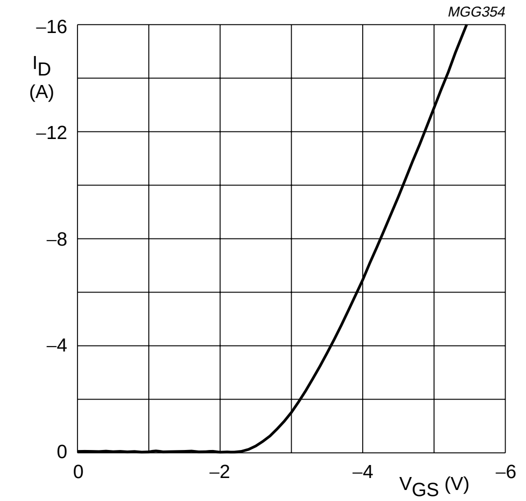
(3) V_{GS} = −4.5 V.

(4) V_{GS} = −4 V.

(5) V_{GS} = −3.5 V.

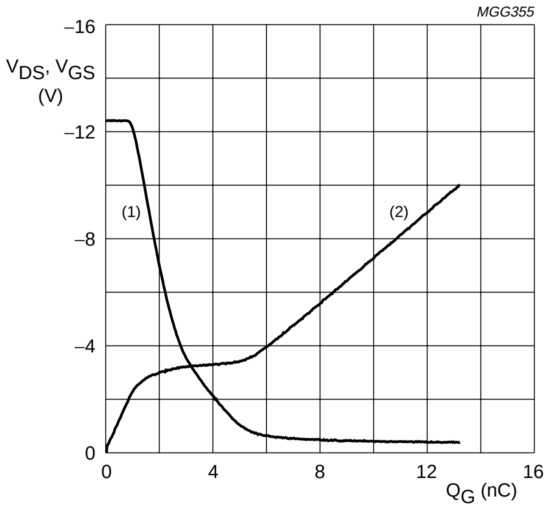
(6) V_{GS} = −3 V.

Fig.7 Output characteristics; typical values.



V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristic; typical value.

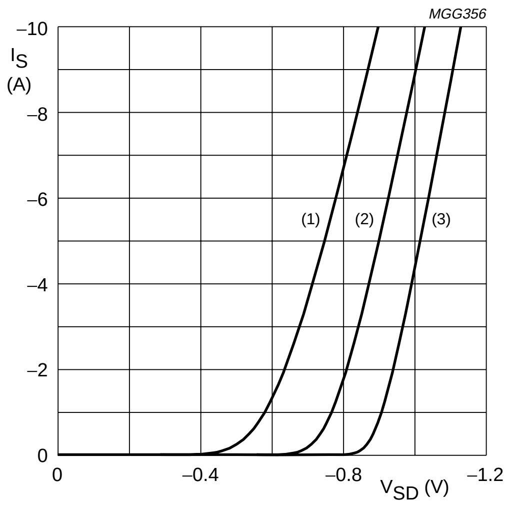


V_{DD} = −12.5 V; I_D = −2 A; T_{amb} = 25 °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.9 Gate-source voltage and drain-source voltage as functions of total gate charge; typical values.



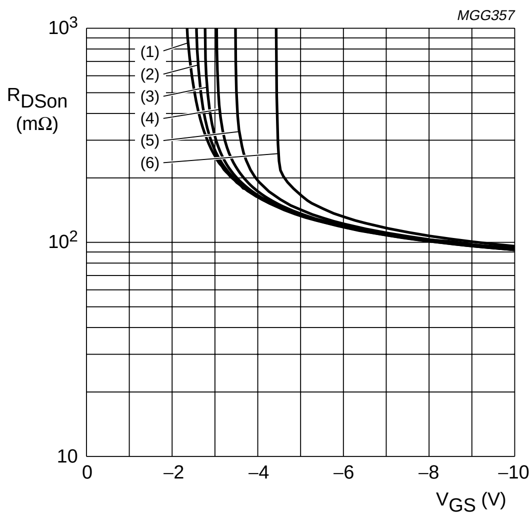
V_{GD} = 0.

(1) T_{amb} = 150 °C; t_p = 300 µs; δ = 0.

(2) T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

(3) T_{amb} = −65 °C; t_p = 300 µs; δ = 0.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.

$V_{DS} \geq I_D \times R_{DSon}$.

(1) I_D = 0.1 A.

(2) I_D = 0.5 A.

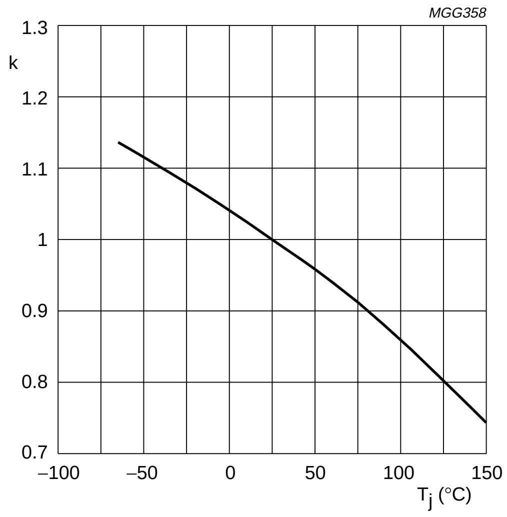
(3) I_D = 1 A.

(4) I_D = 2 A.

(5) I_D = 4 A.

(6) I_D = 8 A.

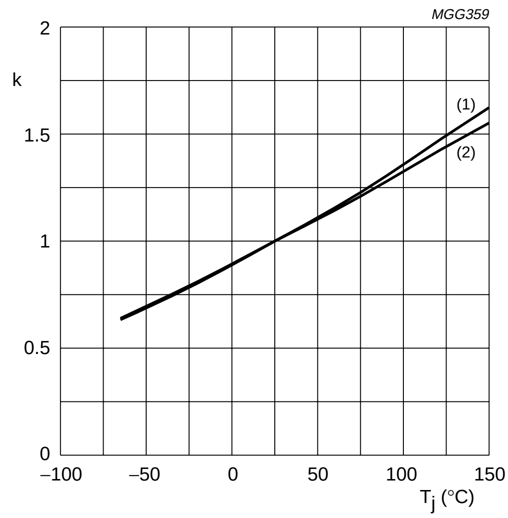
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

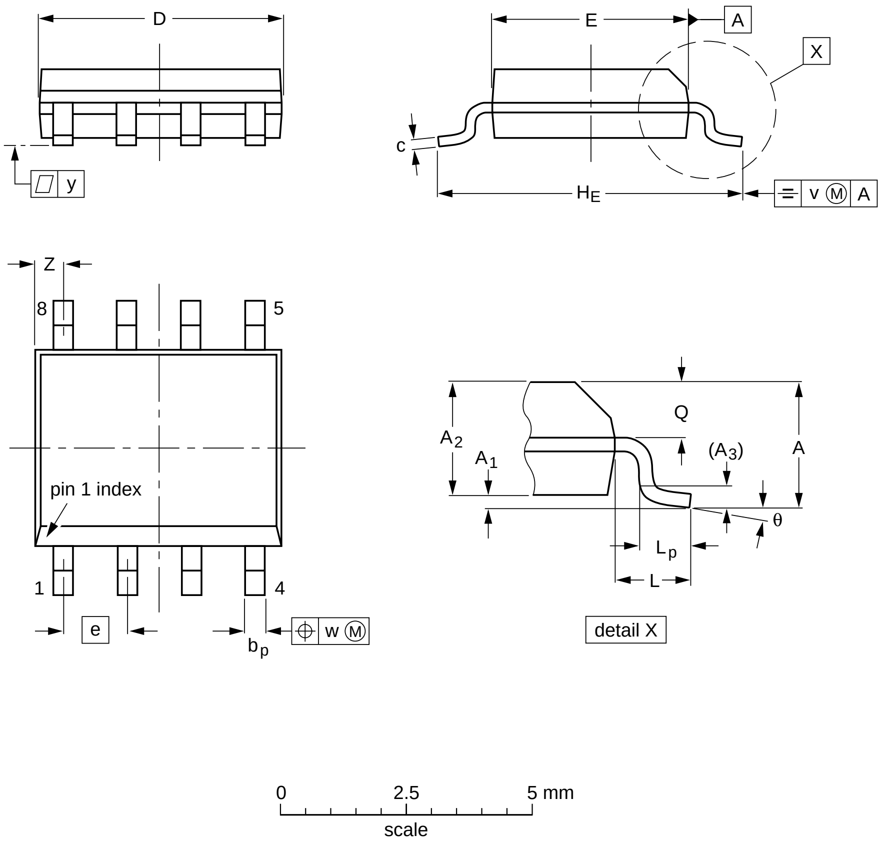
(1) R_{DSon} at $V_{GS} = -10$ V; $I_D = -2$ A.

(2) R_{DSon} at $V_{GS} = -4.5$ V; $I_D = -1$ A.

Fig.13 Temperature coefficient of drain-source on-state resistance; typical values.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm — **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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