DATA SHEET

PHN405
4 N-channel 60 mΩ FET array enhancement mode MOS transistors

Product specification
Supersedes data of 1997 Jun 19
File under Discrete Semiconductors, SC13

1998 Mar 17

Philips
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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Current monitoring.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Four enhancement mode MOS transistors in a 16-pin plastic SOT338-1 (SSOP16) package. Two transistors feature current monitoring (sense FETs).

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT338-1 (SSOP16)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9	g_3	gate 3
10	s_3	source 3
11 and 15	d_3	drain 3
12	m_3	current monitor 3
13	g_4	gate 4
14	s_4	source 4
16	m_4	current monitor 4

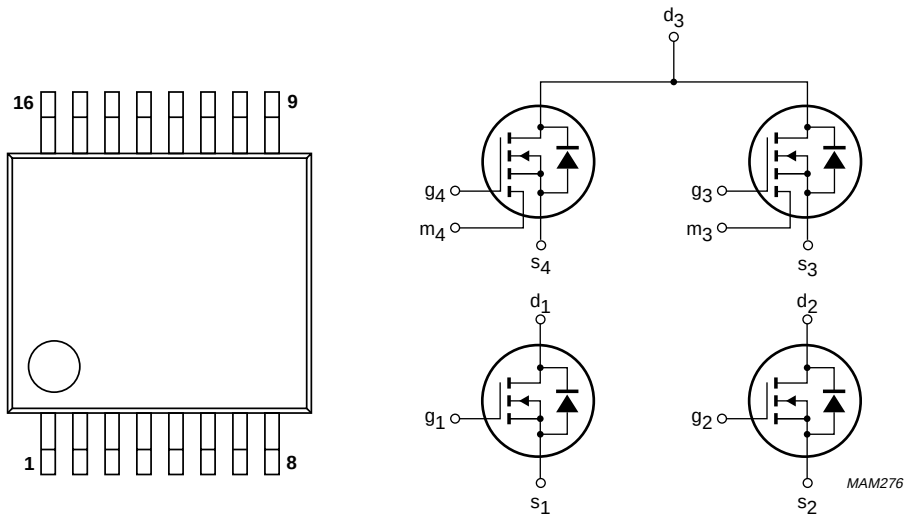

Fig.1 Simplified outline and symbol.

4 N-channel 60 mΩ FET array enhancement mode MOS transistors

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	3.7	A
R_{DSon}	drain-source on-state resistance	I_D = 2 A; V_{GS} = 10 V	–	60	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	1.4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	3.7	A
I_{DM}	peak drain current	note 2	–	14.8	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.4	W
		T_s = 80 °C; note 4	–	1.25	W
		T_s = 80 °C; note 5	–	1.09	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Current monitor					
I_M	monitor current (DC)	T_s = 80 °C	–	50	mA
I_{MM}	peak monitor current	note 2	–	220	mA
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1.4	A
I_{SM}	peak source current	note 2	–	5.6	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. When only one FET dissipates.
4. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
5. When all four FETs dissipate an equal amount of power.

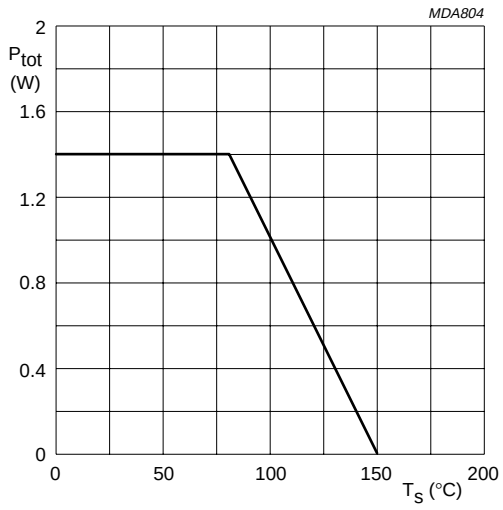
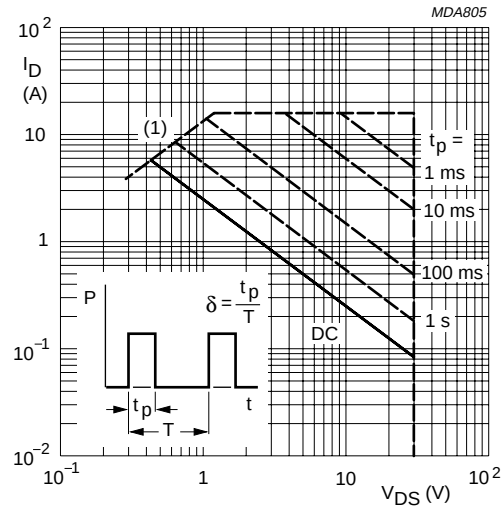


Fig.2 Power derating curve.



δ = 0.01; T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per FET				
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	50	K/W
		note 2	56	K/W
		note 3	64	K/W

Notes

1. When only one FET dissipates.
2. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
3. When all four FETs dissipate an equal amount of power.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	–	120	mΩ
		V_{GS} = 10 V; I_D = 2 A	–	–	60	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	230	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	90	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1 A	–	7.1	10	nC
Q_{GS}	gate-source charge	V_{DD} = 15 V; I_D = 1 A;	–	0.5	–	nC
Q_{GD}	gate-drain charge	V_{DD} = 15 V; I_D = 1 A;	–	2.4	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	3.5	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	10	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	12	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	30	ns
Current monitor						
R_{DMon}	on-state drain-monitor resistance	V_{GM} = 10 V; I_D = 25 mA; I_S = 0	–	–	4	Ω
		V_{GM} = 4.5 V; I_D = 12 mA; I_S = 0	–	–	8	Ω
I_S/I_M	source to monitor current ratio	V_{GS} = 10 V; I_D = 2 A; V_{MS} = 0	–	66.7	–	
C_{Moss}	output capacitance of monitor cells	V_{GM} = V_{MS} = 0; V_{DS} = 24 V; f = 1 MHz	–	1.35	–	pF
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = –100 A/μs	–	25	–	ns

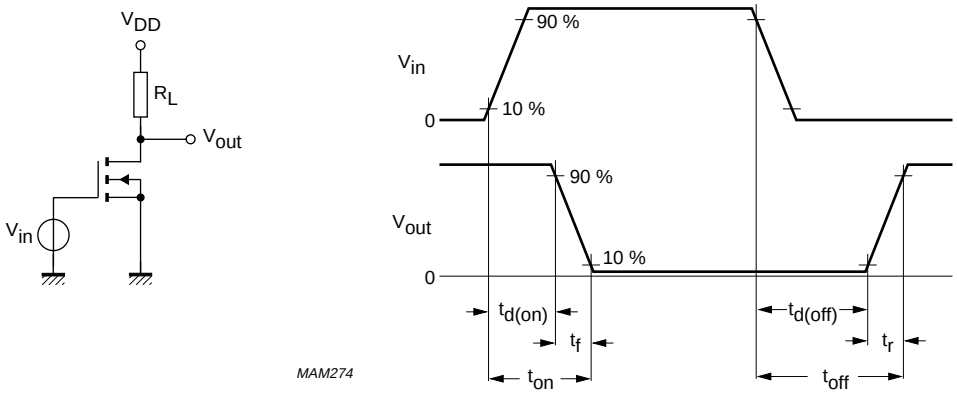


Fig.4 Switching times test circuit with input and output waveforms.

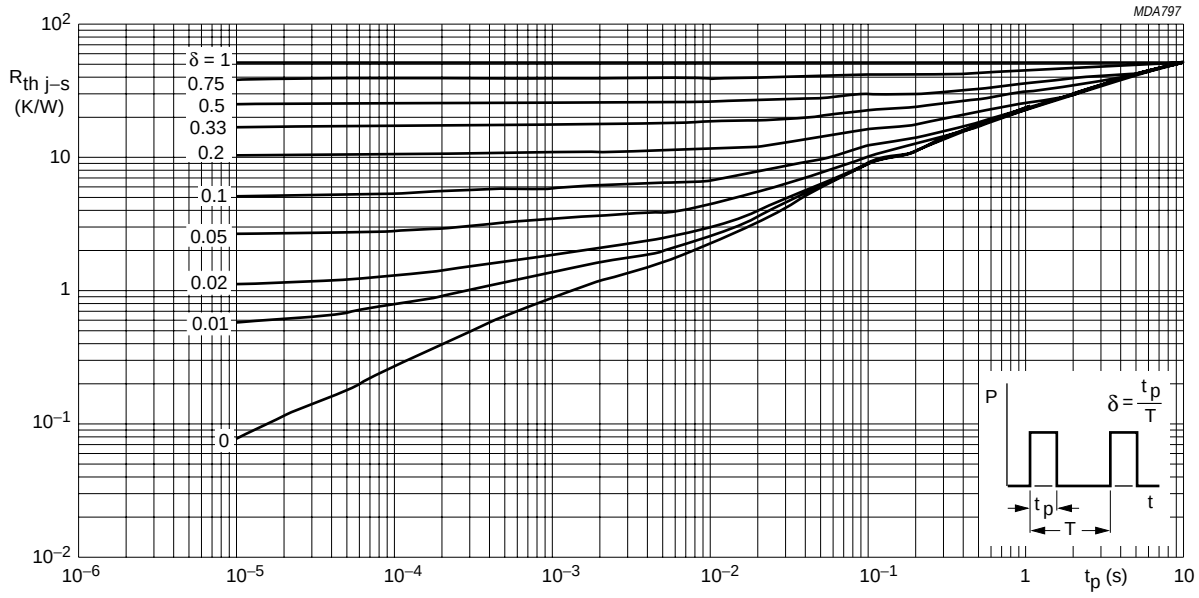
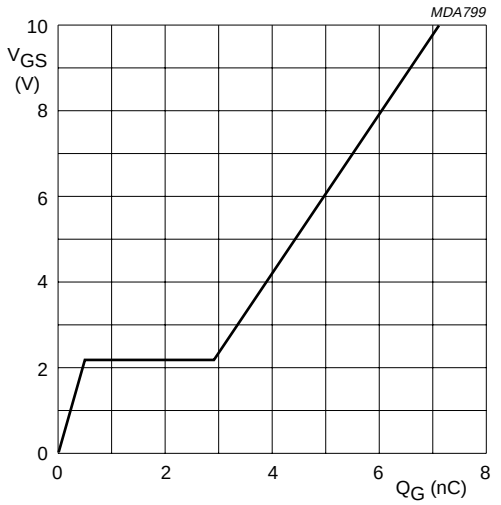
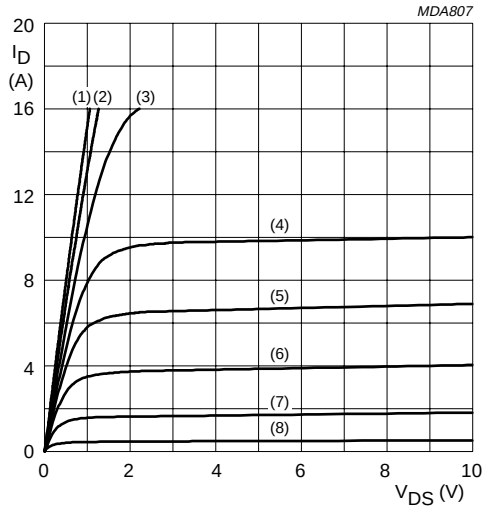


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



V_{DD} = 15 V; I_D = 1 A; T_{amb} = 25 °C.

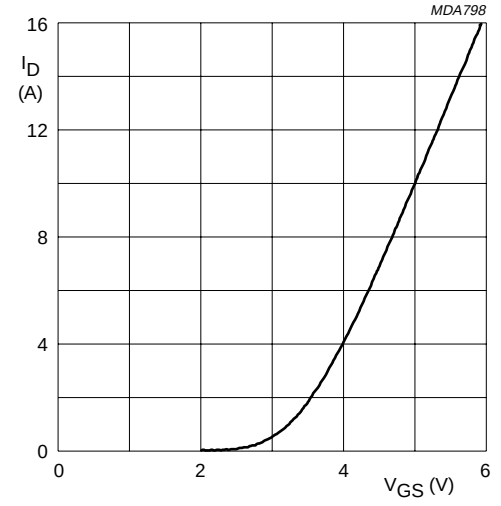
Fig.6 Gate-source voltage as a function of total gate charge; typical values.



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

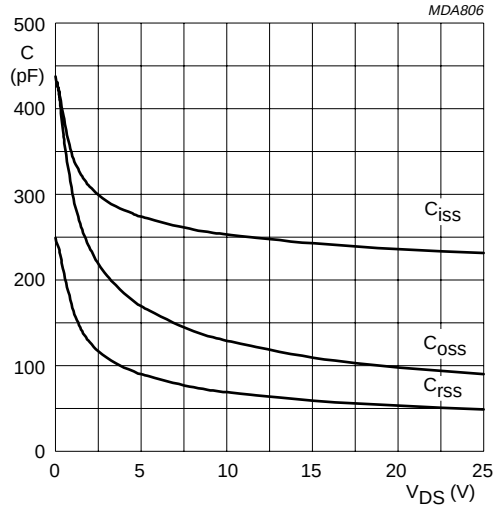
(1) V_{GS} = 10 V.
(2) V_{GS} = 7.5 V.
(3) V_{GS} = 6 V.
(4) V_{GS} = 5 V.
(5) V_{GS} = 4.5 V.
(6) V_{GS} = 4 V.
(7) V_{GS} = 3.5 V.
(8) V_{GS} = 3 V.

Fig.7 Output characteristics; typical values.



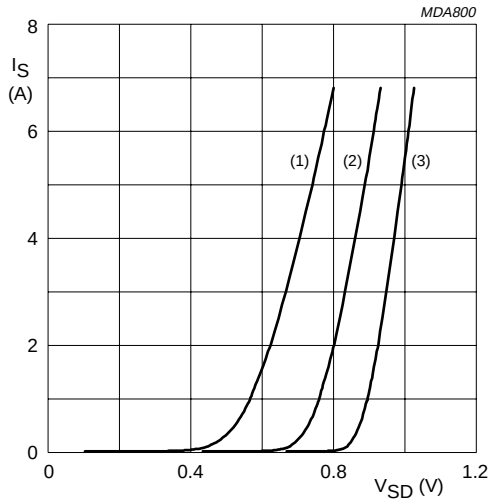
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristic; typical values.



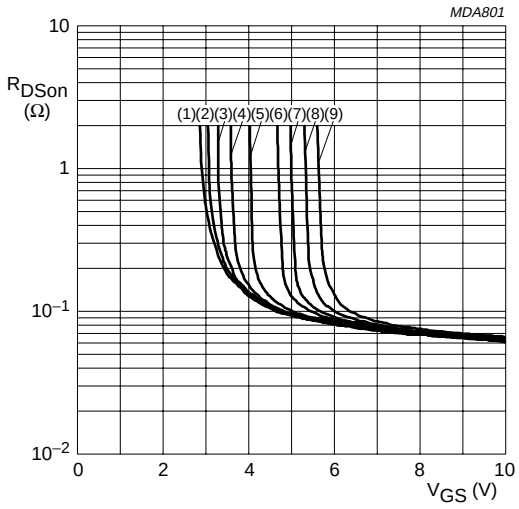
V_{GS} = 0 ; f = 1 MHz; T_j = 25 °C.

Fig.9 Capacitance as a function of drain-source voltage; typical values.



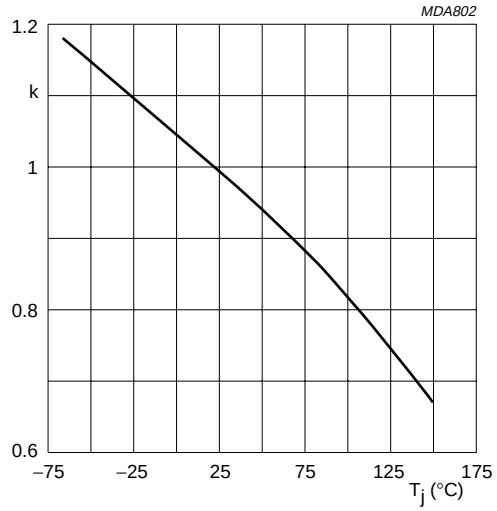
t_p = 300 µs; δ = 0.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –65 °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



T_{amb} = 25 °C; t_p = 300 µs; δ = 0.
(1) I_D = 0.25 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2 A.
(5) I_D = 4 A.
(6) I_D = 8 A.
(7) I_D = 10 A.
(8) I_D = 13 A.
(9) I_D = 16 A.

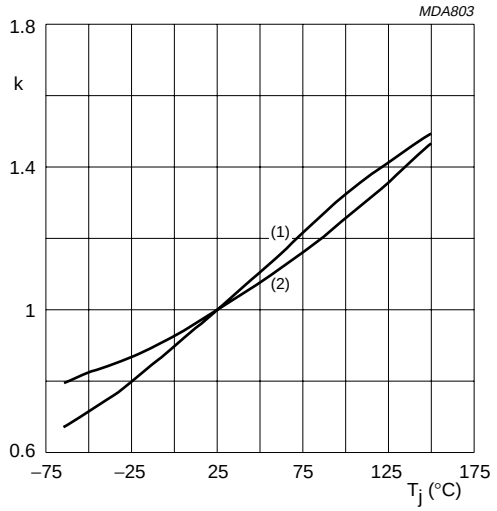
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; I_D = 1 mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at:

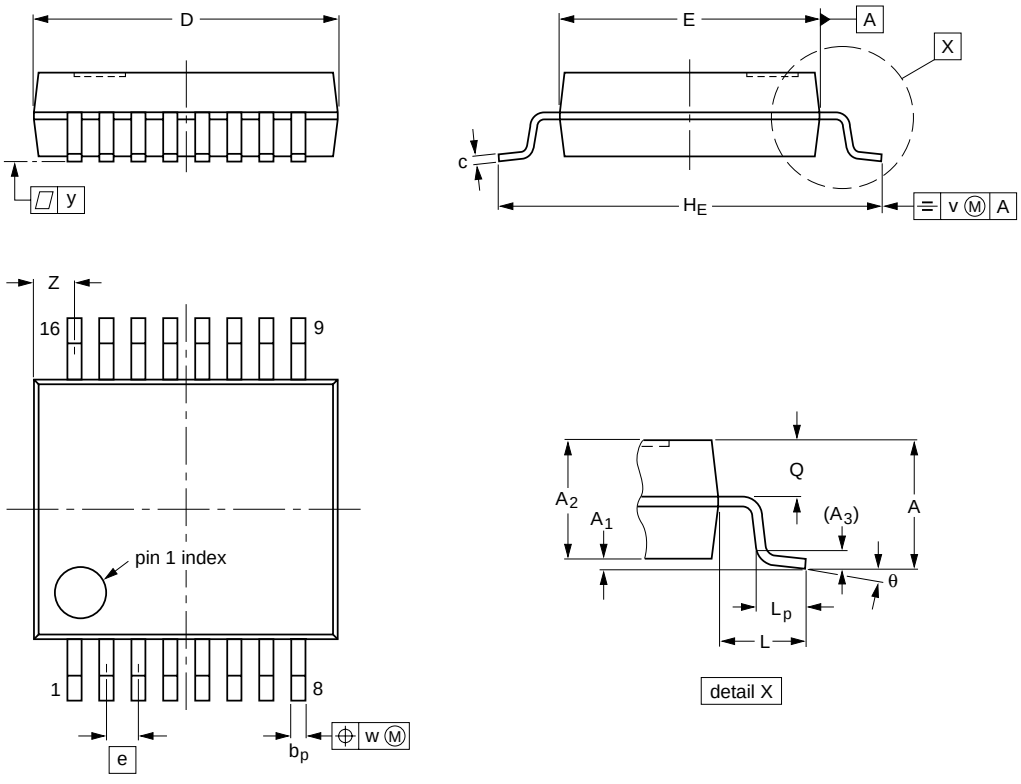
(1) V_{GS} = 10 V; I_D = 2 A.

(2) V_{GS} = 4.5 V; I_D = 1 A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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