

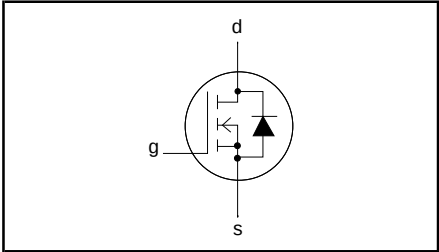
N-channel TrenchMOS™ transistor

PHX9NQ20T , PHF9NQ20T

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 200\text{ V}$
$I_D = 5.2\text{ A}$
$R_{DS(ON)} \leq 400\text{ m}\Omega$

GENERAL DESCRIPTION

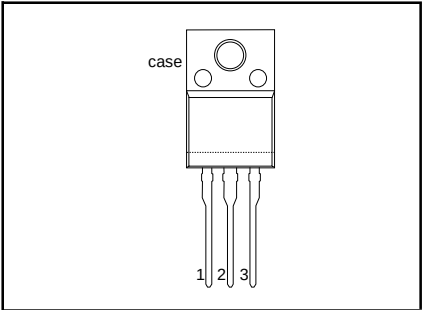
N-channel, enhancement mode field-effect power transistor using **Trench** technology, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHX9NQ20T is supplied in the SOT186A (FPAK) conventional leaded package

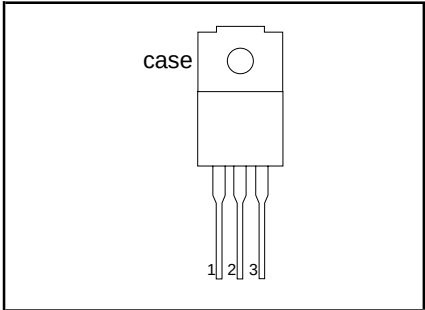
PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A (FPAK)



SOT186 (FPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$	-	200	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{hs} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$	-	5.2	A
		$T_{hs} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$	-	3.3	A
I_{DM}	Pulsed drain current	$T_{hs} = 25\text{ }^{\circ}\text{C}$	-	21	A
P_D	Total power dissipation	$T_{hs} = 25\text{ }^{\circ}\text{C}$	-	25	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	$^{\circ}\text{C}$

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 7.2A$; $t_p = 100 \mu s$; T_j prior to avalanche = $25^\circ C$; $V_{DD} \leq 25 V$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 V$; refer to fig;15	-	93	mJ
I_{AS}	Peak non-repetitive avalanche current		-	8.7	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th j-hs}$	Thermal resistance junction to mounting base		-	-	5	K/W
$R_{th j-a}$	Thermal resistance junction to ambient	SOT186A package, in free air	-	55	-	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V$; $I_D = 0.25 mA$; $T_j = -55^\circ C$	200 178	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1 mA$; $T_j = 150^\circ C$ $T_j = -55^\circ C$	2 1 -	3 - -	4 - 6	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 4.5 A$; $T_j = 150^\circ C$	- -	300 -	400 0.94	m Ω Ω
g_{fs}	Forward transconductance	$V_{DS} = 25 V$; $I_D = 4.5 A$	3.8	6	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10 V$; $V_{DS} = 0 V$	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200 V$; $V_{GS} = 0 V$; $T_j = 150^\circ C$	- -	0.05 -	10 500	μA μA
$Q_{g(tot)}$	Total gate charge	$I_D = 9 A$; $V_{DD} = 160 V$; $V_{GS} = 10 V$	-	24	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 100 V$; $R_D = 10 \Omega$; $V_{GS} = 10 V$; $R_G = 5.6 \Omega$	-	8	-	ns
t_r	Turn-on rise time		-	19	-	ns
t_{doff}	Turn-off delay time	Resistive load	-	25	-	ns
t_f	Turn-off fall time		-	15	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0 V$; $V_{DS} = 25 V$; $f = 1 MHz$	-	959	-	pF
C_{oss}	Output capacitance		-	93	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	8.7	A
I_{SM}	Pulsed source current (body diode)		-	-	35	A
V_{SD}	Diode forward voltage	$I_F = 9\text{ A}$; $V_{GS} = 0\text{ V}$	-	0.85	1.2	V
t_{rr}	Reverse recovery time	$I_F = 9\text{ A}$; $-di_F/dt = 100\text{ A}/\mu\text{s}$;	-	92	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10\text{ V}$; $V_R = 25\text{ V}$	-	0.5	-	μC

ISOLATION LIMITING VALUE & CHARACTERISTIC $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	SOT186A package; $f = 50\text{-}60\text{ Hz}$; sinusoidal waveform; R.H. $\leq 65\%$; clean and dustfree	-		2500	V
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	SOT186 package; R.H. $\leq 65\%$; clean and dustfree	-		1500	V
C_{isol}	Capacitance from pin 2 to external heatsink	$f = 1\text{ MHz}$	-	10	-	pF

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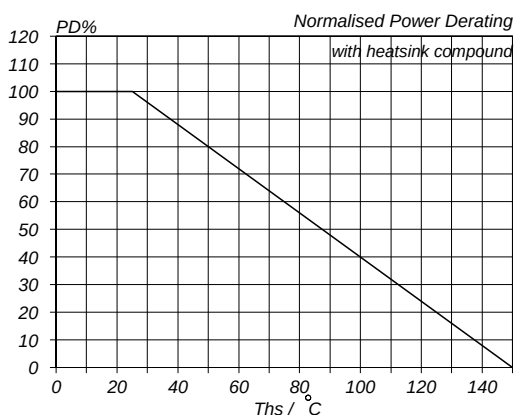


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D 25 ^\circ\text{C}} = f(T_{mb})$

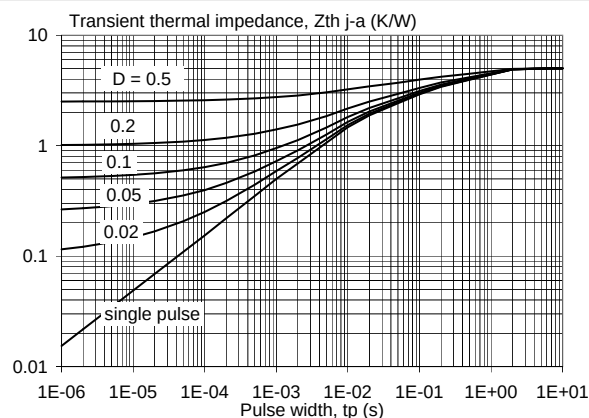


Fig.4. Transient thermal impedance.
 $Z_{th j-mb} = f(t)$; parameter $D = t_p / T$

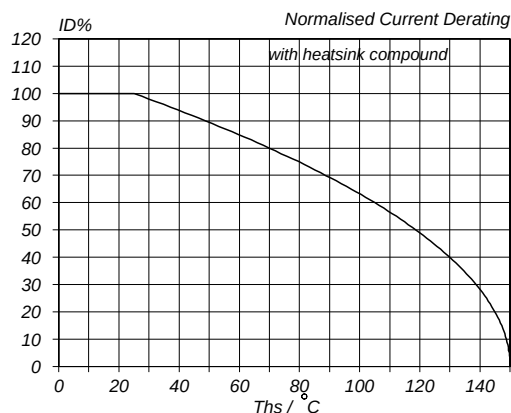


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D 25 ^\circ\text{C}} = f(T_{mb})$; $V_{GS} \geq 10 \text{ V}$

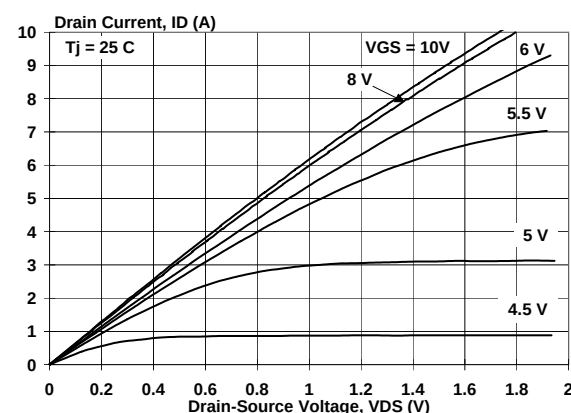


Fig.5. Typical output characteristics, $T_j = 25 ^\circ\text{C}$.
 $I_D = f(V_{DS})$

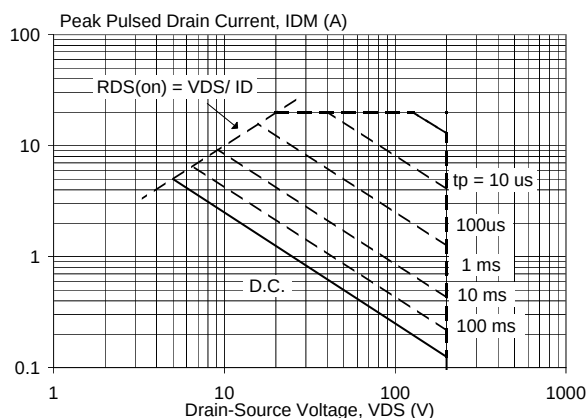


Fig.3. Safe operating area
 $I_D \text{ \& } I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

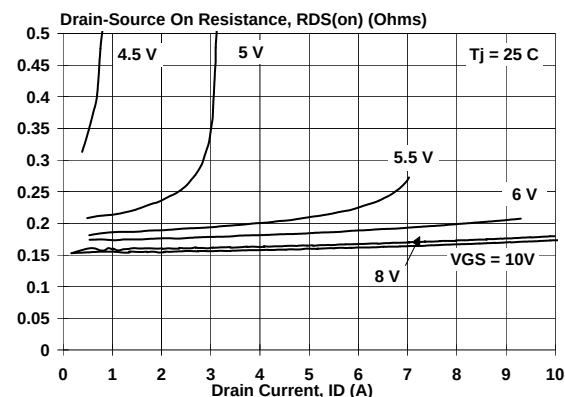


Fig.6. Typical on-state resistance, $T_j = 25 ^\circ\text{C}$.
 $R_{DS(on)} = f(I_D)$

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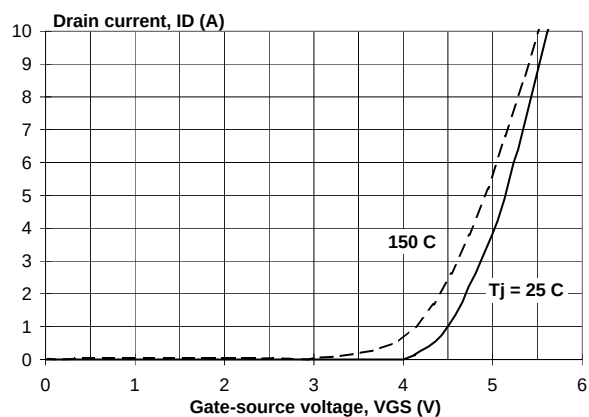


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$

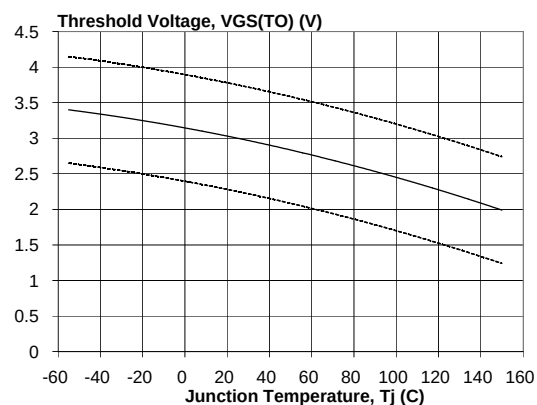


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

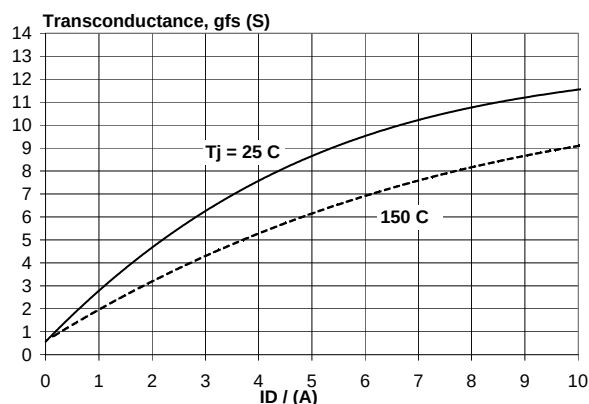


Fig. 8. Typical transconductance, $T_j = 25 \text{ }^\circ\text{C}$.
 $g_{fs} = f(I_D)$

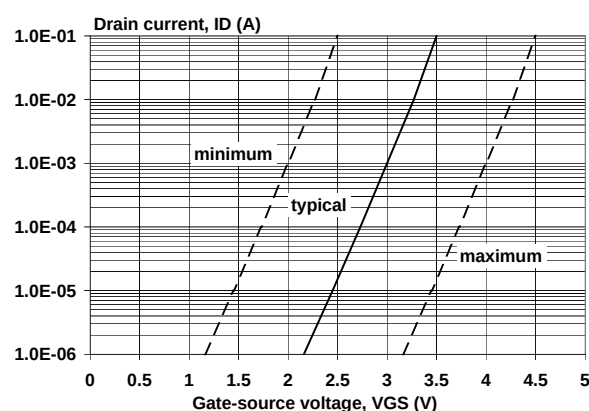


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25 \text{ }^\circ\text{C}$

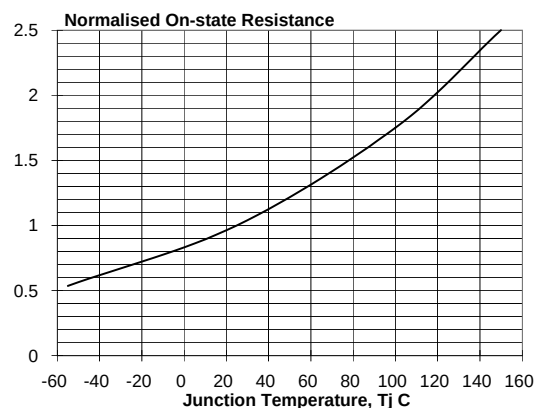


Fig. 9. Normalised drain-source on-state resistance.
 $R_{DS(ON)}/R_{DS(ON)25 \text{ }^\circ\text{C}} = f(T_j)$

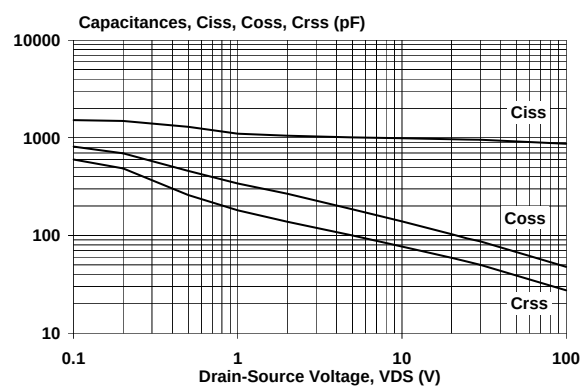
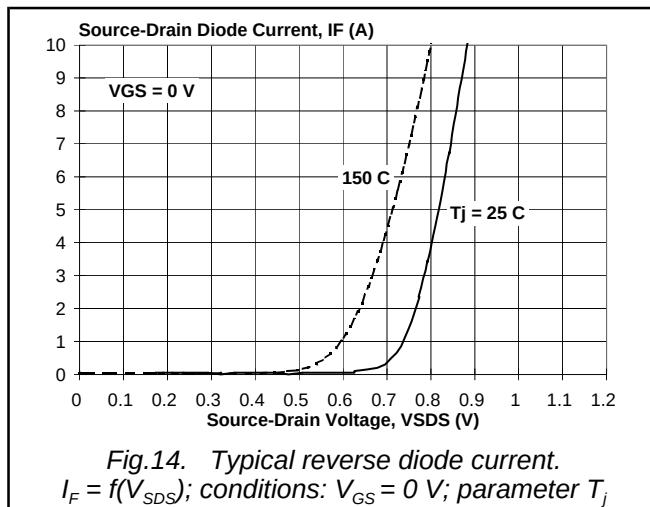
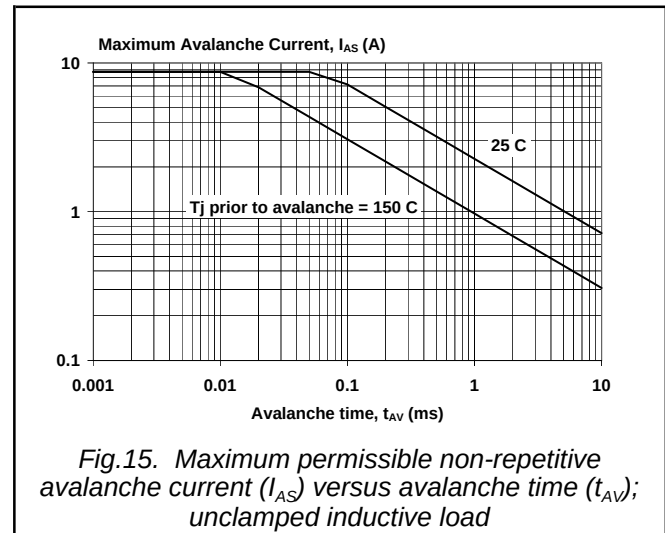
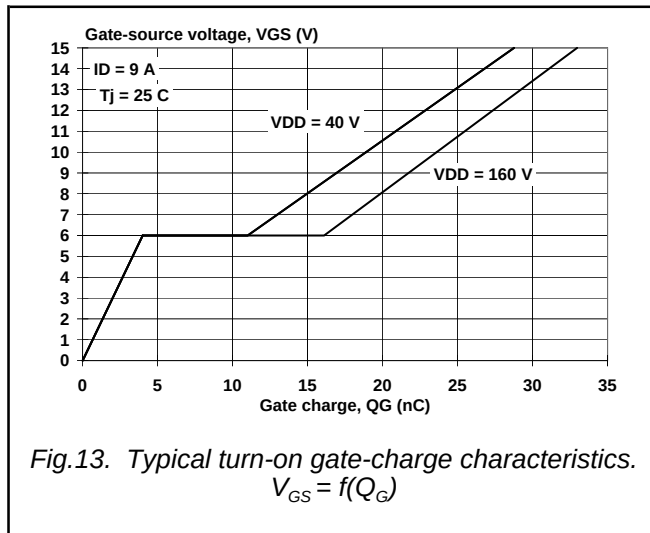


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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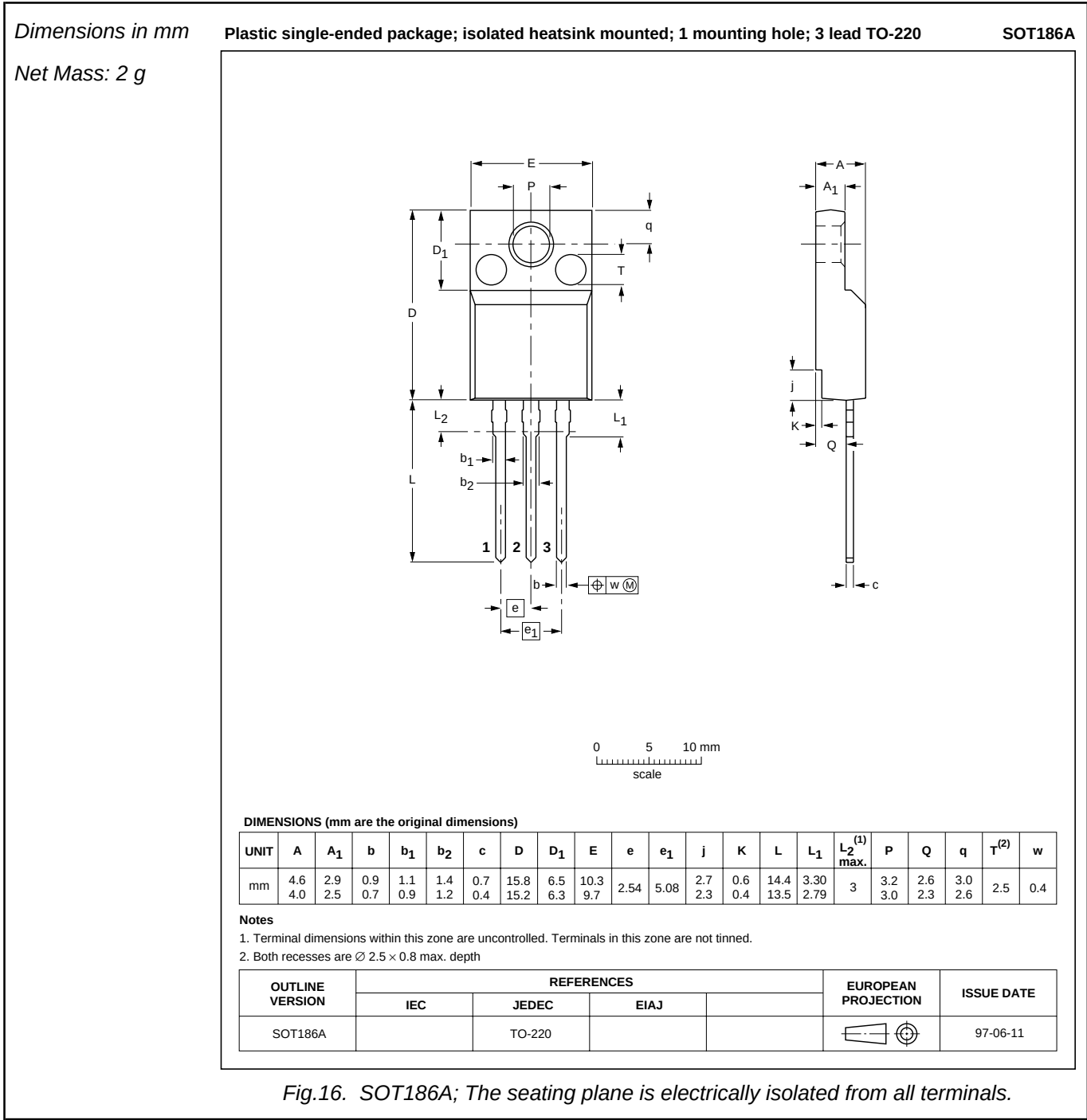
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MECHANICAL DATA



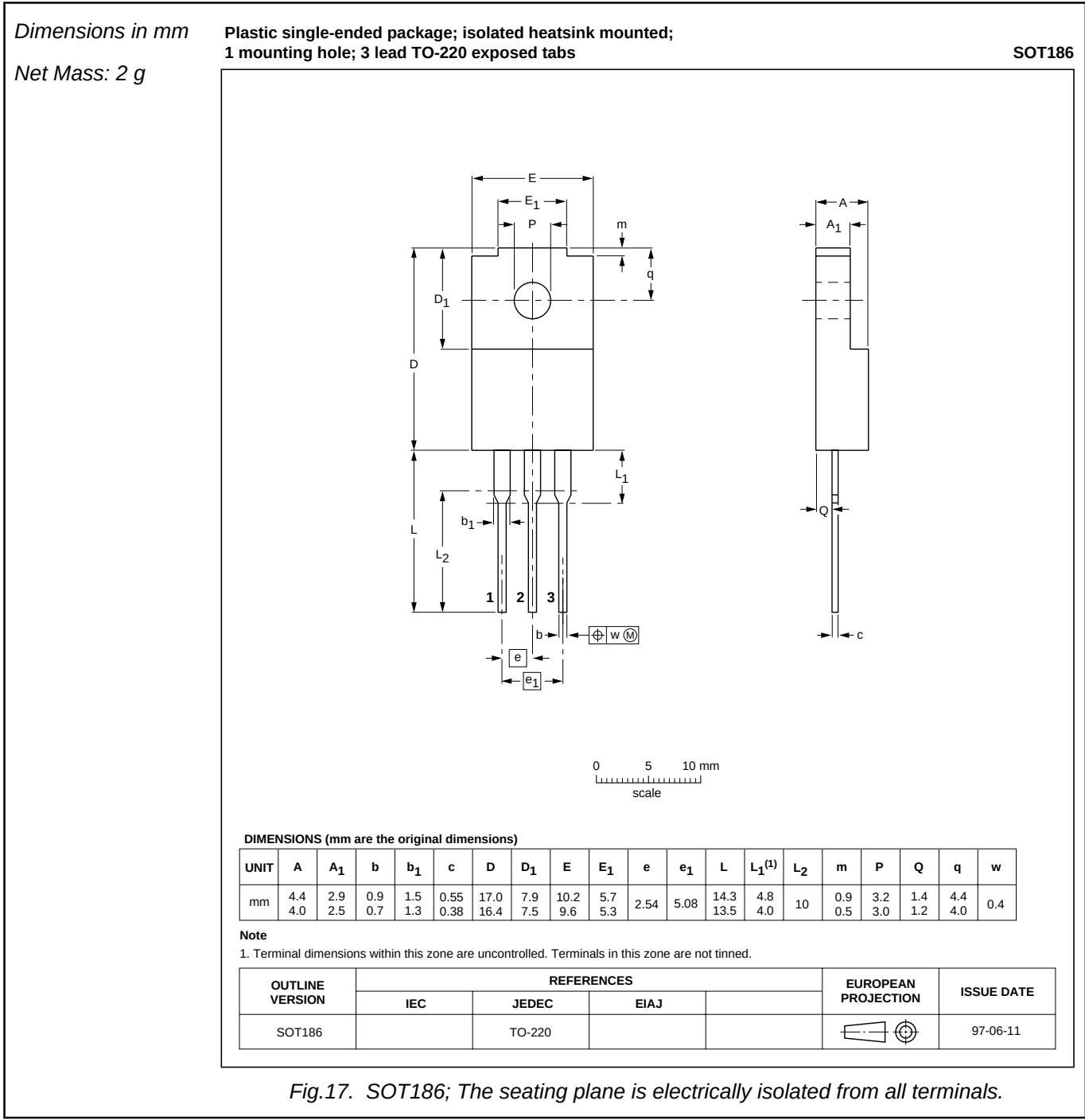
Notes

- 1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
- 2. Refer to mounting instructions for F-pack envelopes.
- 3. Epoxy meets UL94 V0 at 1/8".

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N-channel TrenchMOSTM transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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