PHD24N03LT

N-channel enhancement mode field-effect transistor

Rev. 02 — 27 July 2000 **Product specification**

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™[1] technology.

Product availability:

PHD24N03LT in SOT428 (D-PAK).

2. Features

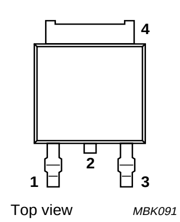
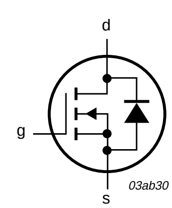
- TrenchMOS™ technology
- Low on-state resistance
- Avalanche ruggedness rated
- Logic level compatible
- Surface mount package.

3. Applications

- DC to DC converter
- High speed, low resistance switch

4. Pinning information

Table 1: Pinning - SOT428, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 **SOT428 (D-PAK)**	 **N-channel MOSFET**
2	drain (d) [1]		
3	source (s)		
4	mounting base, connected to drain (d)		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.

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5. Quick reference data

Table 2: Quick reference data

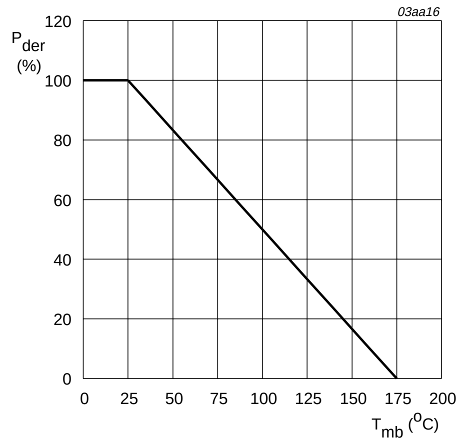
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 °C	–	30	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V	–	20	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	37.5	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	28	50	mΩ
		V_{GS} = 5 V; I_D = 10 A	38	56	mΩ

6. Limiting values

Table 3: Limiting values

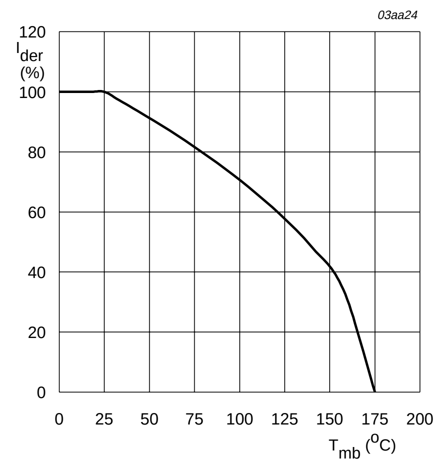
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 °C	–	30	V
V_{DGR}	drain-gate voltage (DC)	T_j = 25 to 175 °C; R_{GS} = 20 kΩ	–	30	V
V_{GS}	gate-source voltage (DC)		–	±15	V
V_{GSM}	peak gate-source voltage	t_p ≤ 50 µs; pulsed; duty cycle = 25%	–	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	–	20	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2	–	14	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	–	80	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	–	37.5	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	–	20	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	–	80	A
Avalanche ruggedness limiting values					
E_{AS}	non-repetitive avalanche energy	unclamped inductive load; I_D = 19 A; t_p = 0.2 ms; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 5 V; starting T_j = 25 °C; Figure 4	–	74	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; V_{DD} ≤ 15 V; R_{GS} = 50 Ω; V_{GS} = 5 V; Figure 4	–	20	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

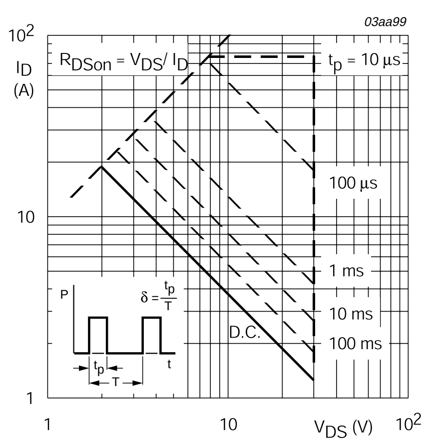
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

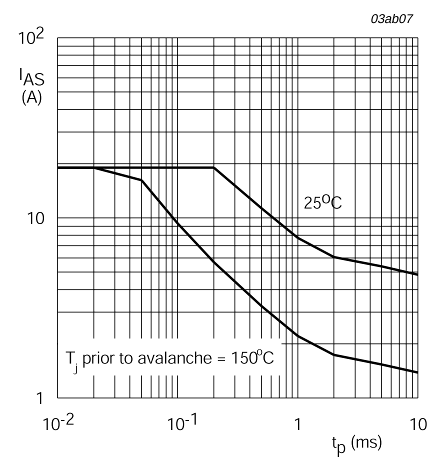
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.



Unclamped inductive load; $V_{DD} \leq 15$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 5$ V; starting T_j = 25°C and 150°C.

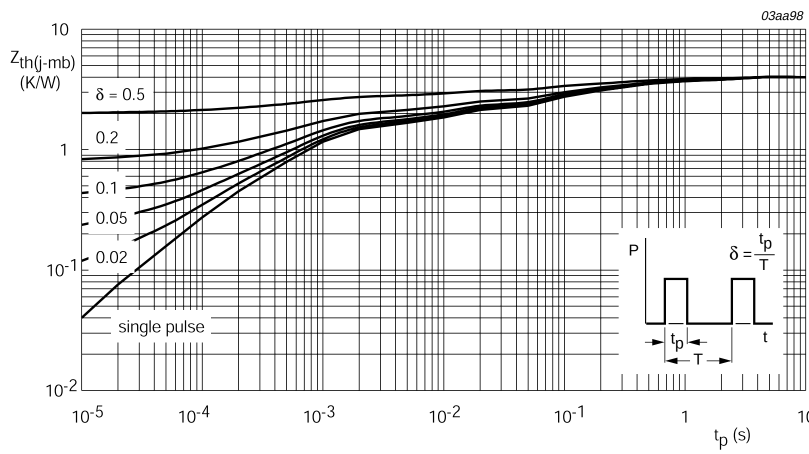
Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	mounted on a metal clad substrate; Figure 5	4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	50	K/W

7.1 Transient thermal impedance



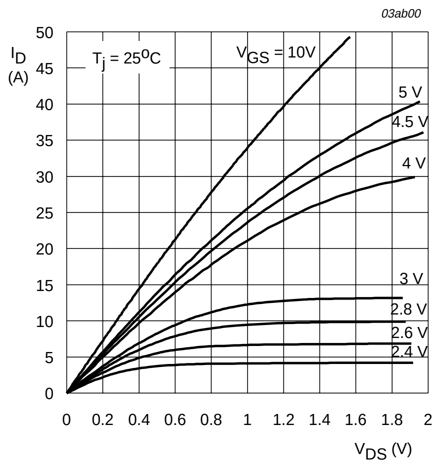
Mounted on a metal clad substrate.

Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

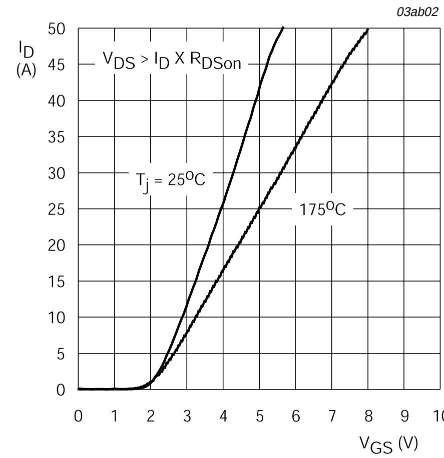
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	40	–	V
		T_j = –55 °C	27	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	–	–	V
		T_j = –55 °C	–	–	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	–	0.05	10	µA
		T_j = 175 °C	–	5.0	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	–	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; Figure 8 and 9				
		T_j = 25 °C	–	28	50	mΩ
		V_{GS} = 5 V; I_D = 10 A; Figure 8 and 9				
		T_j = 25 °C	–	38	56	mΩ
		T_j = 175 °C	–	70	104	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A; Figure 12	–	13	–	S
$Q_{g(tot)}$	total gate charge	I_D = 20 A; V_{DS} = 15 V; V_{GS} = 5 V; Figure 15	–	10	–	nC
Q_{gs}	gate-source charge		–	2.7	–	nC
Q_{gd}	gate-drain (Miller) charge		–	5.7	–	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 13	–	460	–	pF
C_{oss}	output capacitance		–	143	–	pF
C_{rss}	reverse transfer capacitance		–	107	–	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_D = 0.75 Ω; V_{GS} = 5 V; R_G = 10 Ω	–	18	–	ns
t_r	turn-off rise time		–	130	–	ns
$t_{d(off)}$	turn-off delay time		–	22	–	ns
t_f	turn-off fall time		–	45	–	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 14	–	0.95	1.5	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	–	65	–	ns
Q_r	recovered charge		–	75	–	nC



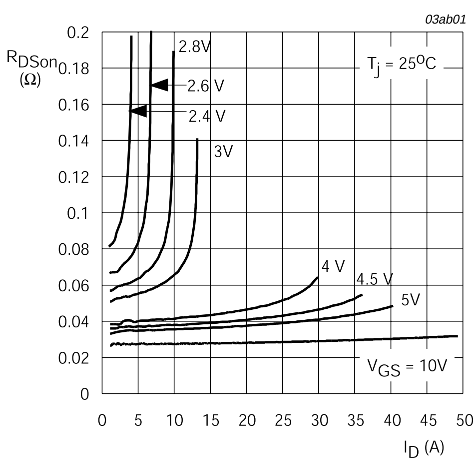
$T_j = 25\ °C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



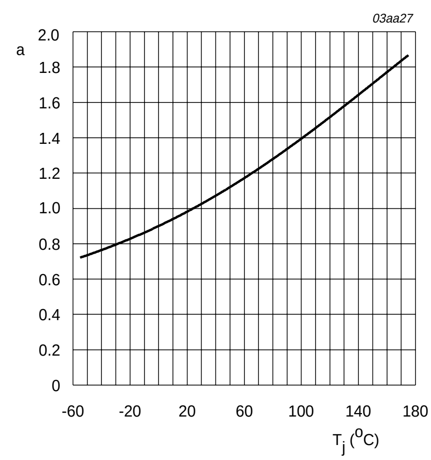
$T_j = 25\ °C$ and $175\ °C$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\ °C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.

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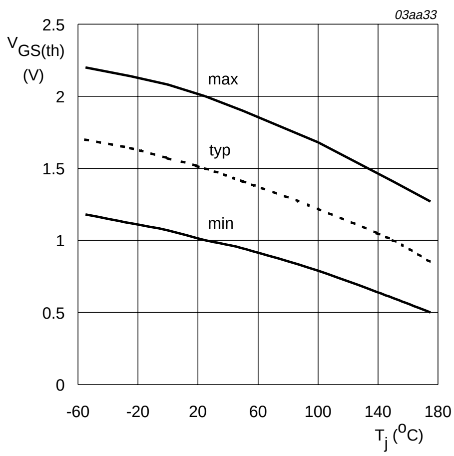
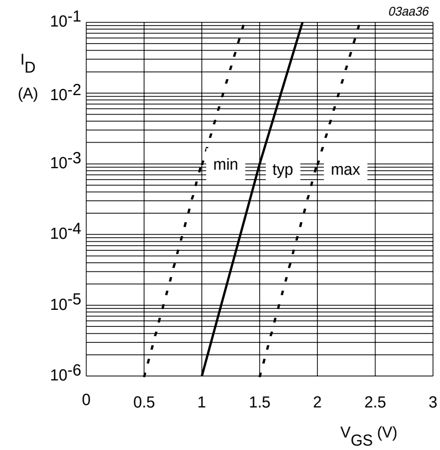


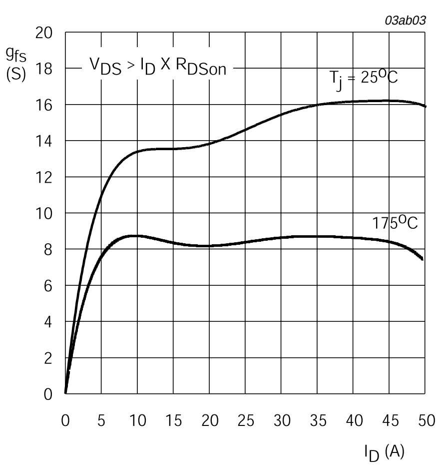
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature.



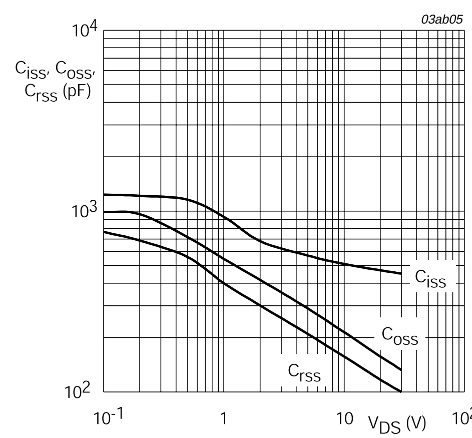
T_j = 25 °C; V_{DS} = 5 V

Fig 11. Sub-threshold drain current as a function of gate-source voltage.



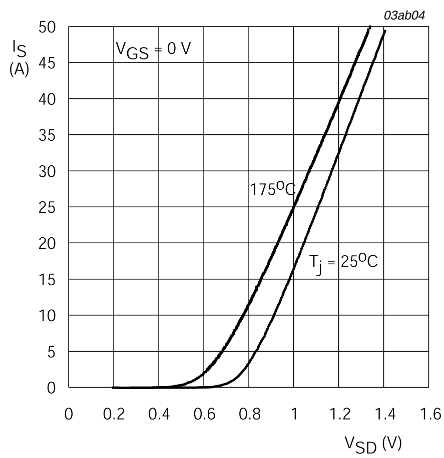
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 12. Forward transconductance as a function of drain current; typical values.



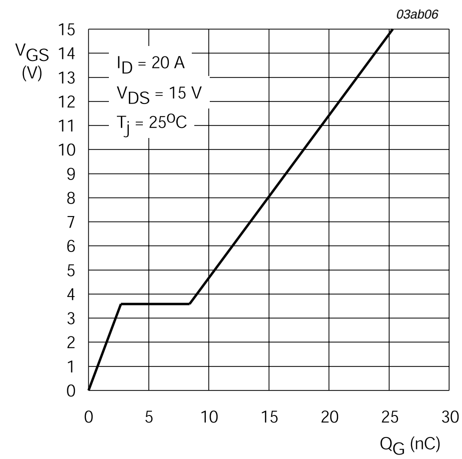
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

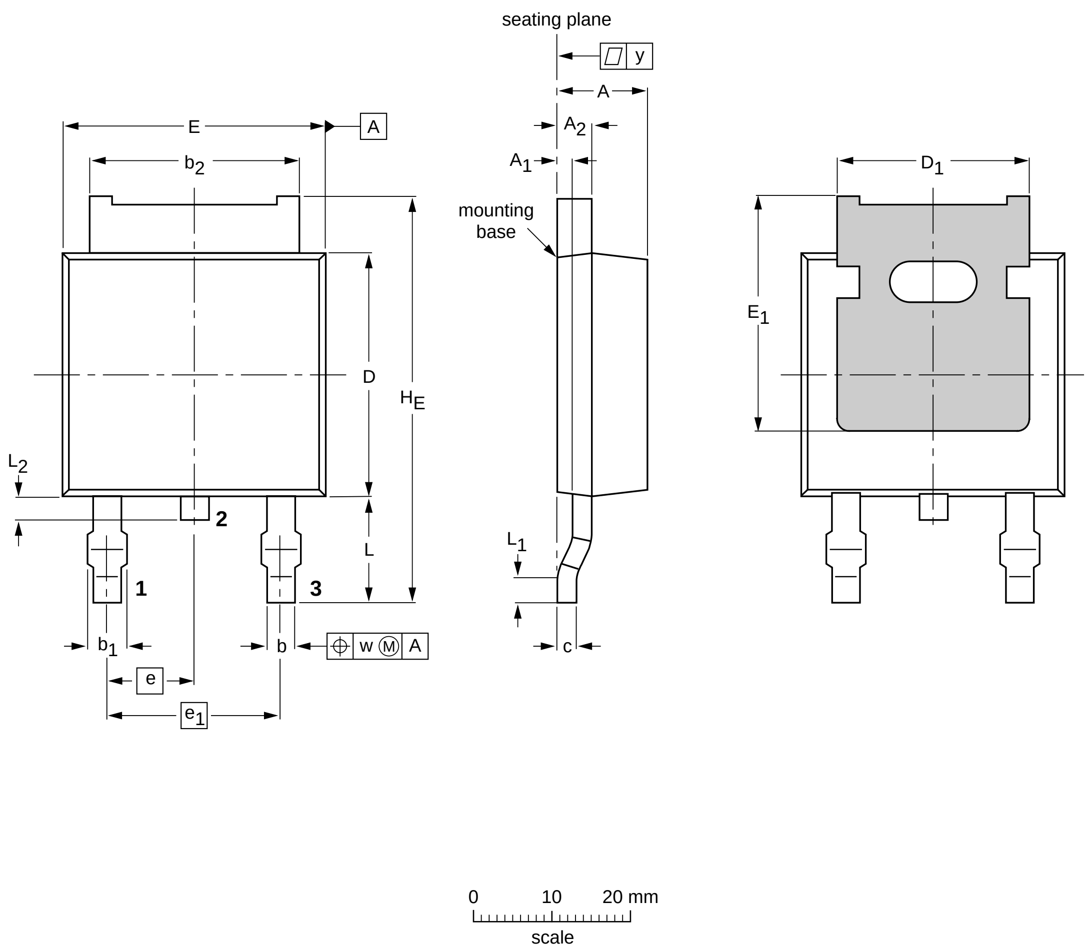


I_D = 20 A; V_{DS} = 15 V

Fig 15. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 (1)	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252	SC-63			~~98-04-07~~ 99-09-13

Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20000727	-	Product specification; second version; supersedes PHD24N03LT_1 of 991201.
01	19991201	-	Product specification; initial version.

11. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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