

PowerMOS transistor

PHD12N10E

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

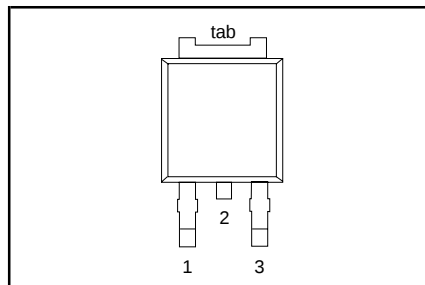
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	14	A
P_{tot}	Total power dissipation	75	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.16	Ω

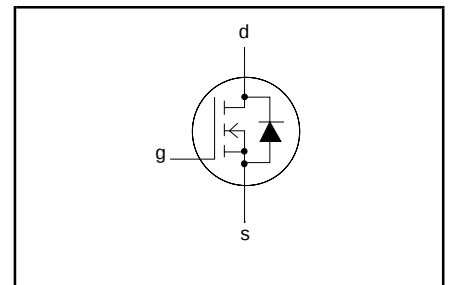
PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	14	A
I_D	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	10	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	56	A
P_{tot}	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	75	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction Temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th \text{ j-mb}}$	Thermal resistance junction to mounting base		-	2	K/W
$R_{th \text{ j-a}}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

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STATIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	-	0.15	0.16	Ω

DYNAMIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5\text{ A}$	4.0	5.5	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	660	825	pF
C_{oss}	Output capacitance		-	140	200	pF
C_{rss}	Feedback capacitance		-	60	100	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ $R_{gen} = 50\text{ }\Omega$	-	10	20	ns
t_r	Turn-on rise time		-	25	40	ns
t_{doff}	Turn-off delay time		-	60	90	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	14	A
I_{DRM}	Pulsed reverse drain current	-	-	-	56	A
V_{SD}	Diode forward voltage	$I_F = 14\text{ A}; V_{GS} = 0\text{ V}$	-	1.2	1.5	V
t_{rr}	Reverse recovery time	$I_F = 14\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	90	-	ns
Q_{rr}	Reverse recovery charge		-	0.6	-	μC

AVALANCHE LIMITING VALUE $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 14\text{ A}; V_{DD} \leq 50\text{ V}; V_{GS} = 10\text{ V};$ $R_{GS} = 50\text{ }\Omega$	-	-	70	mJ

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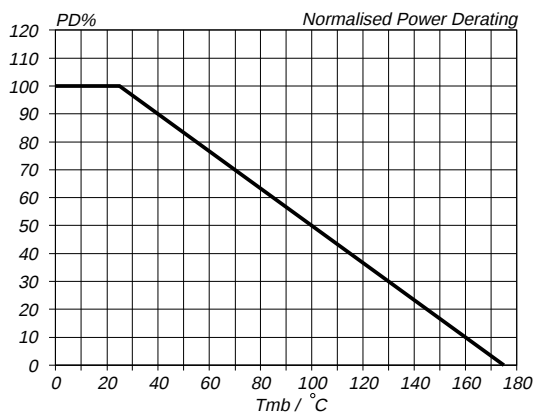


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_{mb})$

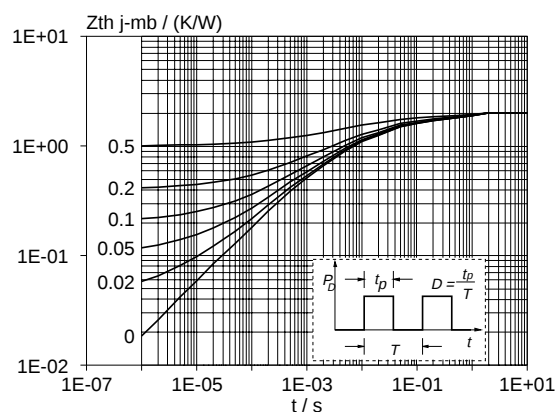


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

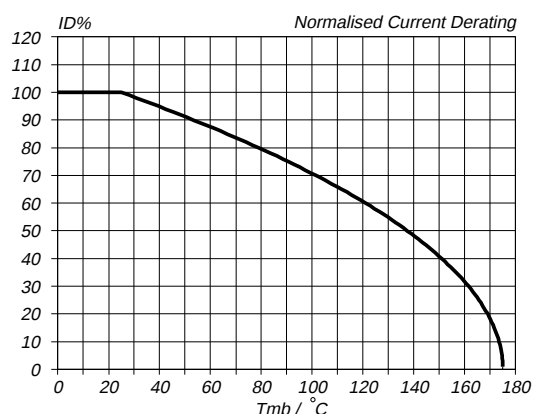


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 10\ V$

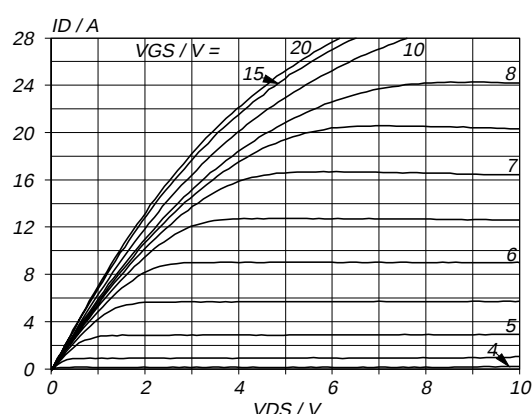


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
 $I_D = f(V_{DS})$; parameter V_{GS}

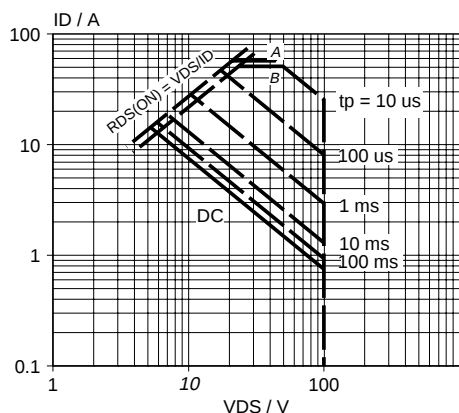


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

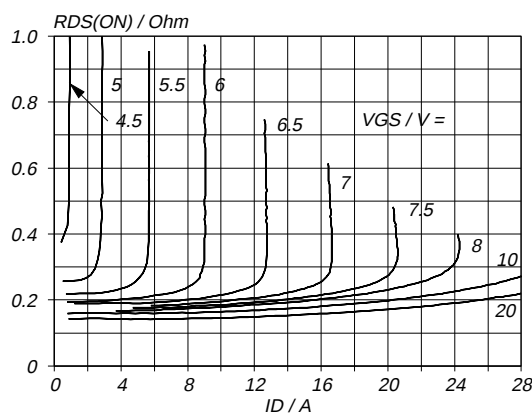


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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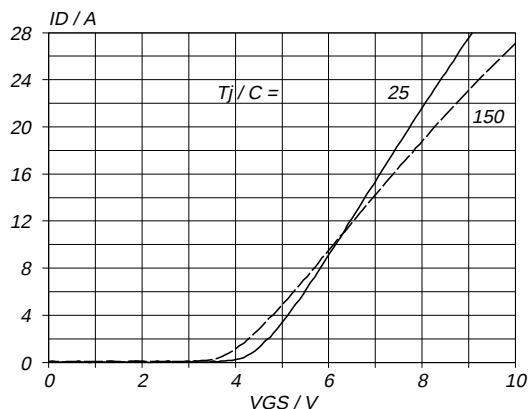


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25$ V; parameter T_j

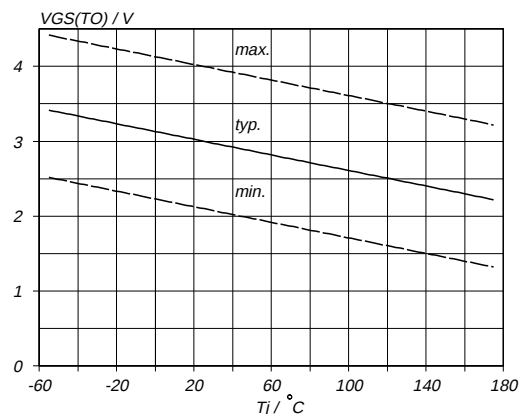


Fig. 10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

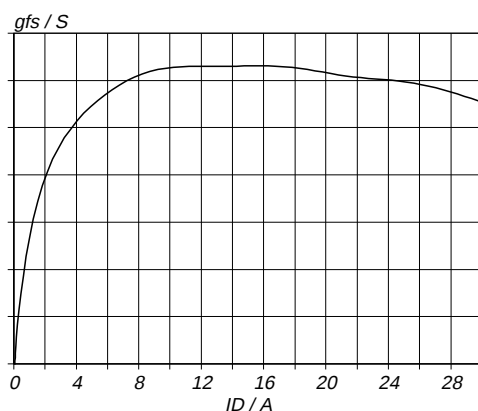


Fig. 8. Typical transconductance, $T_j = 25$ °C.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25$ V

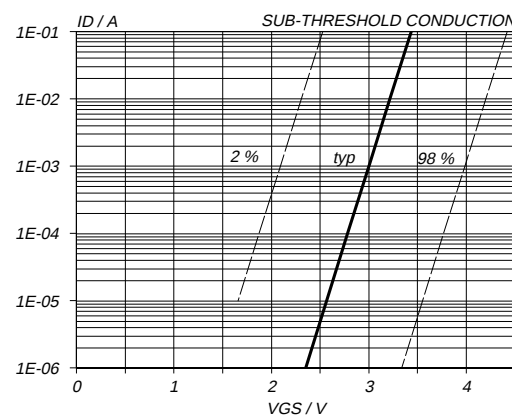


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

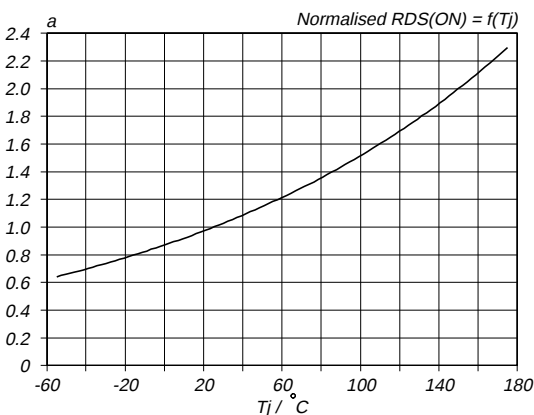


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)} / R_{DS(ON)25\text{ °C}} = f(T_j)$; $I_D = 5$ A; $V_{GS} = 10$ V

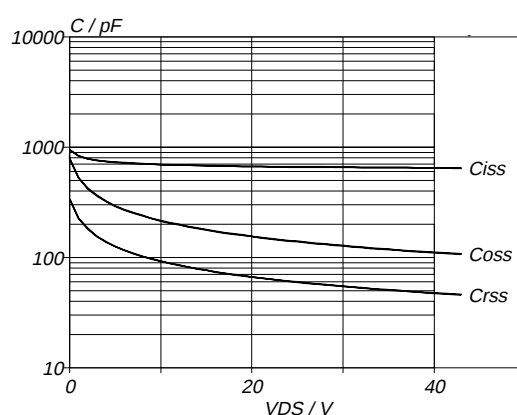


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

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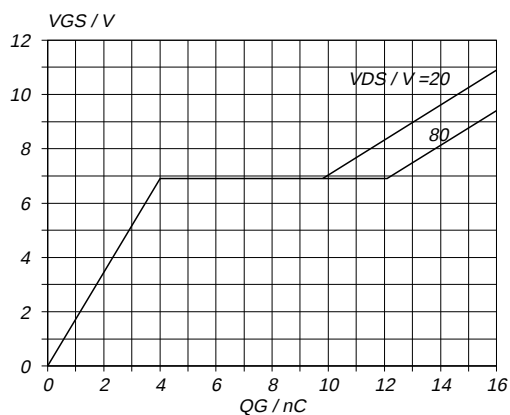


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

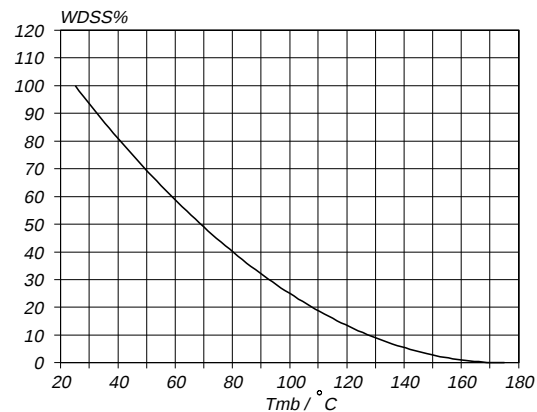


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 14$ A

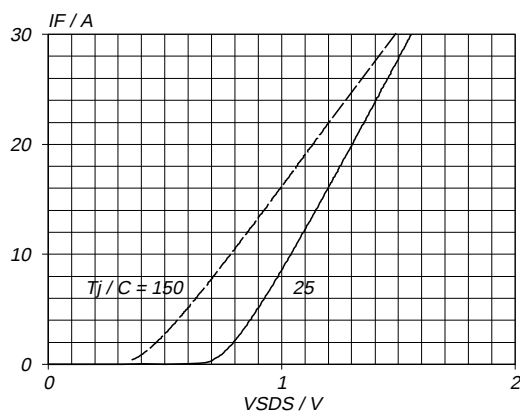


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

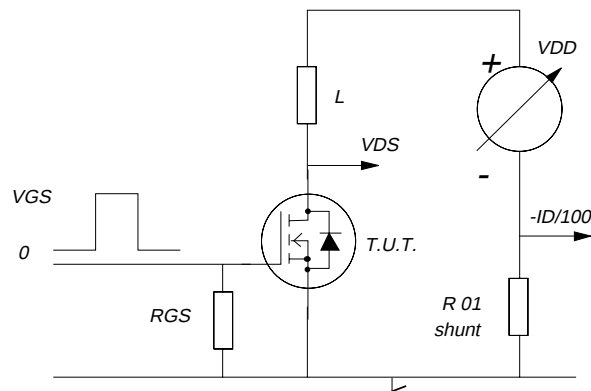


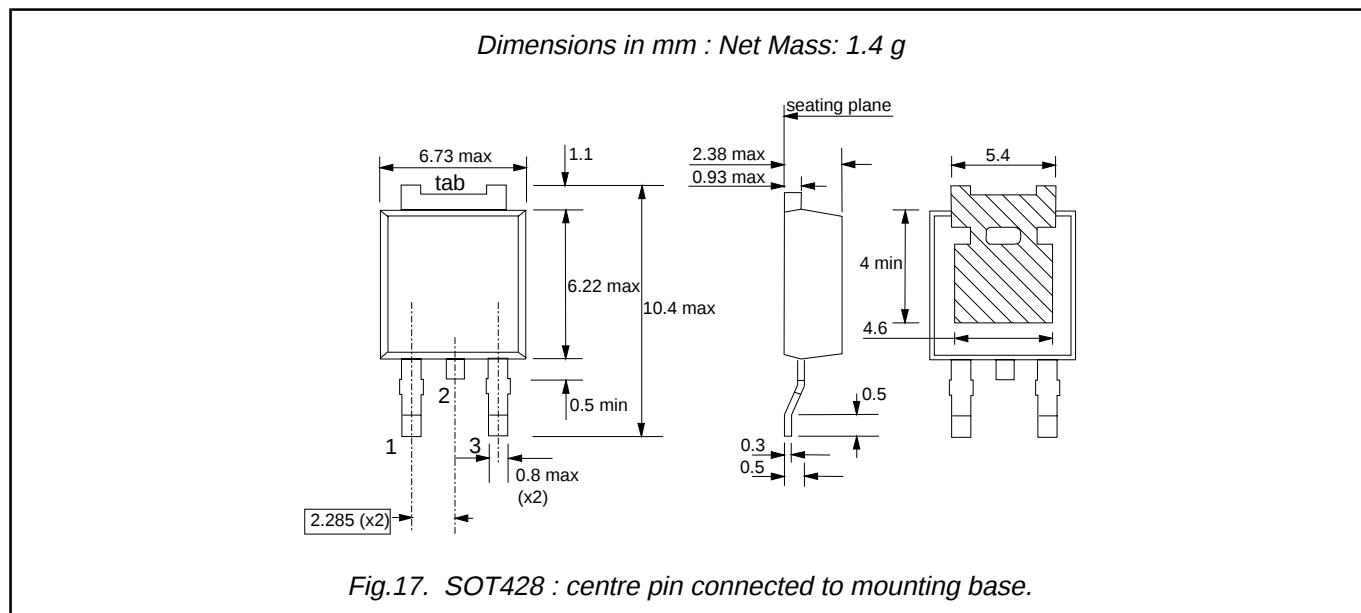
Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$$

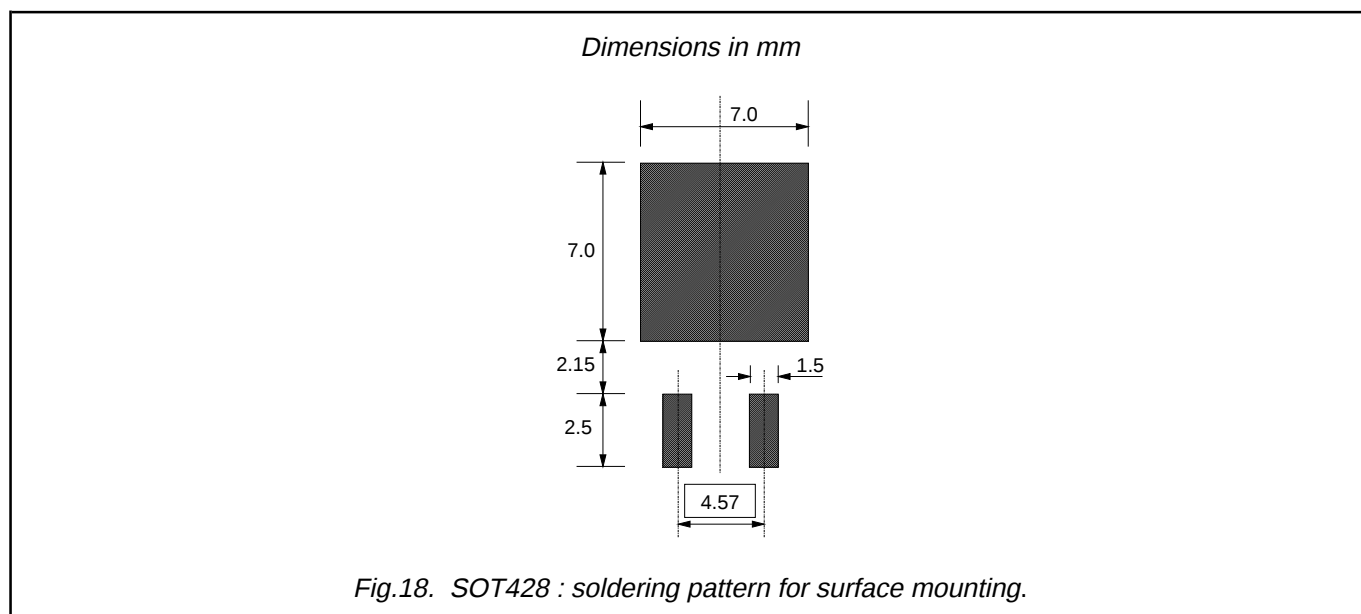
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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