

# DATA SHEET

## **PHC20512**

Complementary enhancement  
mode

MOS transistors

Product specification  
Supersedes data of 1997 Jun 19  
File under Discrete Semiconductors, SC13b

1997 Oct 22

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MOS transistors

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

| PIN | SYMBOL         | DESCRIPTION |
|-----|----------------|-------------|
| 1   | s <sub>1</sub> | source 1    |
| 2   | g <sub>1</sub> | gate 1      |
| 3   | s <sub>2</sub> | source 2    |
| 4   | g <sub>2</sub> | gate 2      |
| 5   | d <sub>2</sub> | drain 2     |
| 6   | d <sub>2</sub> | drain 2     |
| 7   | d <sub>1</sub> | drain 1     |
| 8   | d <sub>1</sub> | drain 1     |

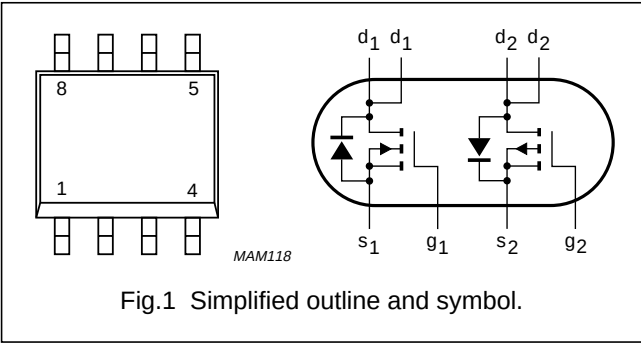


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

| SYMBOL            | PARAMETER                          | CONDITIONS                                                 | MIN. | MAX. | UNIT |
|-------------------|------------------------------------|------------------------------------------------------------|------|------|------|
| Per channel       |                                    |                                                            |      |      |      |
| V <sub>DS</sub>   | drain-source voltage (DC)          |                                                            |      |      |      |
|                   | N-channel                          |                                                            | –    | 30   | V    |
|                   | P-channel                          |                                                            | –    | –30  | V    |
| V <sub>SD</sub>   | source-drain diode forward voltage |                                                            |      |      |      |
|                   | N-channel                          | I <sub>S</sub> = 1.25 A                                    | –    | 1    | V    |
|                   | P-channel                          | I <sub>S</sub> = –1.25 A                                   | –    | –1.3 | V    |
| V <sub>GS</sub>   | gate-source voltage (DC)           |                                                            | –    | ±20  | V    |
| V <sub>GStH</sub> | gate-source threshold voltage      |                                                            |      |      |      |
|                   | N-channel                          | V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA  | 1    | 2.8  | V    |
|                   | P-channel                          | V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = –1 mA | –1   | –2.8 | V    |
| I <sub>D</sub>    | drain current (DC)                 | T <sub>s</sub> = 80 °C                                     |      |      |      |
|                   | N-channel                          |                                                            | –    | 6.4  | A    |
|                   | P-channel                          |                                                            | –    | –4   | A    |
| R <sub>DSon</sub> | drain-source on-state resistance   |                                                            |      |      |      |
|                   | N-channel                          | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 3.2 A             | –    | 0.05 | Ω    |
|                   | P-channel                          | V <sub>GS</sub> = –10 V I <sub>D</sub> = –2 A              | –    | 0.12 | Ω    |
| P <sub>tot</sub>  | total power dissipation            | T <sub>s</sub> = 80 °C                                     | –    | 3.5  | W    |

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL                    | PARAMETER                      | CONDITIONS                        | MIN. | MAX. | UNIT |
|---------------------------|--------------------------------|-----------------------------------|------|------|------|
| <b>Per channel</b>        |                                |                                   |      |      |      |
| $V_{DS}$                  | drain-source voltage (DC)      |                                   |      |      |      |
|                           | N-channel                      |                                   | –    | 30   | V    |
|                           | P-channel                      |                                   | –    | –30  | V    |
| $V_{GS}$                  | gate-source voltage (DC)       |                                   | –    | ±20  | V    |
| $I_D$                     | drain current (DC)             | $T_s = 80\text{ °C}$ ; note 1     |      |      |      |
|                           | N-channel                      |                                   | –    | 6.4  | A    |
|                           | P-channel                      |                                   | –    | –4   | A    |
| $I_{DM}$                  | peak drain current             | note 2                            |      |      |      |
|                           | N-channel                      |                                   | –    | 25   | A    |
|                           | P-channel                      |                                   | –    | –16  | A    |
| $P_{tot}$                 | total power dissipation        | $T_s = 80\text{ °C}$ ; note 3     | –    | 3.5  | W    |
|                           |                                | $T_{amb} = 25\text{ °C}$ ; note 4 | –    | 2.6  | W    |
|                           |                                | $T_{amb} = 25\text{ °C}$ ; note 5 | –    | 1.1  | W    |
|                           |                                | $T_{amb} = 25\text{ °C}$ ; note 6 | –    | 1.5  | W    |
| $T_{stg}$                 | storage temperature            |                                   | –65  | +150 | °C   |
| $T_j$                     | operating junction temperature |                                   | –65  | +150 | °C   |
| <b>Source-drain diode</b> |                                |                                   |      |      |      |
| $I_S$                     | source current (DC)            | $T_s = 80\text{ °C}$              |      |      |      |
|                           | N-channel                      |                                   | –    | 3.5  | A    |
|                           | P-channel                      |                                   | –    | –2.6 | A    |
| $I_{SM}$                  | peak pulsed source current     | note 2                            |      |      |      |
|                           | N-channel                      |                                   | –    | 14   | A    |
|                           | P-channel                      |                                   | –    | –10  | A    |

## Notes

- $T_s$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 27.5 K/W.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 90 K/W.
- Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 90 K/W.

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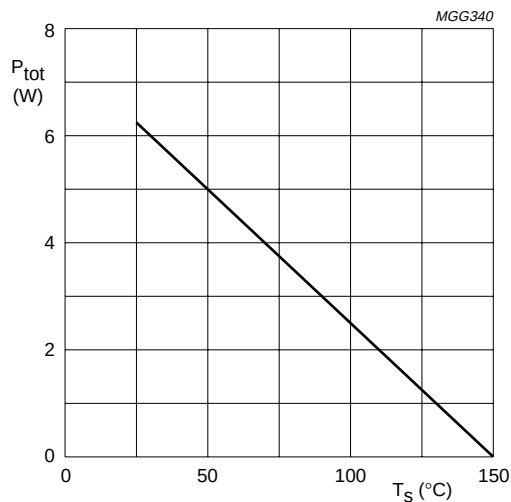
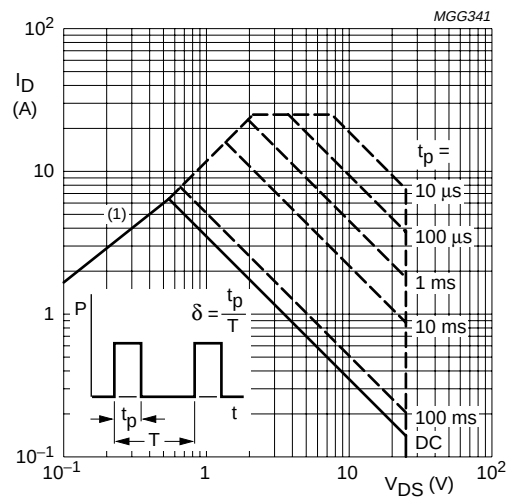
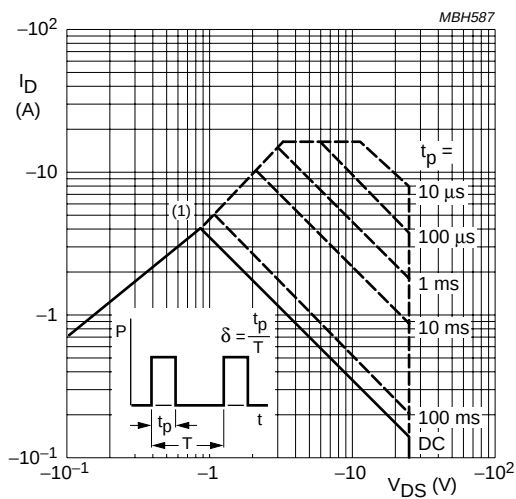


Fig.2 Power derating curve.



$\delta = 0.01$ ;  $T_s = 80$  °C.  
(1)  $R_{DSon}$  limitation.

Fig.3 SOAR; N-channel.



$\delta = 0.01$ ;  $T_s = 80$  °C.  
(1)  $R_{DSon}$  limitation.

Fig.4 SOAR; P-channel.

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## THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                           | VALUE | UNIT |
|---------------|-----------------------------------------------------|-------|------|
| $R_{th\ j-s}$ | thermal resistance from junction to soldering point | 20    | K/W  |

## CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$  unless otherwise specified.

| SYMBOL             | PARAMETER                        | CONDITIONS                                                           | MIN. | TYP. | MAX.      | UNIT     |
|--------------------|----------------------------------|----------------------------------------------------------------------|------|------|-----------|----------|
| <b>Per channel</b> |                                  |                                                                      |      |      |           |          |
| $V_{(BR)DSS}$      | drain-source breakdown voltage   |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 0; I_D = 10\ \mu\text{A}$                                  | 30   | –    | –         | V        |
|                    | P-channel                        | $V_{GS} = 0; I_D = -10\ \mu\text{A}$                                 | -30  | –    | –         | V        |
| $V_{GSth}$         | gate-source threshold voltage    |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = V_{DS}; I_D = 1\ \text{mA}$                                | 1    | –    | 2.8       | V        |
|                    | P-channel                        | $V_{GS} = V_{DS}; I_D = -1\ \text{mA}$                               | -1   | –    | -2.8      | V        |
| $I_{DSS}$          | drain-source leakage current     |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 0; V_{DS} = 24\ \text{V}$                                  | –    | –    | 100       | nA       |
|                    | P-channel                        | $V_{GS} = 0; V_{DS} = -24\ \text{V}$                                 | –    | –    | -100      | nA       |
| $I_{GSS}$          | gate leakage current             | $V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$                              |      |      |           |          |
|                    | N-channel                        |                                                                      | –    | –    | $\pm 100$ | nA       |
|                    | P-channel                        |                                                                      | –    | –    | $\pm 100$ | nA       |
| $R_{DSon}$         | drain-source on-state resistance |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 4.5\ \text{V}; I_D = 1.6\ \text{A}$                        | –    | –    | 0.1       | $\Omega$ |
|                    |                                  | $V_{GS} = 10\ \text{V}; I_D = 3.2\ \text{A}$                         | –    | –    | 0.05      | $\Omega$ |
|                    | P-channel                        | $V_{GS} = -4.5\ \text{V}; I_D = -1\ \text{A}$                        | –    | –    | 0.25      | $\Omega$ |
|                    |                                  | $V_{GS} = -10\ \text{V}; I_D = -2\ \text{A}$                         | –    | –    | 0.12      | $\Omega$ |
| $C_{iss}$          | input capacitance                |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$               | –    | 450  | –         | pF       |
|                    | P-channel                        | $V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$              | –    | 450  | –         | pF       |
| $C_{oss}$          | output capacitance               |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$               | –    | 200  | –         | pF       |
|                    | P-channel                        | $V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$              | –    | 200  | –         | pF       |
| $C_{rss}$          | reverse transfer capacitance     |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$               | –    | 100  | –         | pF       |
|                    | P-channel                        | $V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$              | –    | 100  | –         | pF       |
| $Q_G$              | total gate charge                |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 3.2\ \text{A}$  | –    | 15   | –         | nC       |
|                    | P-channel                        | $V_{GS} = -10\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -2\ \text{A}$ | –    | 13   | –         | nC       |
| $Q_{GS}$           | gate-source charge               |                                                                      |      |      |           |          |
|                    | N-channel                        | $V_{GS} = 10\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 3.2\ \text{A}$  | –    | 1    | –         | nC       |
|                    | P-channel                        | $V_{GS} = -10\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -2\ \text{A}$ | –    | 1    | –         | nC       |

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|---------------------------|------------------------------------|----------------------------------------------------------------------------------------------------|------|------|------|------|
| $Q_{GD}$                  | gate-drain charge                  |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 10\text{ V}; V_{DD} = 15\text{ V}; I_D = 3.2\text{ A}$                                   | –    | 5    | –    | nC   |
|                           | P-channel                          | $V_{GS} = -10\text{ V}; V_{DD} = -15\text{ V}; I_D = -2\text{ A}$                                  | –    | 4    | –    | nC   |
| $t_{d(on)}$               | turn-on delay time                 |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 0\text{ to }10\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 7    | –    | ns   |
|                           | P-channel                          | $V_{GS} = 0\text{ to }-10\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 6    | –    | ns   |
| $t_{d(off)}$              | turn-off delay time                |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 10\text{ to }0\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 20   | –    | ns   |
|                           | P-channel                          | $V_{GS} = -10\text{ to }0\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 29   | –    | ns   |
| $t_f$                     | fall time                          |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 0\text{ to }10\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 8    | –    | ns   |
|                           | P-channel                          | $V_{GS} = -10\text{ to }0\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 16   | –    | ns   |
| $t_r$                     | rise time                          |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 10\text{ to }0\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 12   | –    | ns   |
|                           | P-channel                          | $V_{GS} = 0\text{ to }-10\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 4    | –    | ns   |
| $t_{on}$                  | turn-on switching time             |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 0\text{ to }10\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 15   | –    | ns   |
|                           | P-channel                          | $V_{GS} = 0\text{ to }-10\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 10   | –    | ns   |
| $t_{off}$                 | turn-off switching time            |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GS} = 10\text{ to }0\text{ V}; V_{DD} = 15\text{ V}; I_D = 1\text{ A}; R_{gen} = 6\ \Omega$    | –    | 32   | –    | ns   |
|                           | P-channel                          | $V_{GS} = -10\text{ to }0\text{ V}; V_{DD} = -15\text{ V}; I_D = -1\text{ A}; R_{gen} = 6\ \Omega$ | –    | 45   | –    | ns   |
| <b>Source-drain diode</b> |                                    |                                                                                                    |      |      |      |      |
| $V_{SD}$                  | source-drain diode forward voltage |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $V_{GD} = 0; I_S = 1.25\text{ A}$                                                                  | –    | –    | 1    | V    |
|                           | P-channel                          | $V_{GD} = 0; I_S = -1.25\text{ A}$                                                                 | –    | –    | -1.3 | V    |
| $t_{rr}$                  | reverse recovery time              |                                                                                                    |      |      |      |      |
|                           | N-channel                          | $I_S = 1.25\text{ A}; di/dt = -100\text{ A}/\mu\text{s}$                                           | –    | 45   | –    | ns   |
|                           | P-channel                          | $I_S = -1.25\text{ A}; di/dt = 100\text{ A}/\mu\text{s}$                                           | –    | 75   | –    | ns   |

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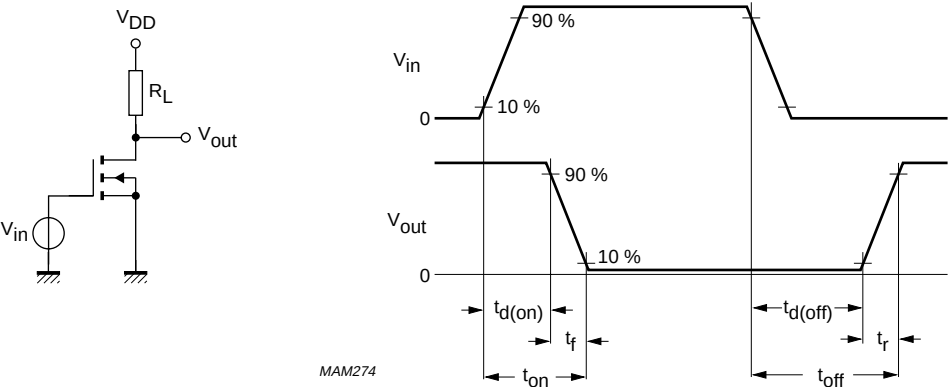


Fig.5 Switching times test circuit with input and output waveforms; N-channel.

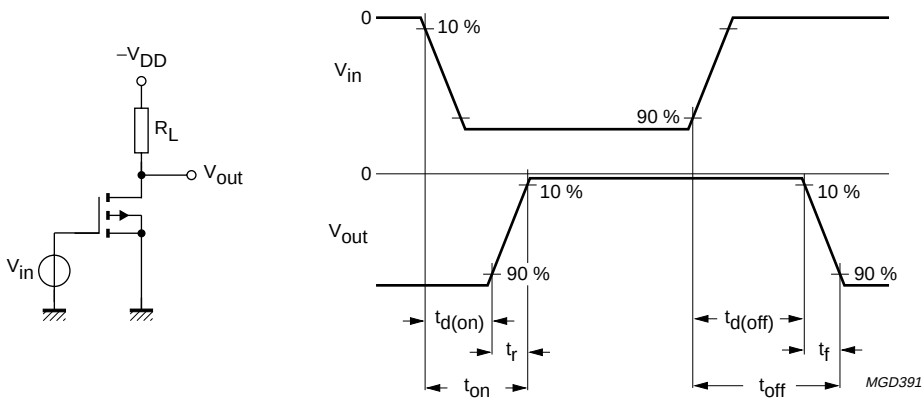
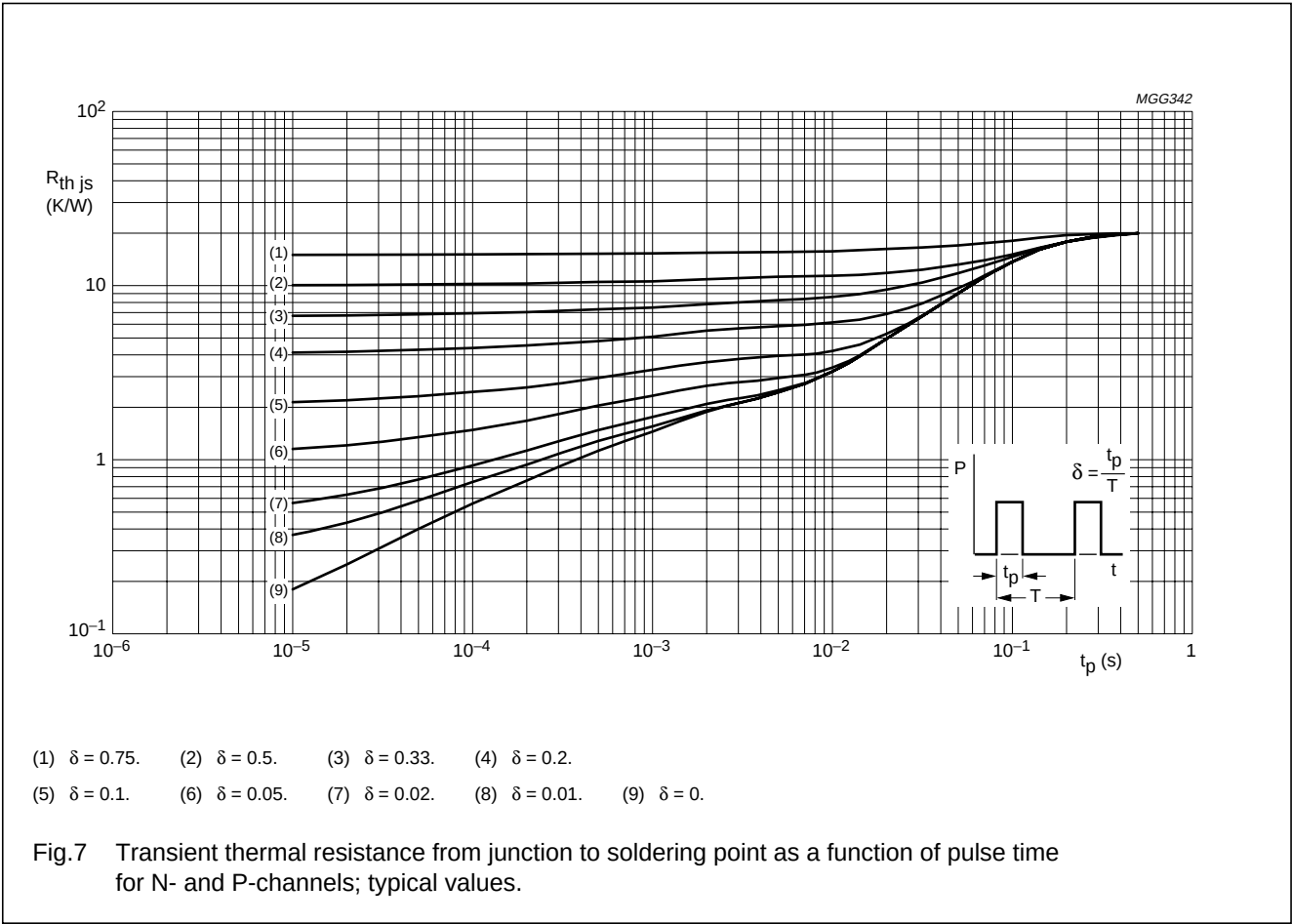


Fig.6 Switching times test circuit with input and output waveforms; P-channel.

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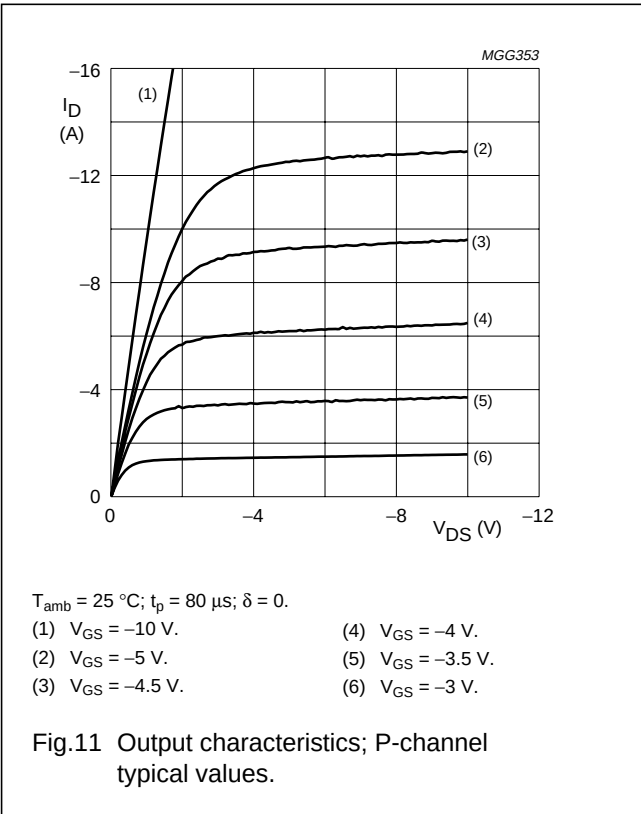
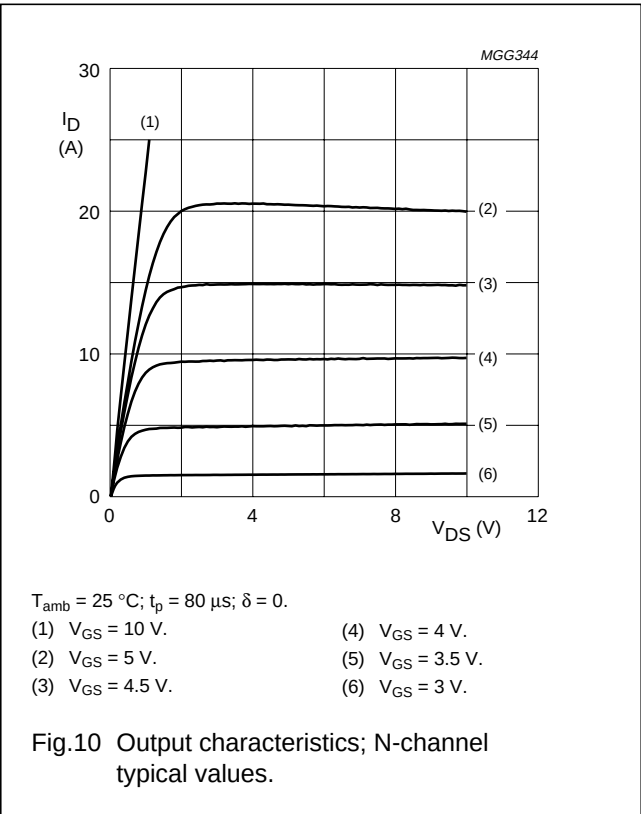
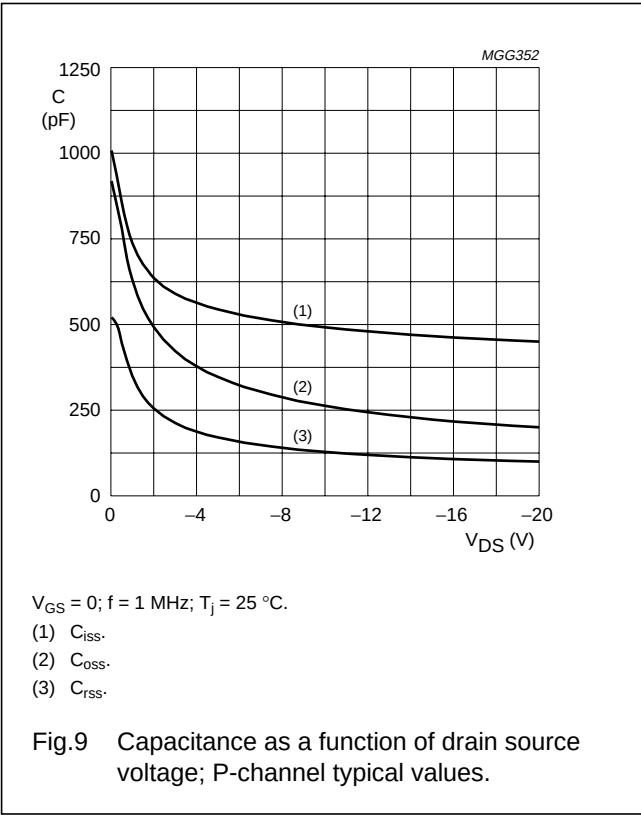
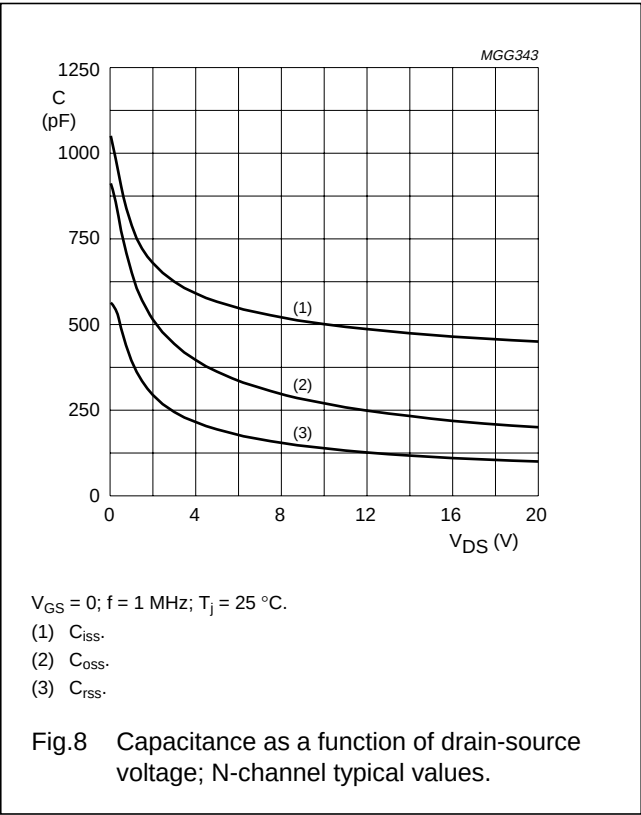
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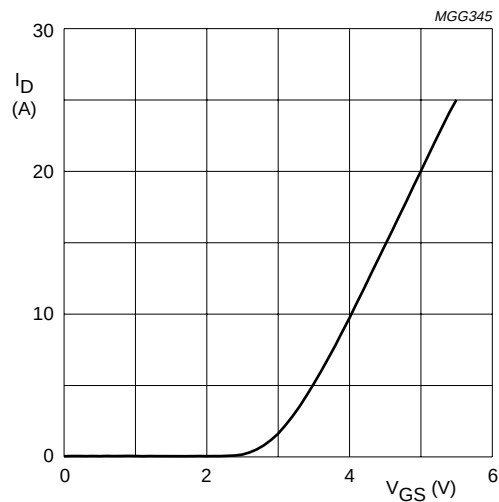
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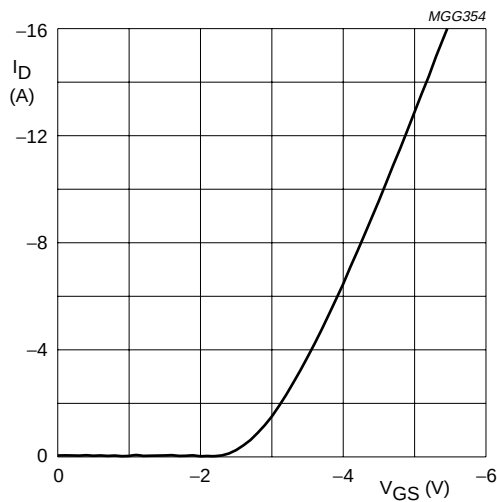
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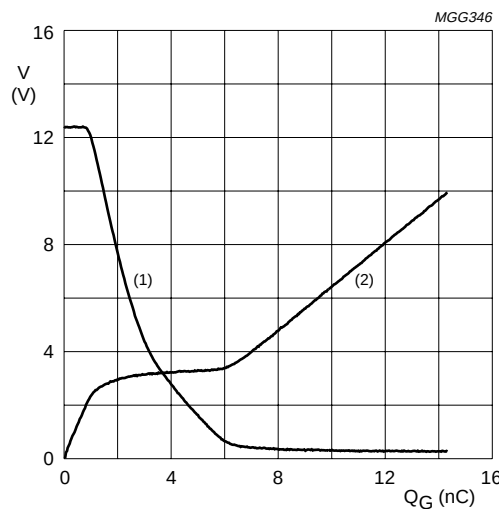
$V_{DS} = 10\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 80\text{ }\mu\text{s}$ ;  $\delta = 0$ .

Fig.12 Transfer characteristic; N-channel typical values.



$V_{DS} = -10\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 80\text{ }\mu\text{s}$ ;  $\delta = 0$ .

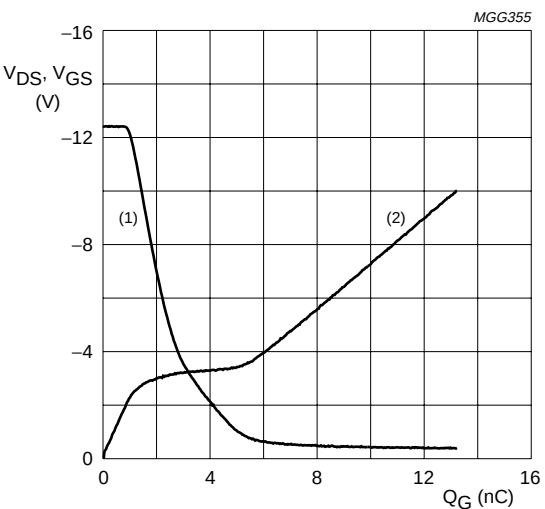
Fig.13 Transfer characteristic; P-channel typical values.



$V_{DD} = 12.5\text{ V}$ ;  $I_D = 3.2\text{ A}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

- (1)  $V_{DS}$ .
- (2)  $V_{GS}$ .

Fig.14 Gate-source voltage and drain-source voltage as a function of total gate charge; N-channel typical values.



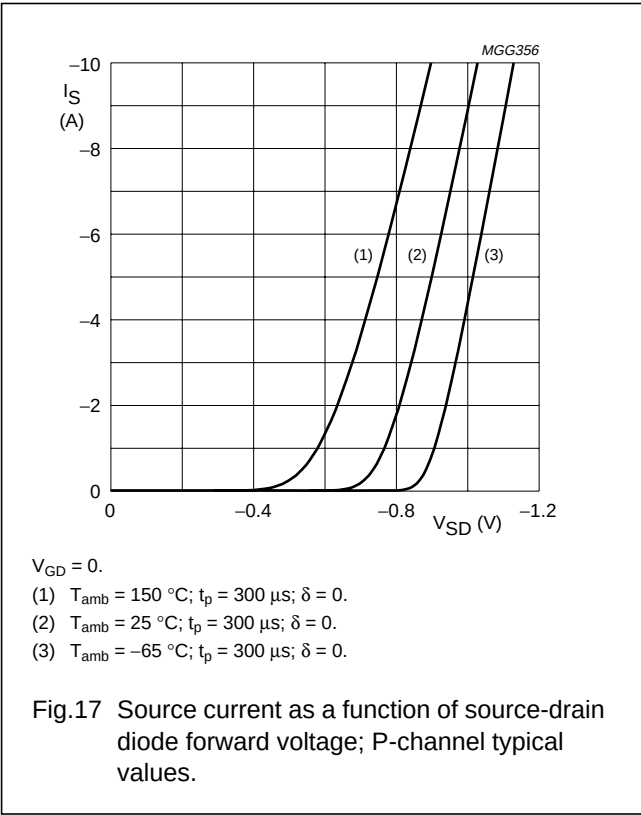
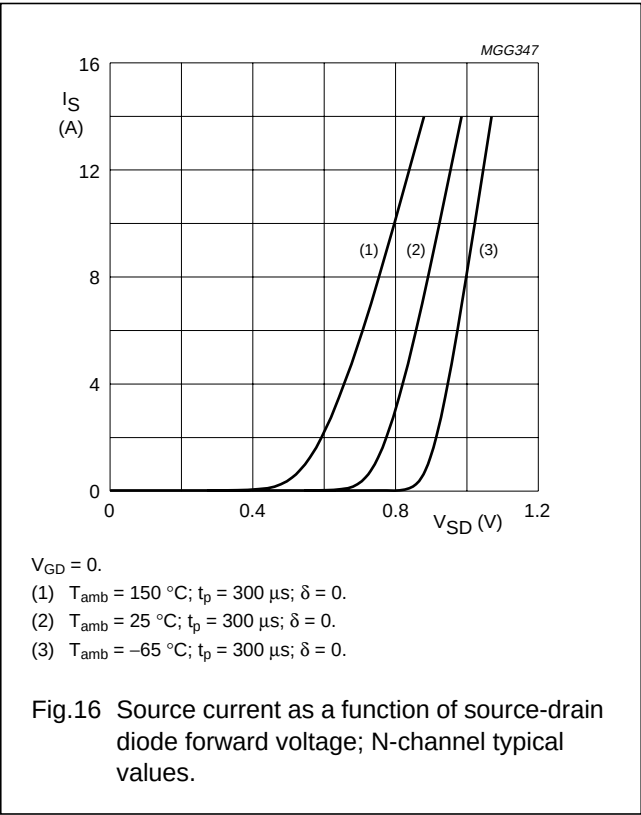
$V_{DD} = -12.5\text{ V}$ ;  $I_D = -2\text{ A}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

- (1)  $V_{DS}$ .
- (2)  $V_{GS}$ .

Fig.15 Gate-source voltage and drain-source voltage as a function of total gate charge; P-channel typical values.

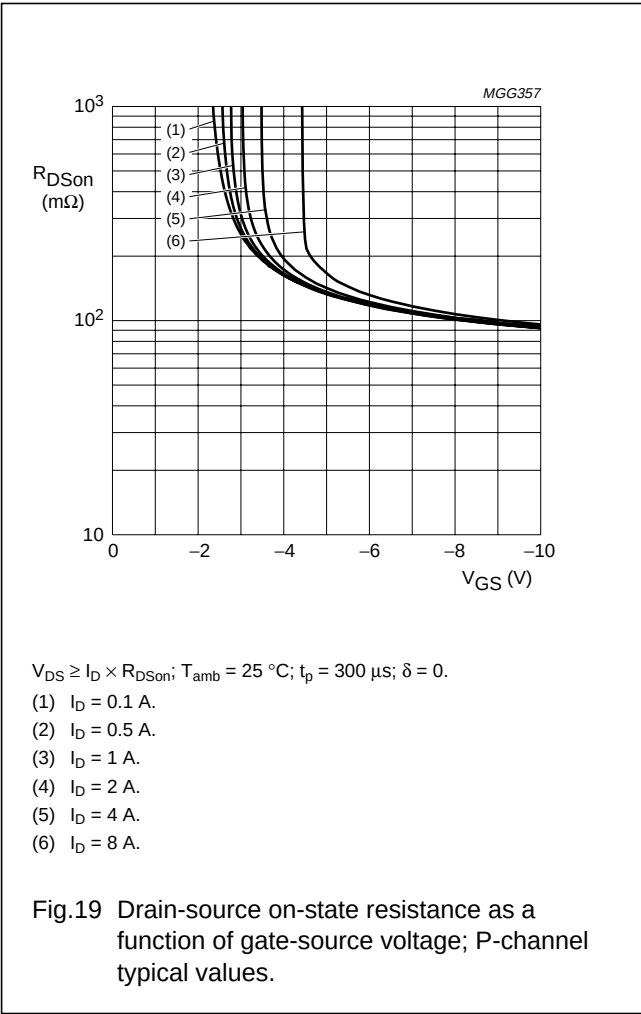
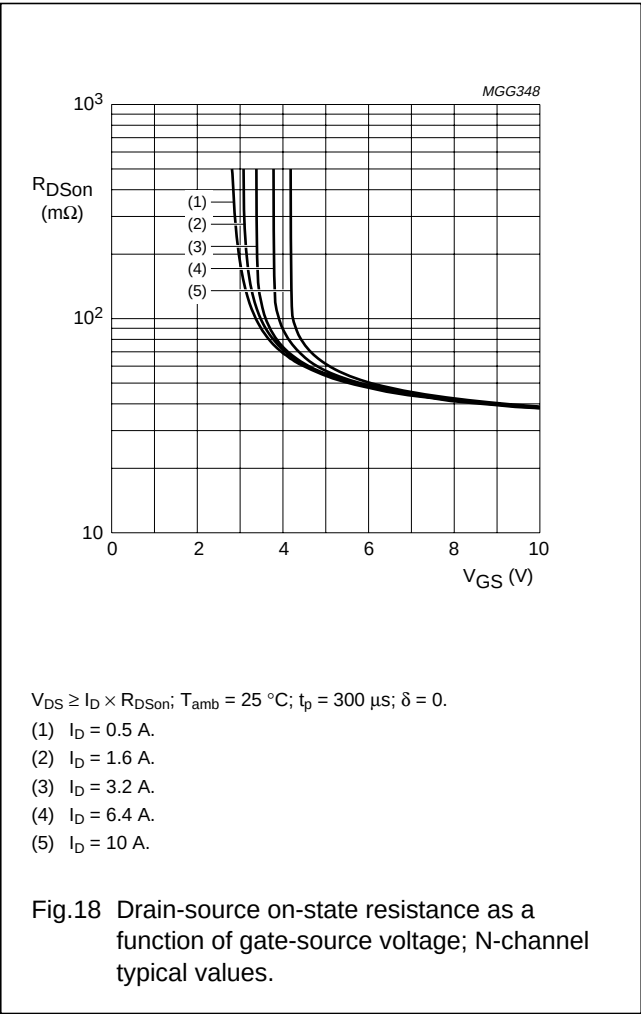
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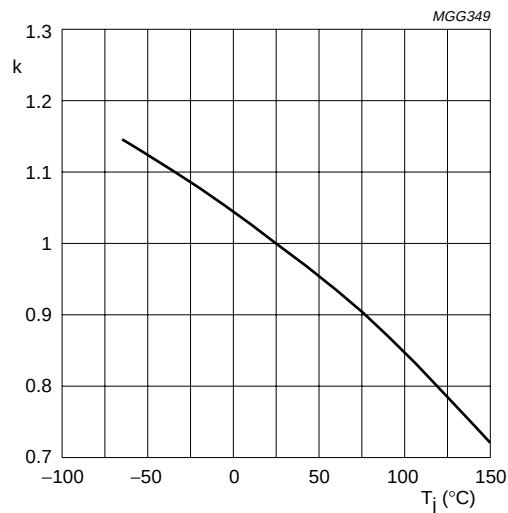
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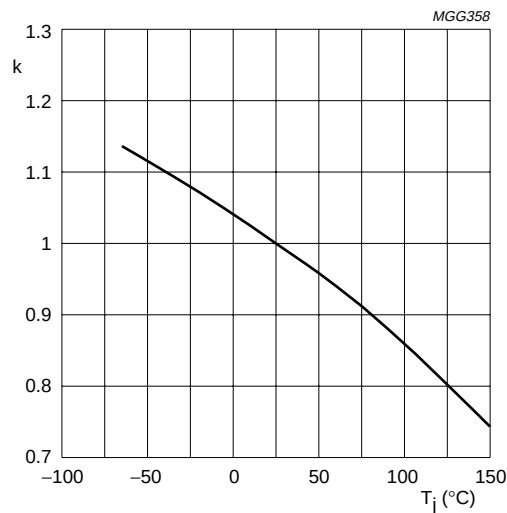
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$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

$V_{GSth}$  at  $V_{DS} = V_{GS}$ ;  $I_D = 1 \text{ mA}$ .

Fig.20 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; N-channel typical values.



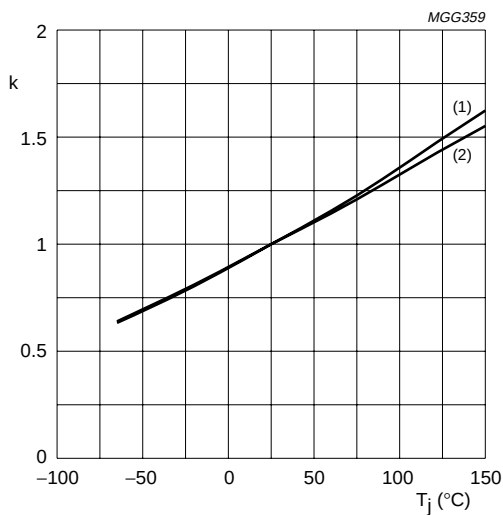
$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

$V_{GSth}$  at  $V_{DS} = V_{GS}$ ;  $I_D = -1 \text{ mA}$ .

Fig.21 Temperature coefficient of gate-source threshold voltage as function of junction temperature; P-channel typical values.

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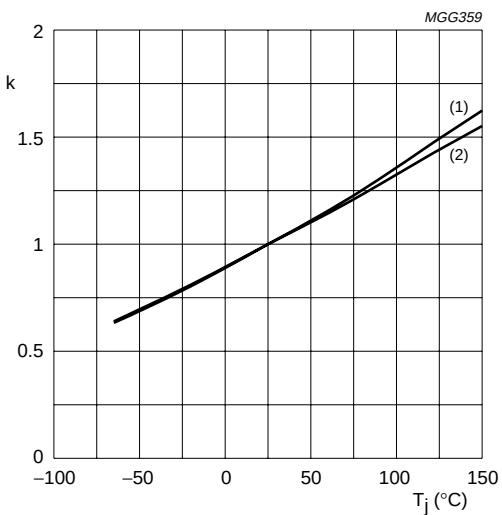
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$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

- (1)  $R_{DSon}$  at  $V_{GS} = 10\text{ V}$ ;  $I_D = 3.2\text{ A}$ .
- (2)  $R_{DSon}$  at  $V_{GS} = 4.5\text{ V}$ ;  $I_D = 1.6\text{ A}$ .

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

- (1)  $R_{DSon}$  at  $V_{GS} = -10\text{ V}$ ;  $I_D = -2\text{ A}$ .
- (2)  $R_{DSon}$  at  $V_{GS} = -4.5\text{ V}$ ;  $I_D = -1\text{ A}$ .

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

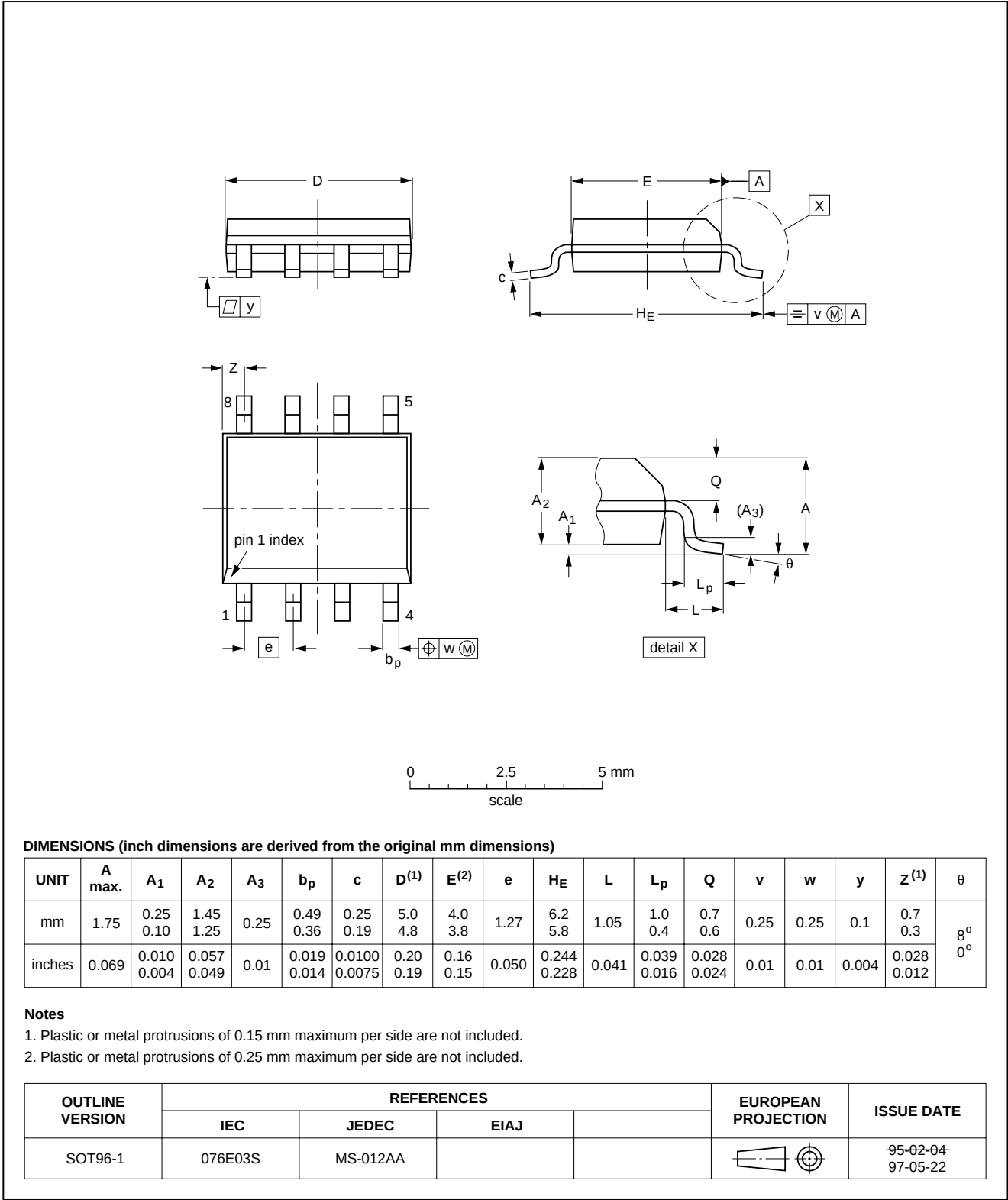
Complementary enhancement mode  
MOS transistors

PHC20512

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



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## Complementary enhancement mode MOS transistors

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PHC20512

### DEFINITIONS

| Data Sheet Status                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                                                                                                                                                                                                                                                                                                                                                                                   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                                                                                                                                                                                                                                                                                                                                                                                 | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                                                                                                                                                                                                                                                                                                                                                                                     | This data sheet contains final product specifications.                                |
| Limiting values                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                       |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |                                                                                       |
| Application information                                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification.                                                                                                                                                                                                                                                                                                                                                       |                                                                                       |

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.



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**Complementary enhancement mode  
MOS transistors**

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**PHC20512****NOTES**

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**Complementary enhancement mode  
MOS transistors**

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**PHC20512****NOTES**

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**Complementary enhancement mode  
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**PHC20512****NOTES**

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